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Schematics and other handouts serve for informational purposes only!

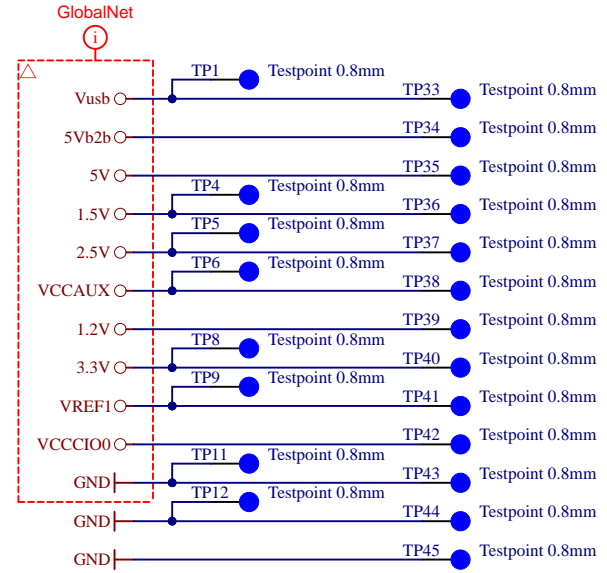
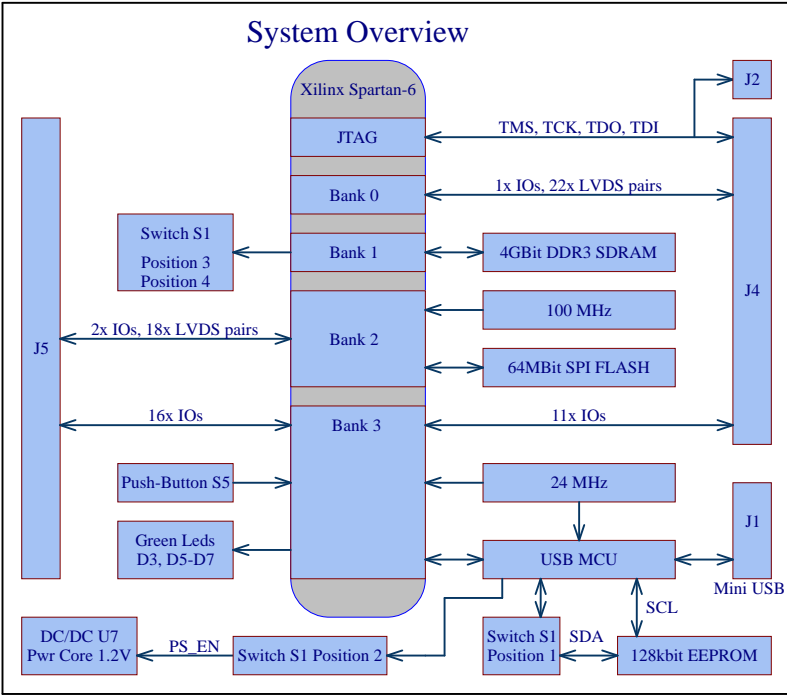


Title: TE0630 - Legal Notices Modules		
A4	Number: TE0630 63I22-A	Rev. 03
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Filename: Legal_Notices.SchDoc		

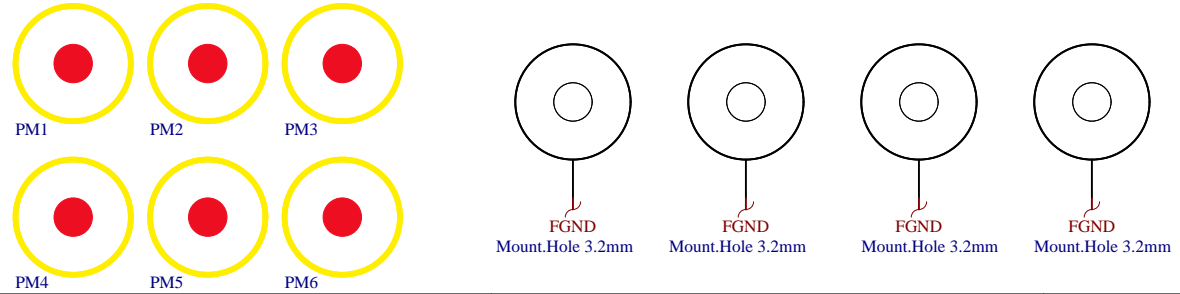
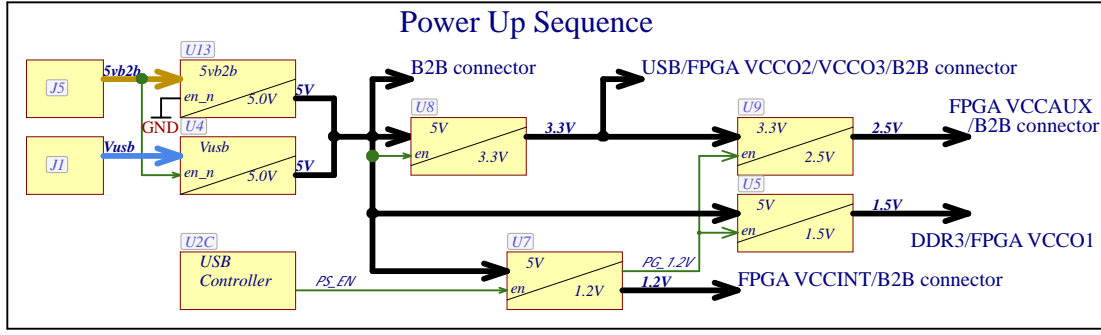
REV	Description	
-01	Initial revision	
-02	1) Replaced U8 by EN6338QI 2) Rerouted nets around U8, results in new track length for: Signal V3_IO_06 15.2475 mm (was 15.0047mm) Signal V3_IO_07 16.0151 mm (was 15.0452 mm) 3) Replaced U5 by EN 6338QI 4) PS_EN now via OR gate 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A 6) Fixed Footprint of U10 according to datasheet 7) Update from LIB 8) Rearranged Testpoints 9) Added Traceability Pad 10) Replaced S5 by smaller PB AN26337 11) Hardware revision coding updated to Rev02 12) Flash change (U14) 2020-03-30	
-03	1) All sch and pcb components were updated 2) R46 was changed to 330 Ohm 3) "TE0630.SchDoc" page was updated: System Overview was redesigned, Power Up Sequence was added, S/N1 Serialnumber was removed 4) U7 was changed from EN6347QI to MPM3860GQW-Z 5) U8 and U5 were changed from EN6338QI to MPM3834CGPA 6) Added pullups R84 and R85 for ST pin of U10 and U11 on page "FPGA_CFG_CLK.SchDoc" 7) TE logo was changed to UKCA Logo on page "TE0630.SchDoc" 8) "B2B_Connectors.SchDoc" page was updated: service information about IOs pins was added, colored signal groups were added 9) BR0 net was pulled to 1.5V on page "FPGA_DDR3.SchDoc" 10) U12 was changed from NT5CC64M16GP-DII to IS43TR16256BL-125KBLI 11) Assembly option. Pull down resistor R70 was added on page "FPGA_B0.SchDoc" 12) Assembly Variants table was changed on page "FPGA_DDR3.SchDoc": obsolete variants were deleted, new assembly variants were added 13) "Legal_Notices.SchDoc" page was added 14) Parameters of some capacitors were changed: C77 , C80 : 6.3V -> 10V 15) Fiducials PM1-PM6 were updated and moved for same positions on top and bottom layers 16) Removed testpoints TP2,TP3,TP7,TP10,TP13,TP14,TP15,TP17, TP19,TP20,TP21, TP27,TP28,TP30,TP31,TP32 17) Added testpoints TP27 and TP28 on page "USB.SchDoc" 18) Some net classes names were deleted: "MatchLendht150Mil", "MatchLendht300Mil", "Clear_10mil", "S50-33" 19) Net class "3Bank2Half" was renamed to "Bank3"	MT

	Title: TE0630 - Changes list		
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	Filename: Revision_Changes.SchDoc		

- U_Power
Power.SchDoc
- U_FPGA_PWR
FPGA_PWR.SchDoc
- UKCA
UKCA Logo on Top Overlay
UKCA-TOOVERLAY
- Serial
Serialnumber 6,3 x 6.3mm



Special notes:



BR0	BR1	BR2	BR3	See BR nets on page "FPGA_DDR3.SchDoc"
0	0	0	0	-00 Initial revision
1	0	0	0	-01
0	1	0	0	-02
1	1	0	0	-03

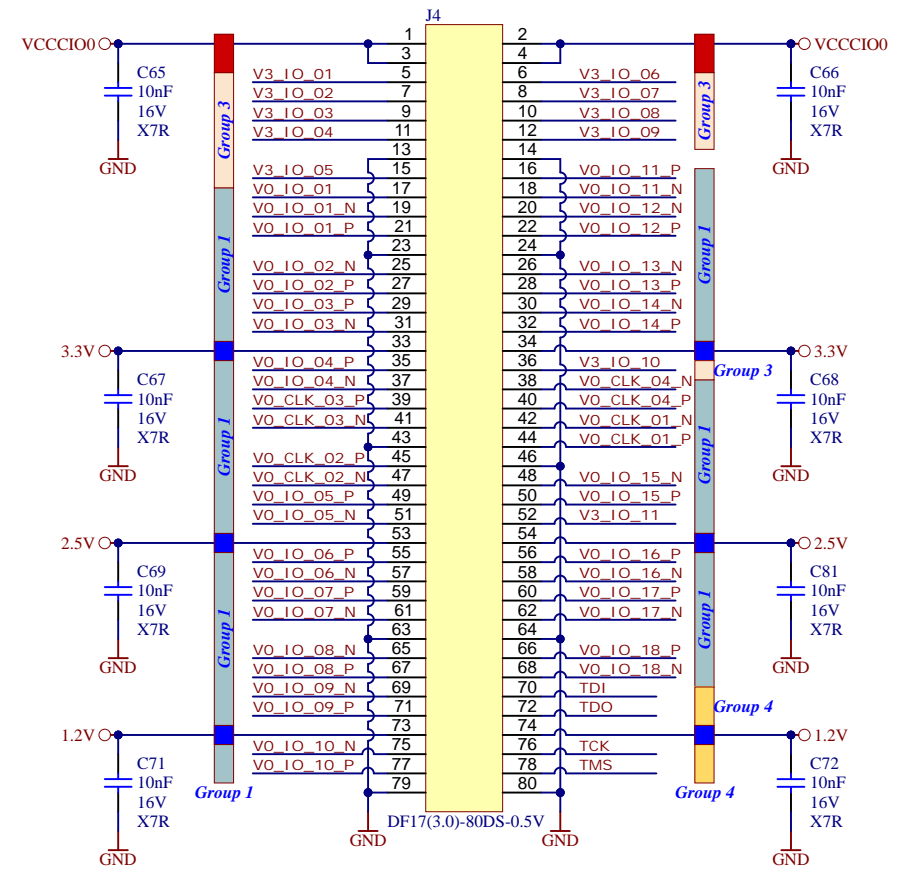
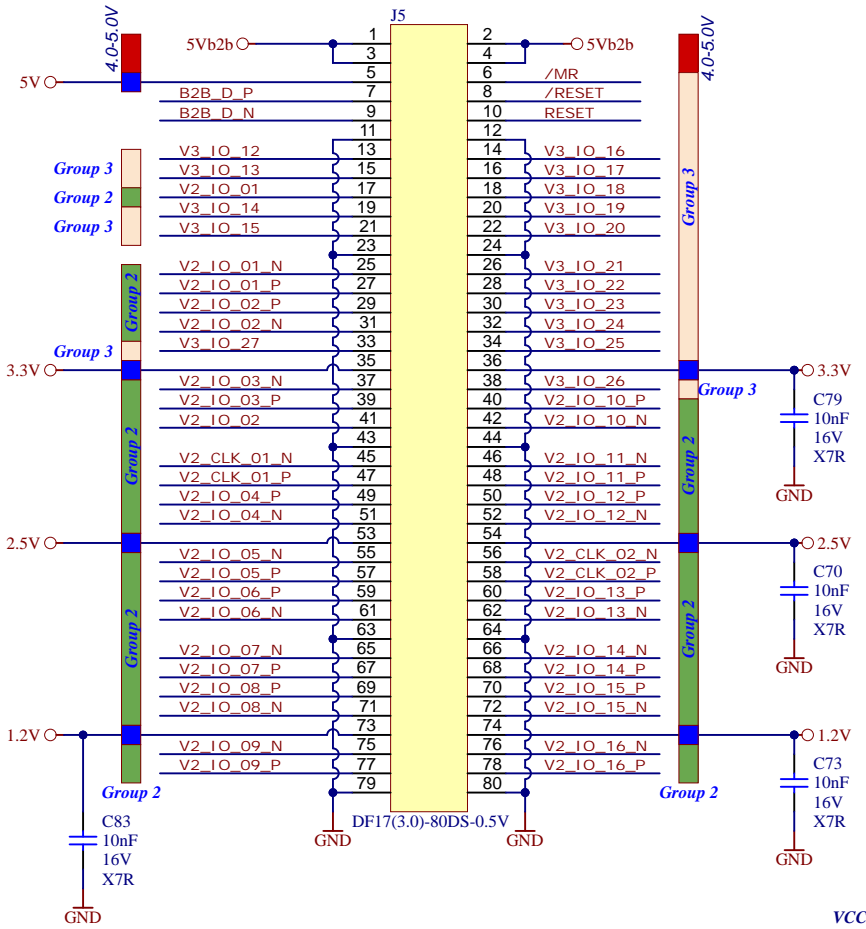
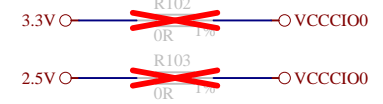
Assembly variant	63122-A
Created by	MT
Modified by	MT
Modified at	2023-06-22



Title: TE0630		
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B2 38 IOs 3.3V, 18 LVDS Pairs
B3 16 IOs 3.3V

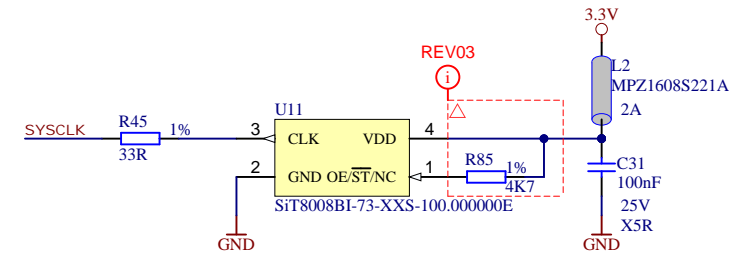
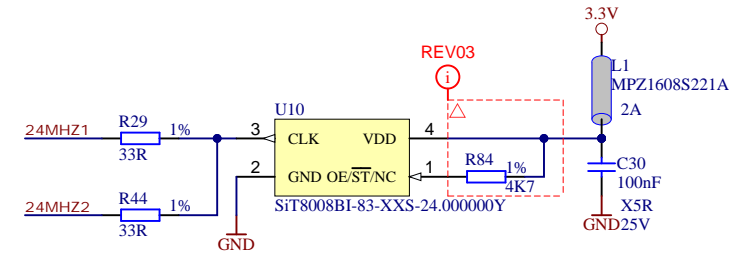
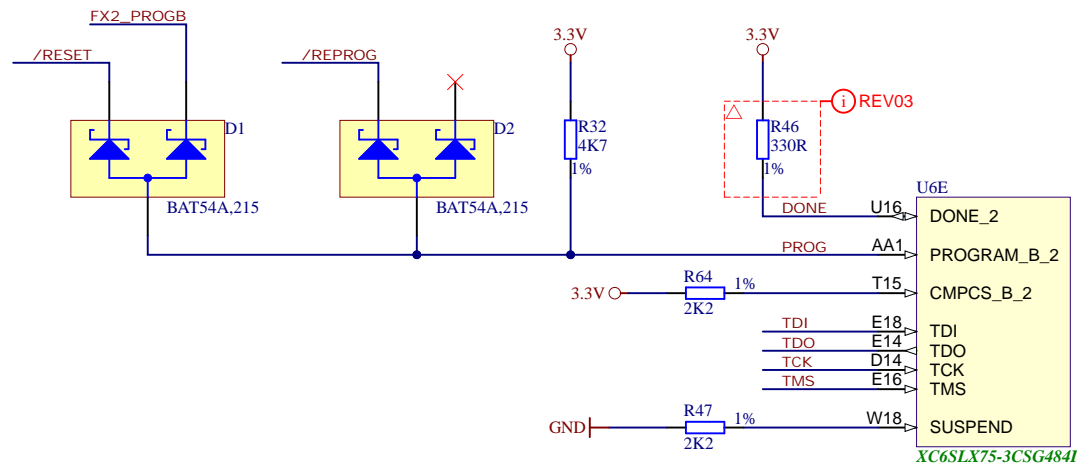
B0 45 IOs VCCIO0, 22 LVDS Pairs
B3 11 IOs 3.3V



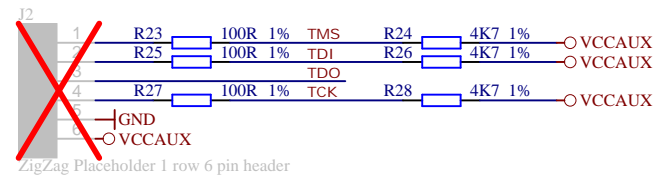
- VCCIO0 1.1..3.45V
- VCCIO2 3.3V
- VCCIO3 3.3V
- VCCAUX 2.5V
- Group 1 0..VCCIO0
- Group 2 0..VCCIO2
- Group 3 0..VCCIO3
- Group 4 0..VCCAUX
- PWR in
- PWR out




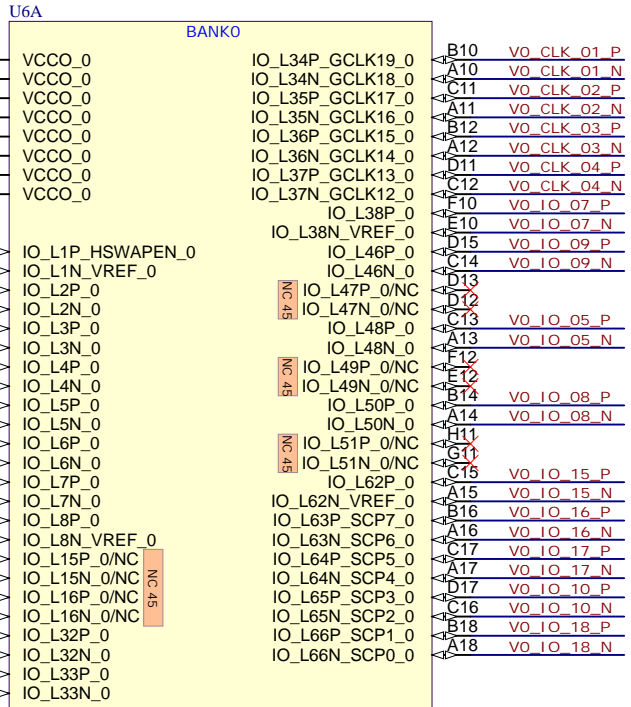
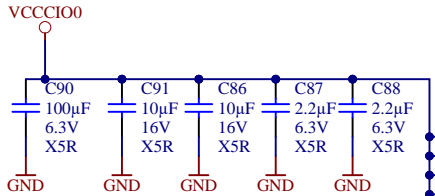
Title: TE0630 - B2B_Connectors		
A4	Number: TE0630 63I22-A	Rev. 03
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- 24MHZ1 TP22 Testpoint 0.8mm
- 24MHZ2 TP23 Testpoint 0.8mm
- SYSCLK TP24 Testpoint 0.8mm
- PROG TP29 Testpoint 0.8mm

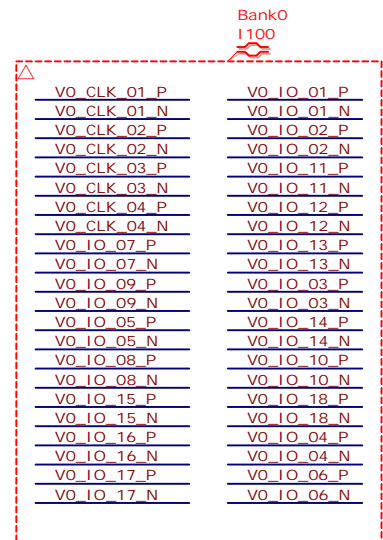


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HSWAP = high --> No configuration pullups
 HSWAP = low: R49 DNP, R70 populated

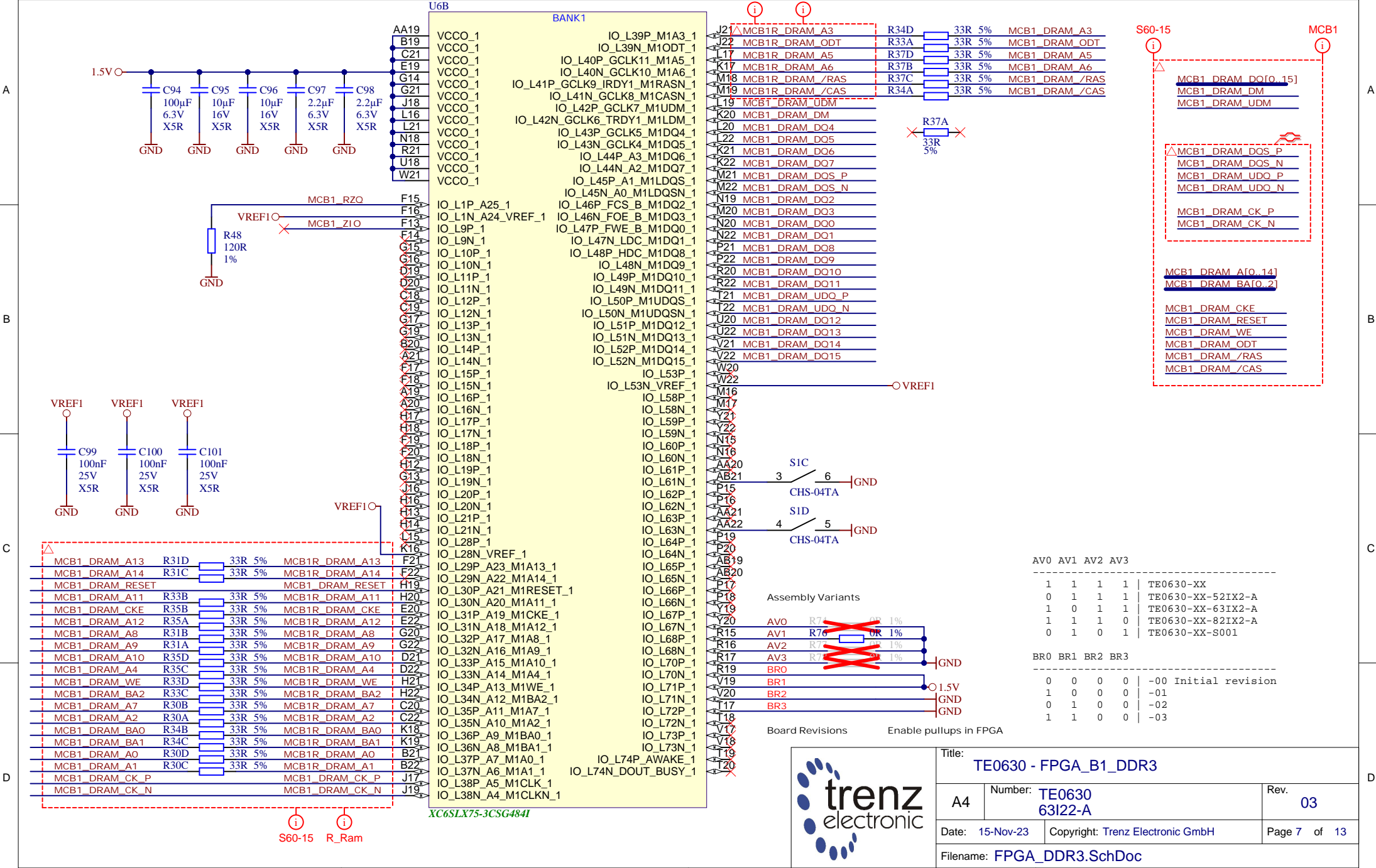
HSWAP = high: R49 populated, R70 DNP
 HSWAP = low: R49 DNP, R70 populated



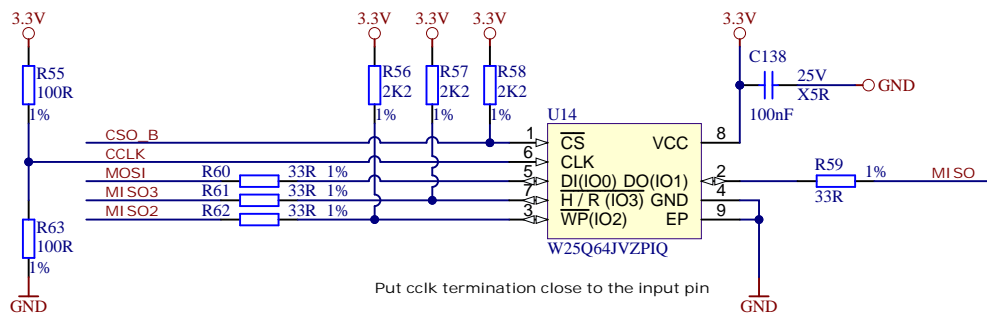
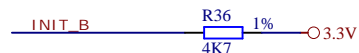
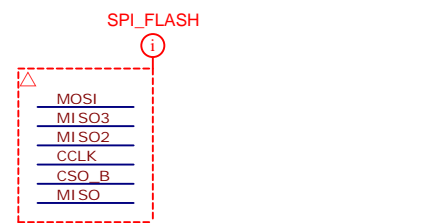
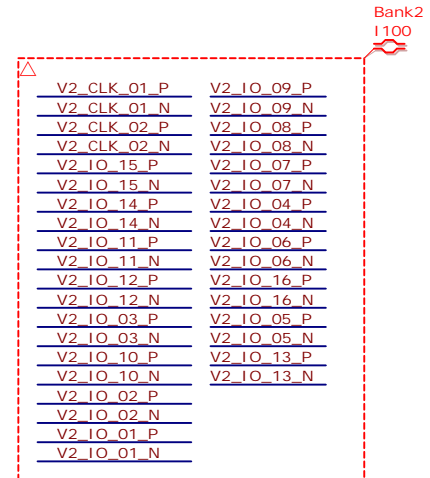
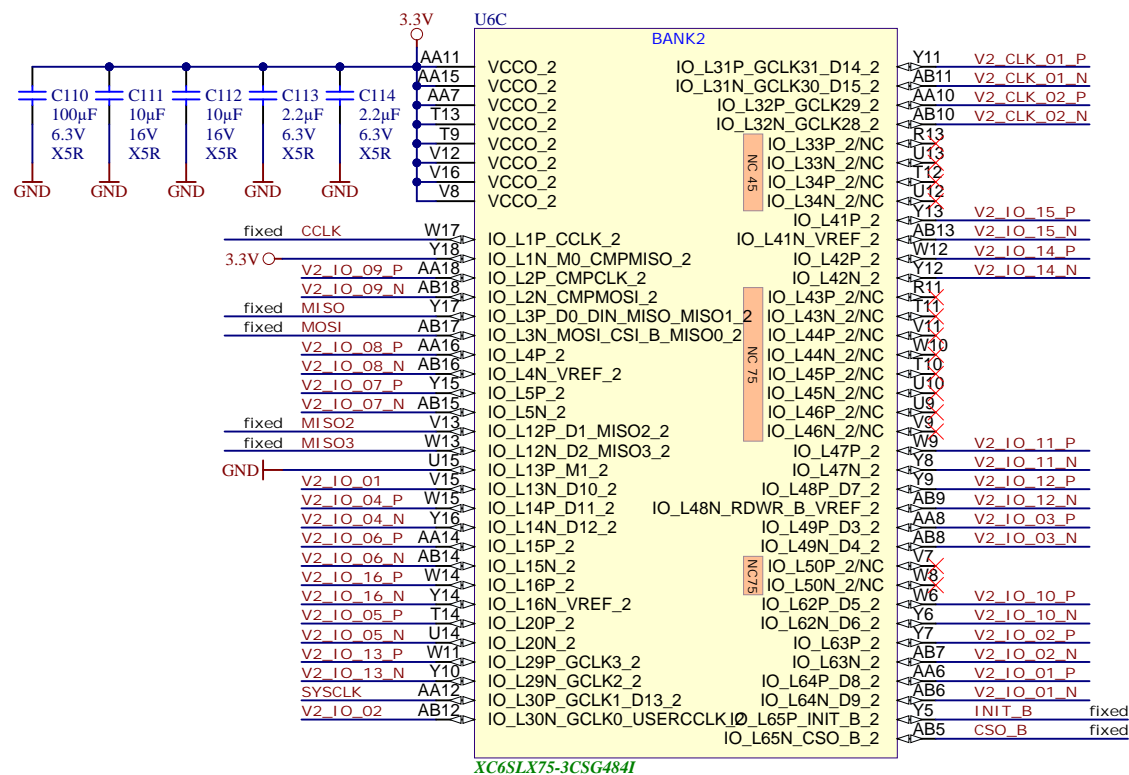
XC6SLX75-3CSG484I



Title: TE0630 - FPGA_B0		
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Title: TE0630 - FPGA_B1_DDR3		
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CSO_B TP16 Testpoint 0.8mm
MOSI TP18 Testpoint 0.8mm



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A

A

B

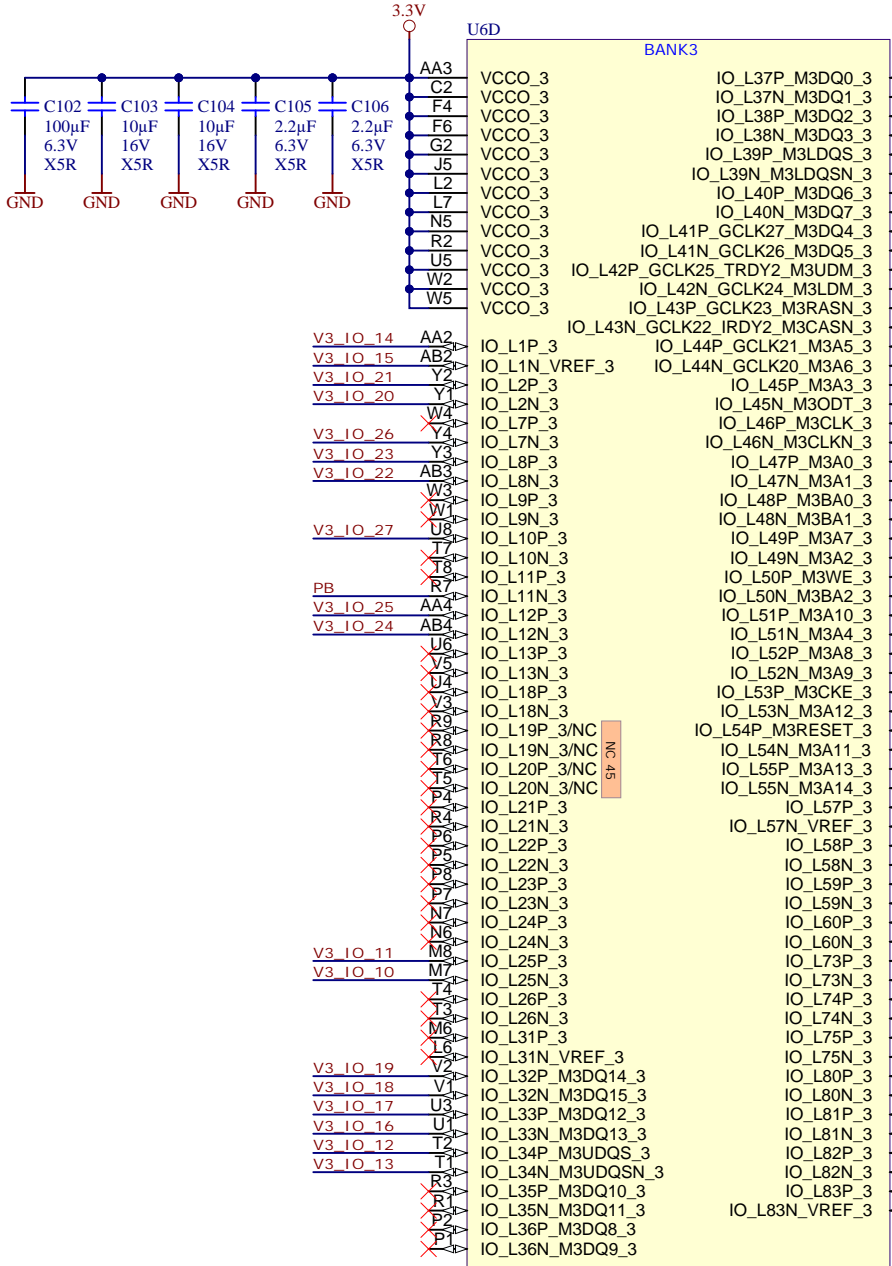
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C

D

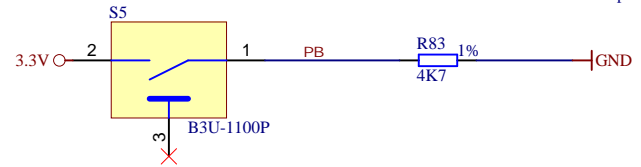
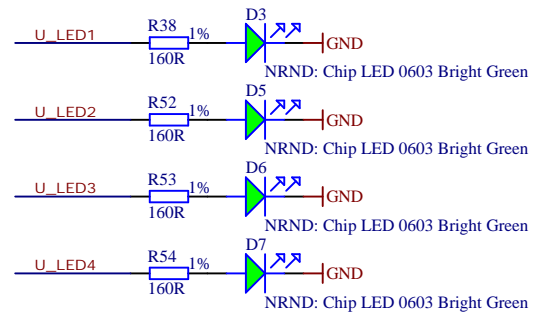
D



AA3	VCCO_3	IO_L37P_M3DQ0_3	N3
C2	VCCO_3	IO_L37N_M3DQ1_3	N1
F4	VCCO_3	IO_L38P_M3DQ2_3	M2
F6	VCCO_3	IO_L38N_M3DQ3_3	M1
G2	VCCO_3	IO_L39P_M3LDQS_3	L3
J5	VCCO_3	IO_L39N_M3LDQSN_3	L1
L2	VCCO_3	IO_L40P_M3DQ6_3	K1
L7	VCCO_3	IO_L40N_M3DQ7_3	K2
N5	VCCO_3	IO_L41P_GCLK27_M3DQ4_3	J3
R2	VCCO_3	IO_L41N_GCLK26_M3DQ5_3	J1
U5	VCCO_3	IO_L42P_GCLK25_TRDY2_M3UDM_3	H2
W2	VCCO_3	IO_L42N_GCLK24_M3LDM_3	H1
W5	VCCO_3	IO_L43P_GCLK23_M3RASN_3	N4
		IO_L43N_GCLK22_IRDY2_M3CASN_3	P3
V3_IO_14	AA2	IO_L1P_3	G3
V3_IO_15	AB2	IO_L1N_VREF_3	G1
V3_IO_21	Y2	IO_L2P_3	M4
V3_IO_20	Y1	IO_L2N_3	M3
		IO_L2P_3	M3
		IO_L2N_3	M3
V3_IO_26	W4	IO_L7P_3	F2
V3_IO_23	Y3	IO_L7N_3	F1
V3_IO_22	AB3	IO_L8P_3	M5
		IO_L8N_3	M5
		IO_L9P_3	L4
		IO_L9N_3	L4
V3_IO_27	W3	IO_L10P_3	E3
		IO_L10N_3	E3
		IO_L11P_3	F1
		IO_L11N_3	F1
PB	R7	IO_L12P_3	K4
V3_IO_25	AA4	IO_L12N_3	K3
V3_IO_24	AB4	IO_L13P_3	D2
		IO_L13N_3	D1
		IO_L18P_3	K6
		IO_L18N_3	K6
		IO_L19P_3/NC	C3
		IO_L19N_3/NC	C1
		IO_L20P_3/NC	J6
		IO_L20N_3/NC	J6
		IO_L21P_3	I4
		IO_L21N_3	I4
		IO_L22P_3	B2
		IO_L22N_3	B1
		IO_L23P_3	H4
		IO_L23N_3	H3
		IO_L24P_3	H6
		IO_L24N_3	H5
V3_IO_11	M8	IO_L25P_3	H8
V3_IO_10	M7	IO_L25N_3	H8
		IO_L26P_3	J7
		IO_L26N_3	J7
		IO_L27P_3	K8
		IO_L27N_3	K8
		IO_L28P_3	K7
		IO_L28N_3	K7
		IO_L29P_3	F4
		IO_L29N_3	F4
		IO_L31P_3	F3
		IO_L31N_3	F3
		IO_L32P_M3DQ14_3	G8
V3_IO_19	V2	IO_L32N_M3DQ15_3	G7
V3_IO_18	V1	IO_L33P_M3DQ12_3	G6
V3_IO_17	U3	IO_L33N_M3DQ13_3	G4
V3_IO_16	U1	IO_L34P_M3UDQS_3	F5
V3_IO_12	T2	IO_L34N_M3UDQSN_3	F5
V3_IO_13	T1	IO_L35P_M3DQ10_3	E5
		IO_L35N_M3DQ11_3	E5
		IO_L36P_M3DQ8_3	F8
		IO_L36N_M3DQ9_3	F8
		IO_L37N_VREF_3	F7
		IO_L38N_VREF_3	F7
		IO_L80P_3	C4
		IO_L80N_3	C4
		IO_L81P_3	D3
		IO_L81N_3	D3
		IO_L82P_3	E6
		IO_L82N_3	E6
		IO_L83P_3	D5
		IO_L83N_3	D5
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		IO_L83N_VREF_3	A2

XC6SLX75-3CSG484I

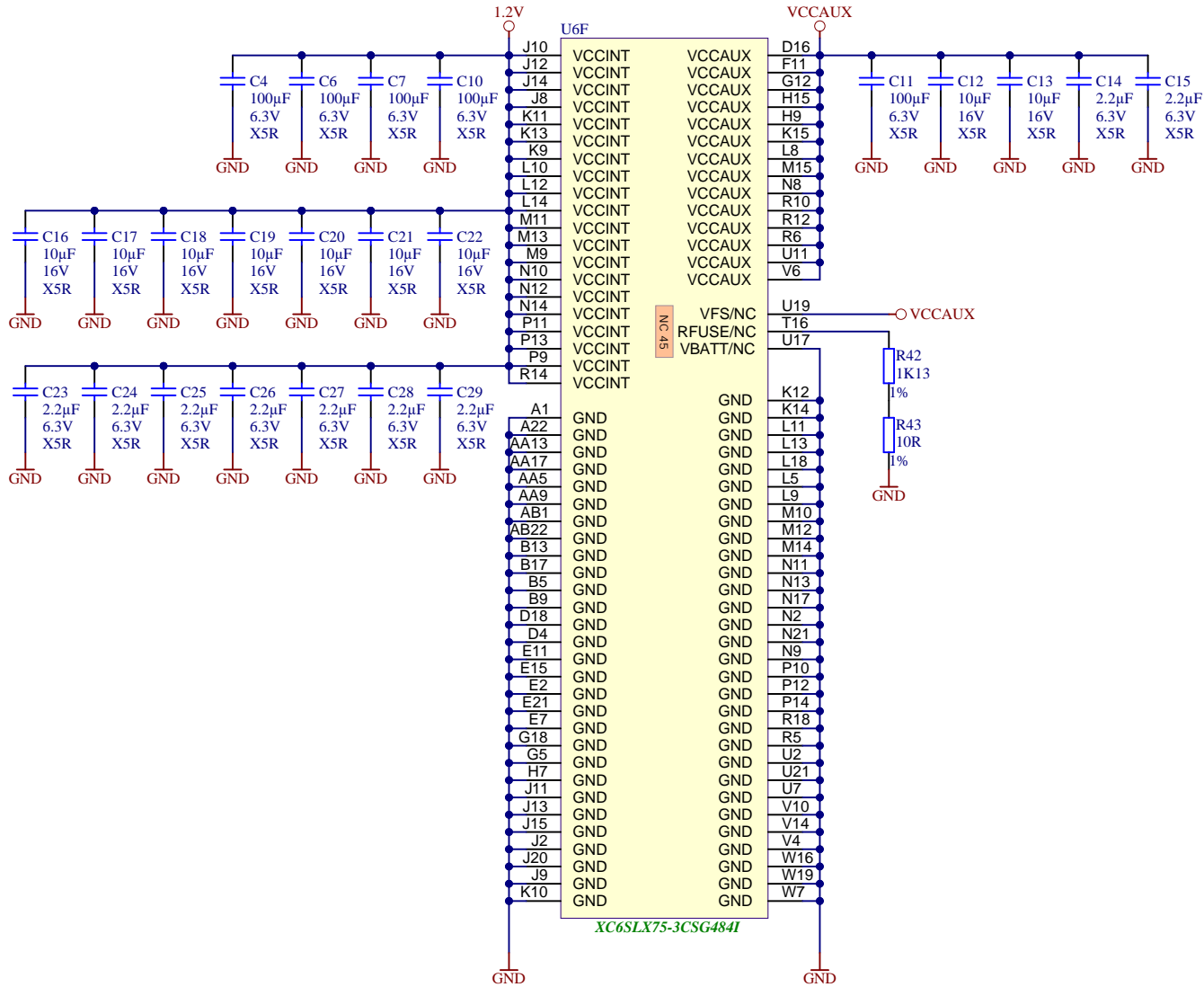
IFCLK	PA0/INT0	V3_IO_01
24MHZ1	PA1/INT1	V3_IO_02
RDY0/SLRD	PA2/SLOE	V3_IO_03
RDY1/SLWR	PA4/FI FOADR0	V3_IO_04
U_LED1	PA5/FI FOADR1	V3_IO_05
U_LED2	PA6/PKTEND	V3_IO_06
U_LED3	SDA	V3_IO_07
U_LED4	SCL	V3_IO_08
CTL0/FLAGA		V3_IO_09
CTL1/FLAGB		V3_IO_10
CTL2/FLAGC		V3_IO_11
FD0		V3_IO_12
FD1		V3_IO_13
FD2		V3_IO_14
FD3		V3_IO_15
FD4		V3_IO_16
FD5		V3_IO_17
FD6		V3_IO_18
FD7		V3_IO_19
/REPROG		V3_IO_20
PA3/WU		V3_IO_21
PB		V3_IO_22
		V3_IO_23
		V3_IO_24
		V3_IO_25
		V3_IO_26




Title: **TE0630 - FPGA_B3**

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		Title: TE0630 - FPGA_PWR	
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A

B

C

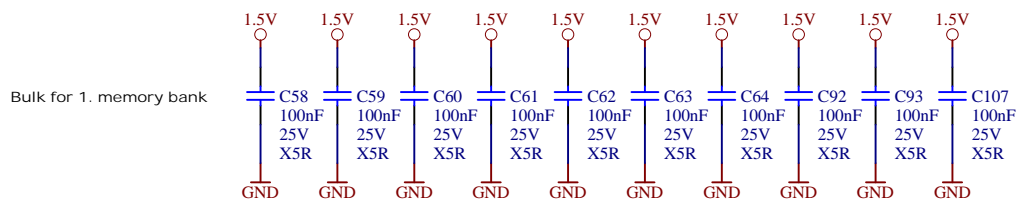
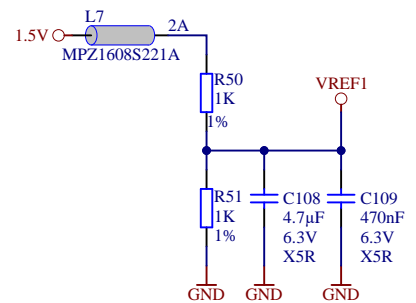
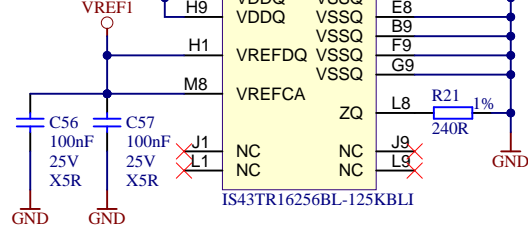
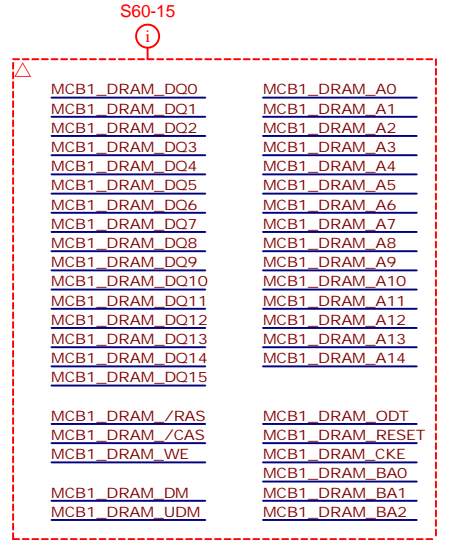
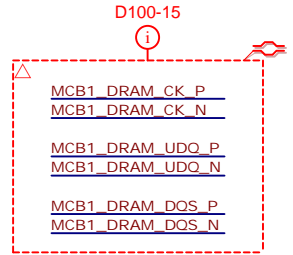
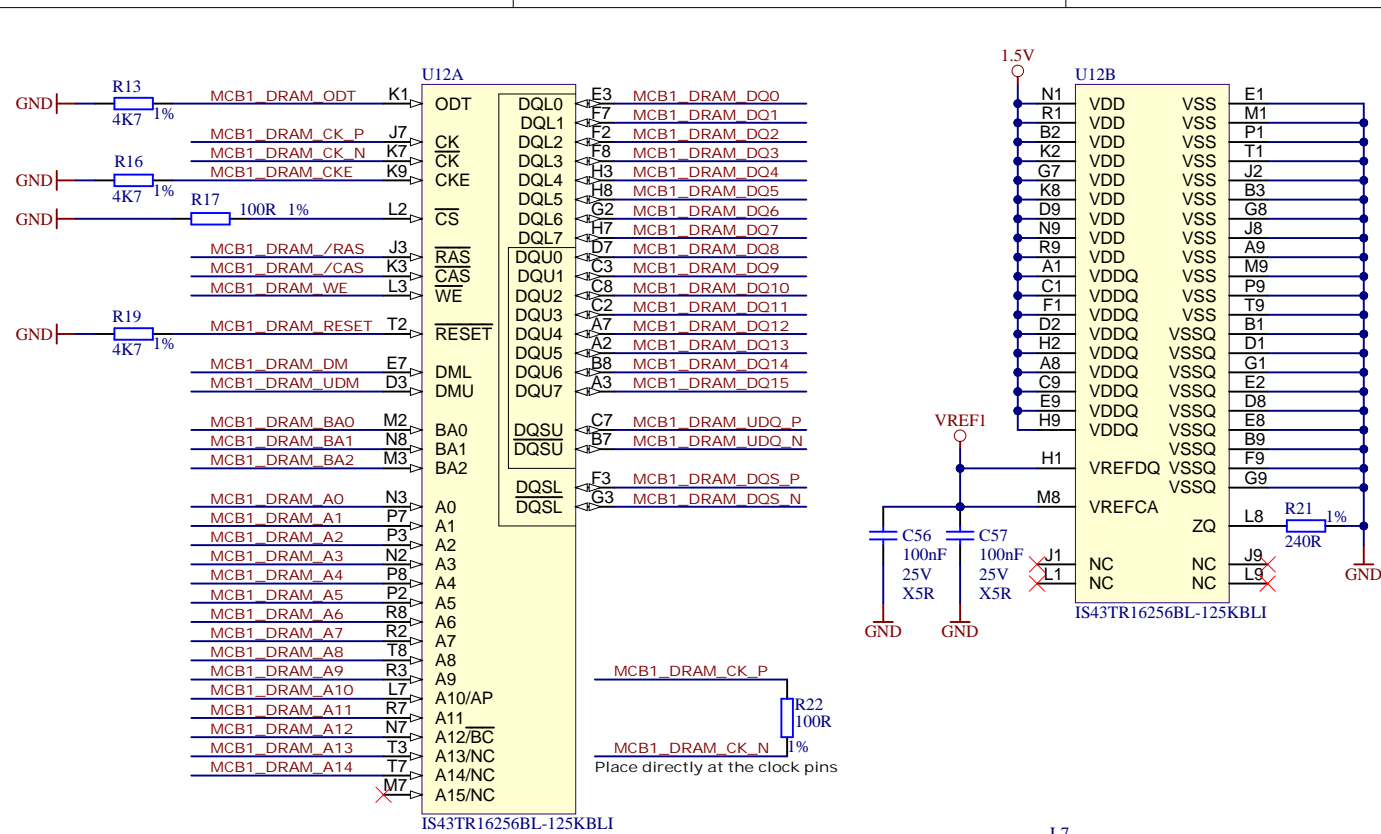
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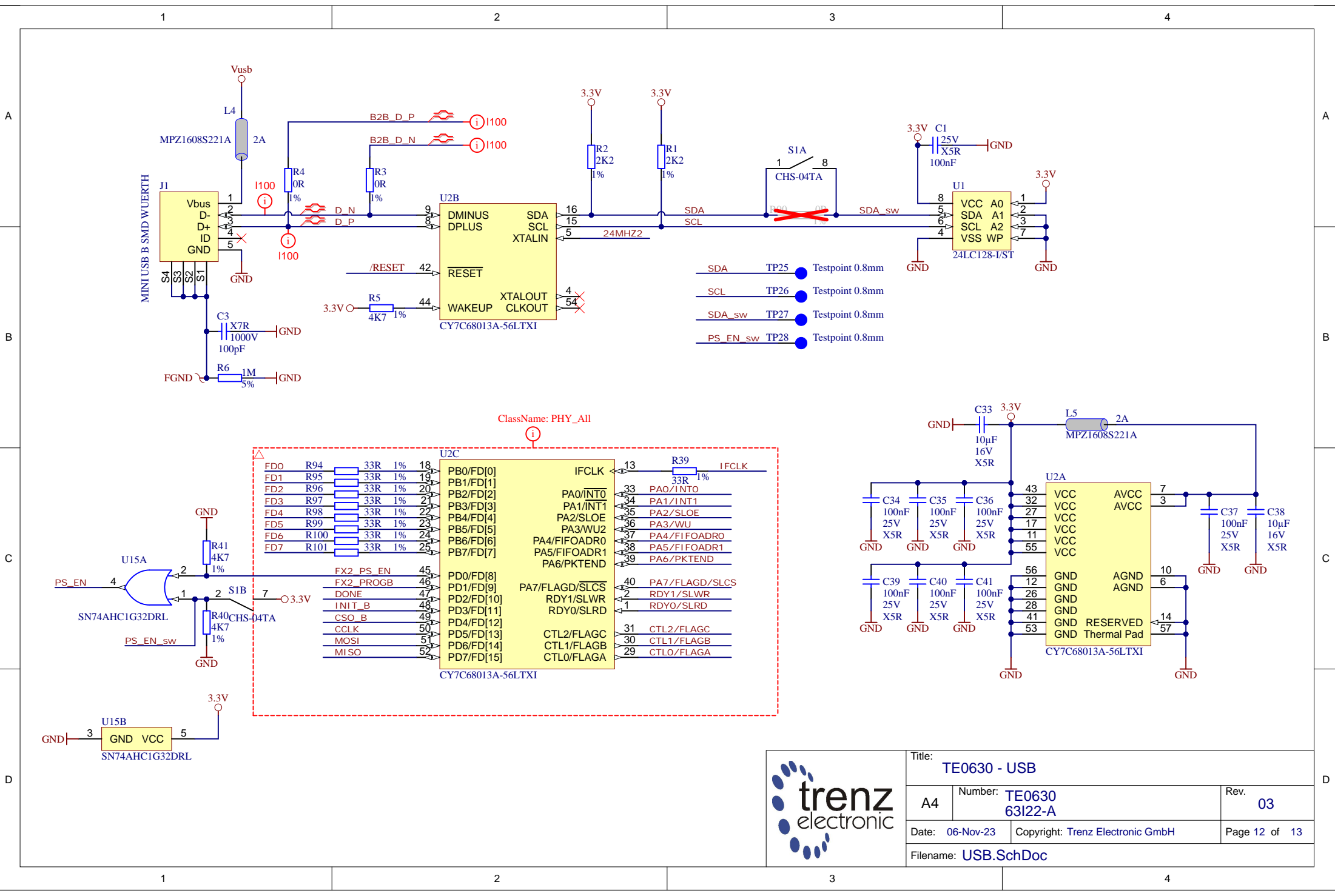
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D



Title: TE0630 - DDR3_RAM		
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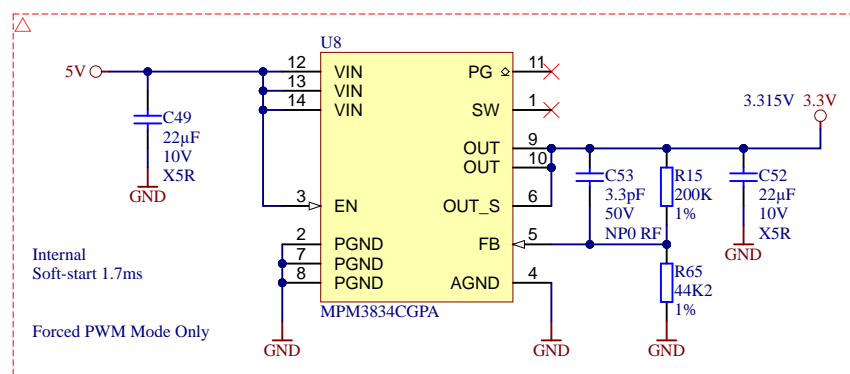


- SDA TP25 Testpoint 0.8mm
- SCL TP26 Testpoint 0.8mm
- SDA_sw TP27 Testpoint 0.8mm
- PS_EN_sw TP28 Testpoint 0.8mm

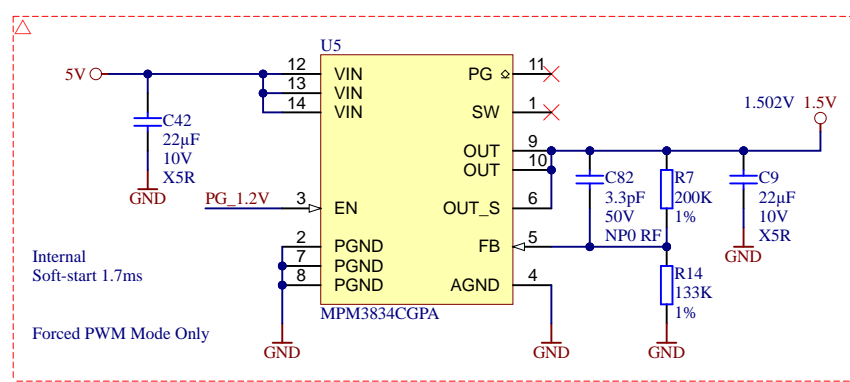
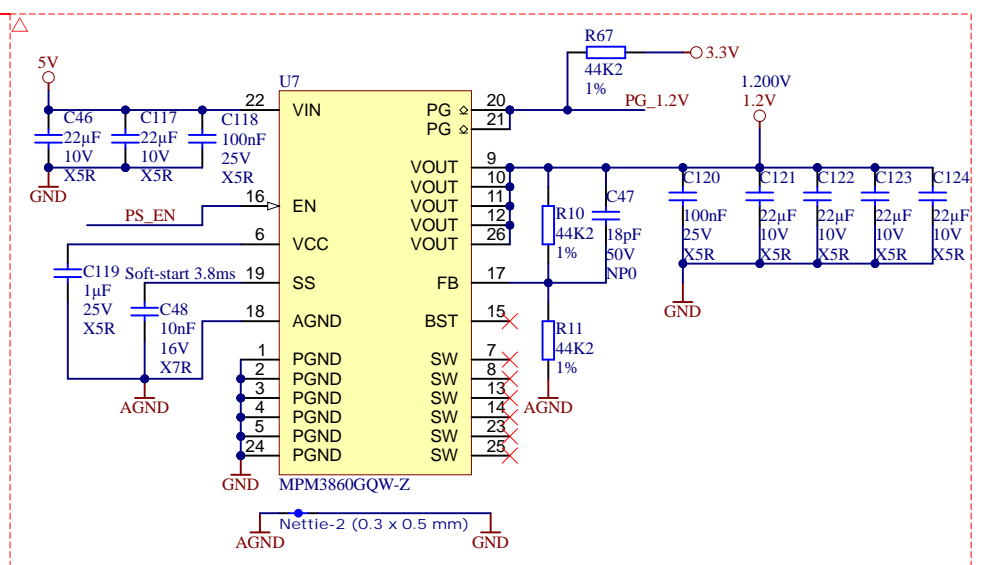
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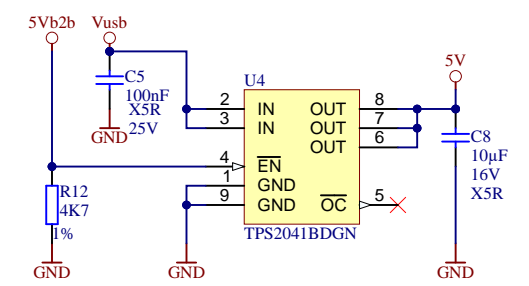
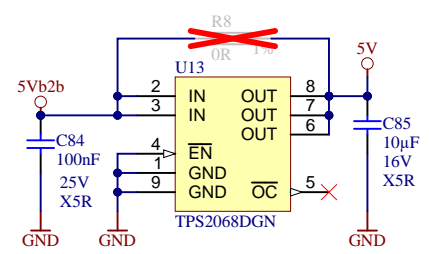
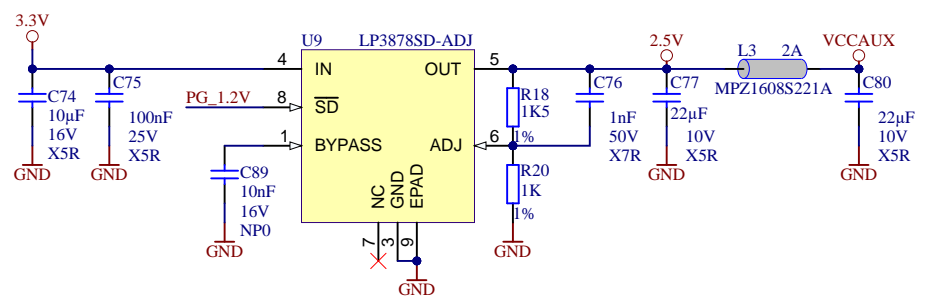
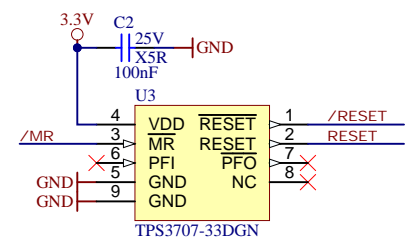
Title: TE0630 - USB		
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REV3



REV3



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