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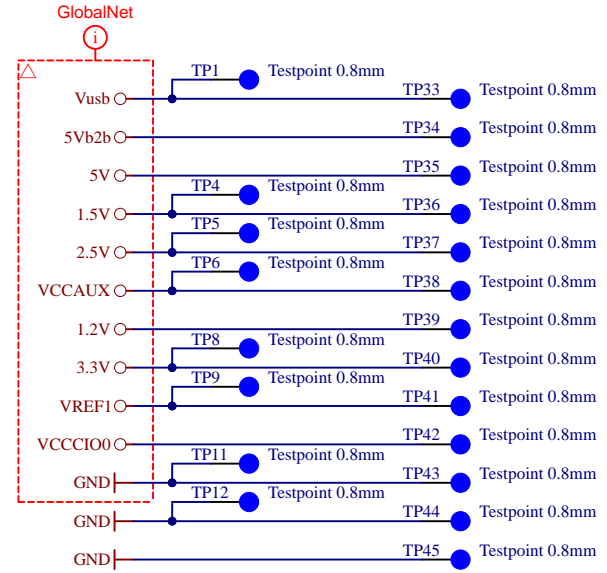
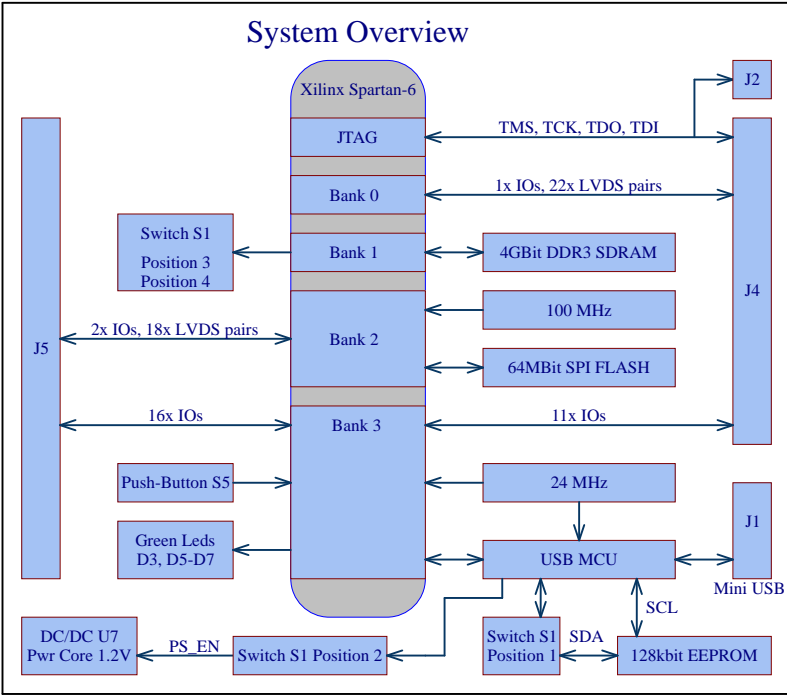
Schematics and other handouts serve for informational purposes only!

	Title: TE0630 - Legal Notices Modules		
	A4	Number: TE0630 82122-A	Rev. 03
	Date: 19-Sep-23	Copyright: Trenz Electronic GmbH	Page 1 of 13
	Filename: Legal_Notices.SchDoc		

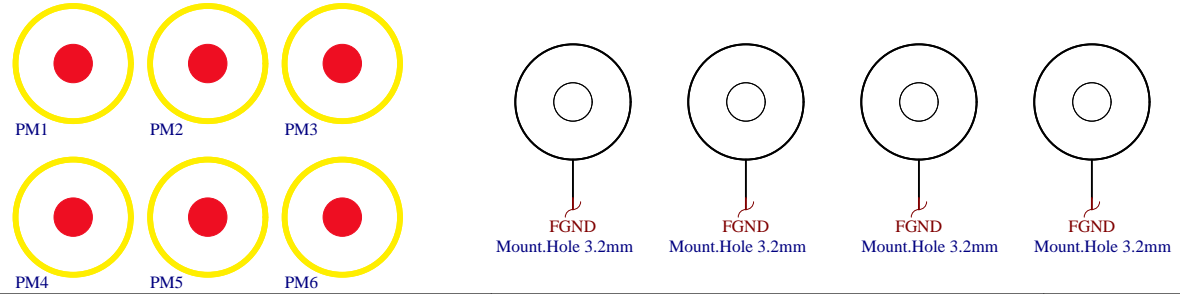
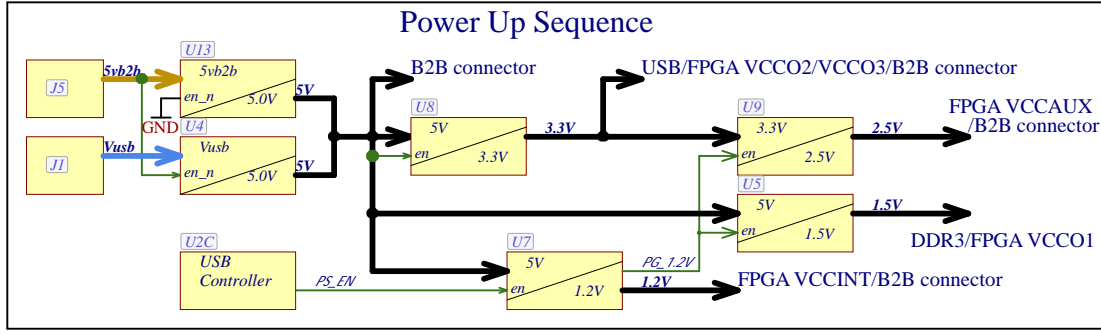
REV	Description	
-01	Initial revision	
-02	<ul style="list-style-type: none"> 1) Replaced U8 by EN6338QI 2) Rerouted nets around U8, results in new track length for: Signal V3_IO_06 15.2475 mm (was 15.0047mm) Signal V3_IO_07 16.0151 mm (was 15.0452 mm) 3) Replaced U5 by EN 6338QI 4) PS_EN now via OR gate 5) Replaced obsolete Diodes D1, D2 D4, by BAT54A 6) Fixed Footprint of U10 according to datasheet 7) Update from LIB 8) Rearranged Testpoints 9) Added Traceability Pad 10) Replaced S5 by smaller PB AN26337 11) Hardware revision coding updated to Rev02 12) Flash change (U14) 2020-03-30 	
-03	<ul style="list-style-type: none"> 1) All sch and pcb components were updated 2) R46 was changed to 330 Ohm 3) "TE0630.SchDoc" page was updated: System Overview was redesigned, Power Up Sequence was added, S/N1 Serialnumber was removed 4) U7 was changed from EN6347QI to MPM3860GQW-Z 5) U8 and U5 were changed from EN6338QI to MPM3834CGPA 6) Added pullups R84 and R85 for ST pin of U10 and U11 on page "FPGA_CFG_CLK.SchDoc" 7) TE logo was changed to UKCA Logo on page "TE0630.SchDoc" 8) "B2B_Connectors.SchDoc" page was updated: service information about IOs pins was added, colored signal groups were added 9) BR0 net was pulled to 1.5V on page "FPGA_DDR3.SchDoc" 10) U12 was changed from NT5CC64M16GP-DII to IS43TR16256BL-125KBLI 11) Assembly option. Pull down resistor R70 was added on page "FPGA_B0.SchDoc" 12) Assembly Variants table was changed on page "FPGA_DDR3.SchDoc": obsolete variants were deleted, new assembly variants were added 13) "Legal_Notices.SchDoc" page was added 14) Parameters of some capacitors were changed: C77 , C80 : 6.3V -> 10V 15) Fiducials PM1-PM6 were updated and moved for same positions on top and bottom layers 16) Removed testpoints TP2,TP3,TP7,TP10,TP13,TP14,TP15,TP17, TP19,TP20,TP21, TP27,TP28,TP30,TP31,TP32 17) Added testpoints TP27 and TP28 on page "USB.SchDoc" 18) Some net classes names were deleted: "MatchLendht150Mil", "MatchLendht300Mil", "Clear_10mil", "S50-33" 19) Net class "3Bank2Half" was renamed to "Bank3" 	MT

	Title: TE0630 - Changes list		
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	Filename: Revision_Changes.SchDoc		

- U_Power
Power.SchDoc
- U_FPGA_PWR
FPGA_PWR.SchDoc
- UKCA
UKCA Logo on Top Overlay
- UKCA-TOOVERLAY
- Serial
Serialnumber 6,3 x 6.3mm



Special notes:



BR0	BR1	BR2	BR3	See BR nets on page "FPGA_DDR3.SchDoc"
0	0	0	0	-00 Initial revision
1	0	0	0	-01
0	1	0	0	-02
1	1	0	0	-03

Assembly variant	82122-A
Created by	MT
Modified by	MT
Modified at	2023-06-22

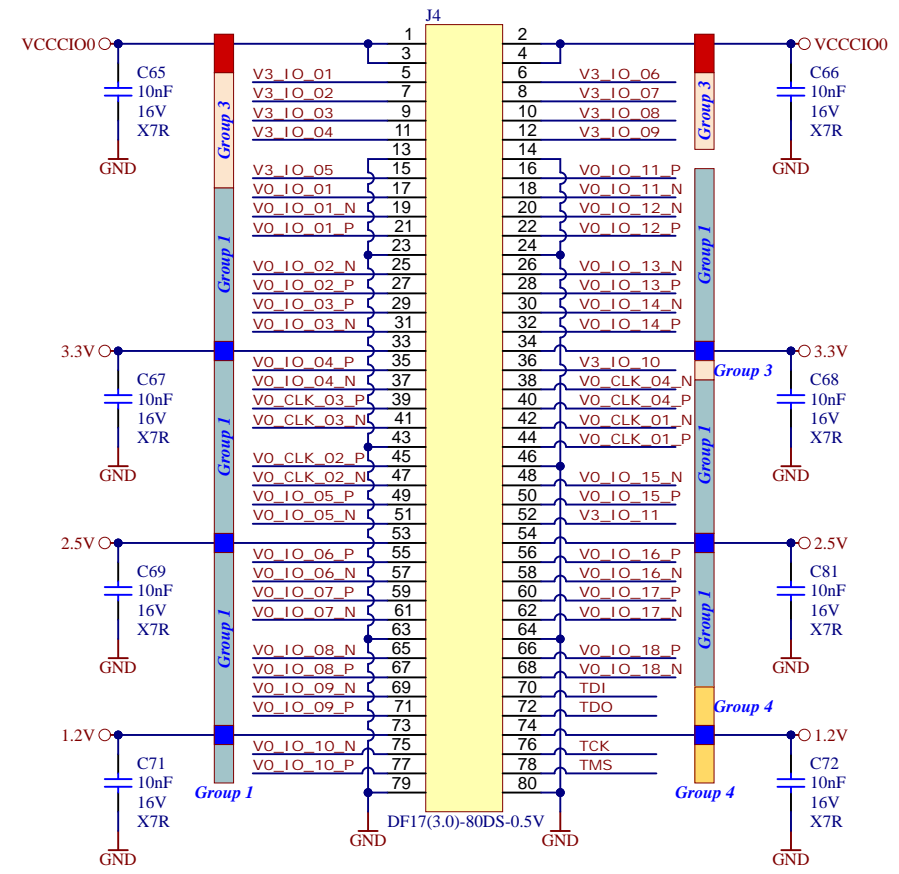
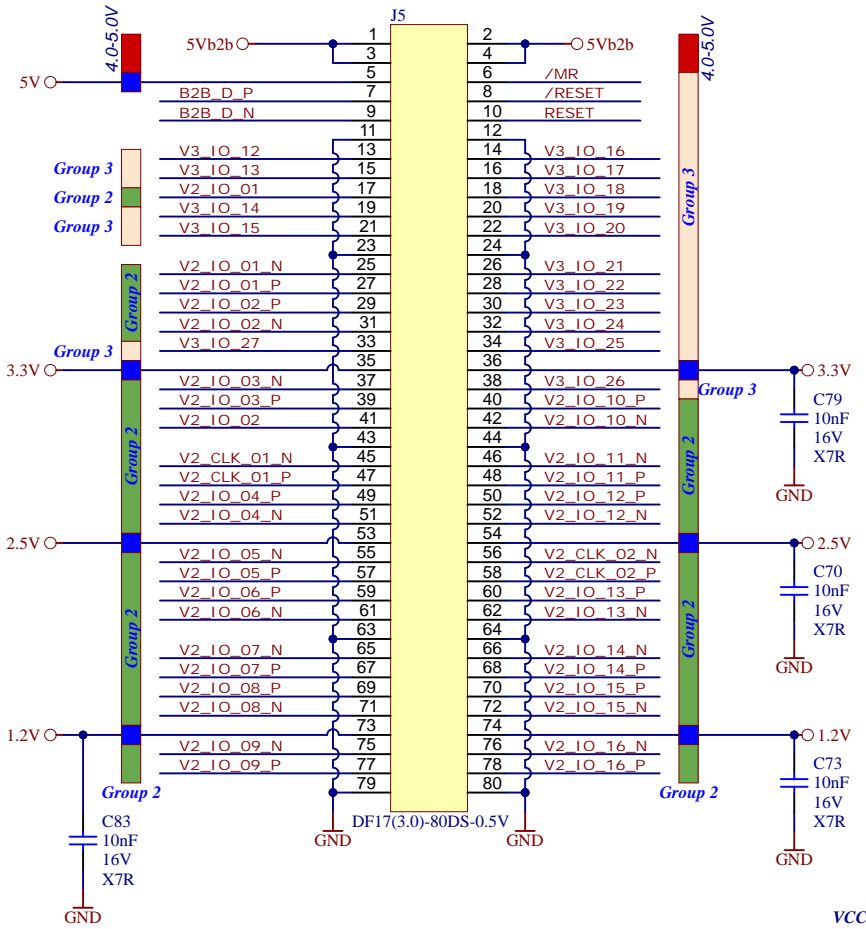
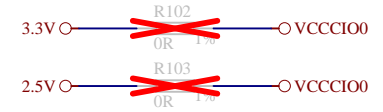
Title: **TE0630**

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Filename: **TE0630.SchDoc**

B2 38 IOs 3.3V, 18 LVDS Pairs
B3 16 IOs 3.3V

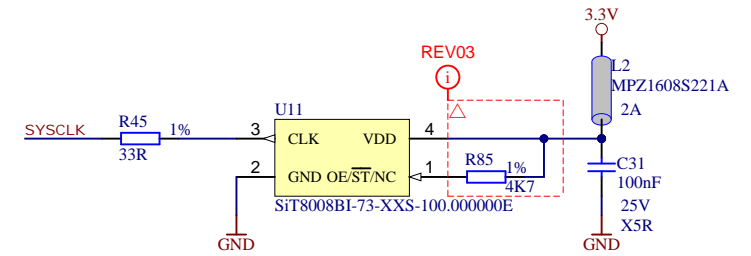
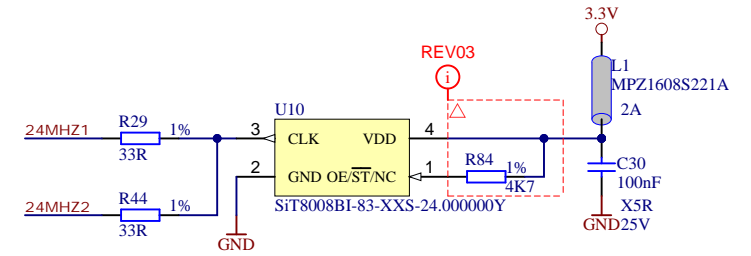
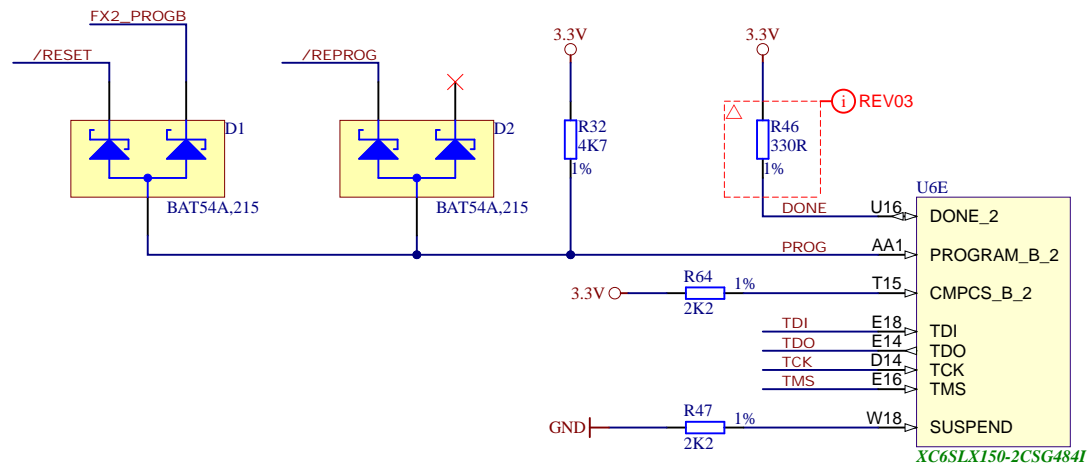
B0 45 IOs VCCIO0, 22 LVDS Pairs
B3 11 IOs 3.3V



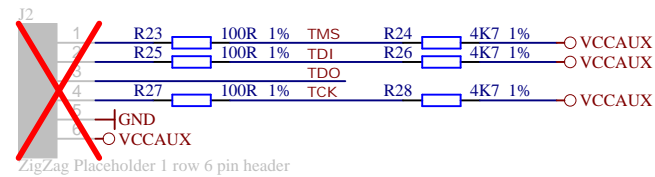
- VCCIO0 1.1..3.45V
- VCCIO2 3.3V
- VCCIO3 3.3V
- VCCAUX 2.5V
- Group 1 0..VCCIO0
- Group 2 0..VCCIO2
- Group 3 0..VCCIO3
- Group 4 0..VCCAUX
- PWR in
- PWR out




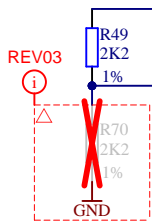
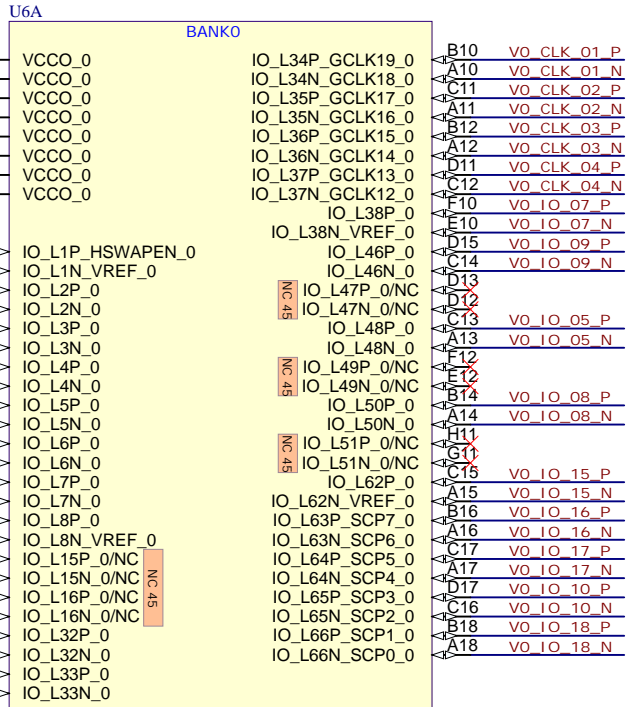
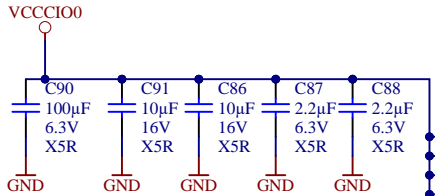
Title: TE0630 - B2B_Connectors		
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- 24MHZ1 TP22 Testpoint 0.8mm
- 24MHZ2 TP23 Testpoint 0.8mm
- SYSCLK TP24 Testpoint 0.8mm
- PROG TP29 Testpoint 0.8mm



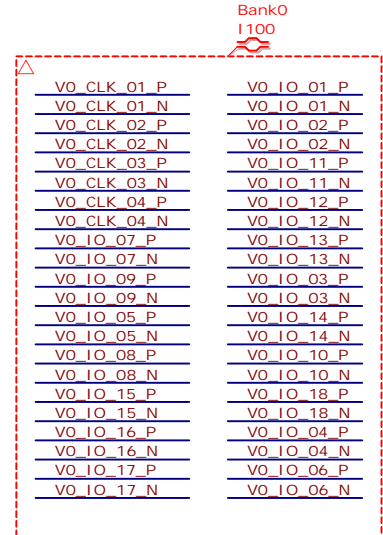
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		A4	Number: TE0630 82122-A
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Filename: FPGA_CFG_CLK.SchDoc			



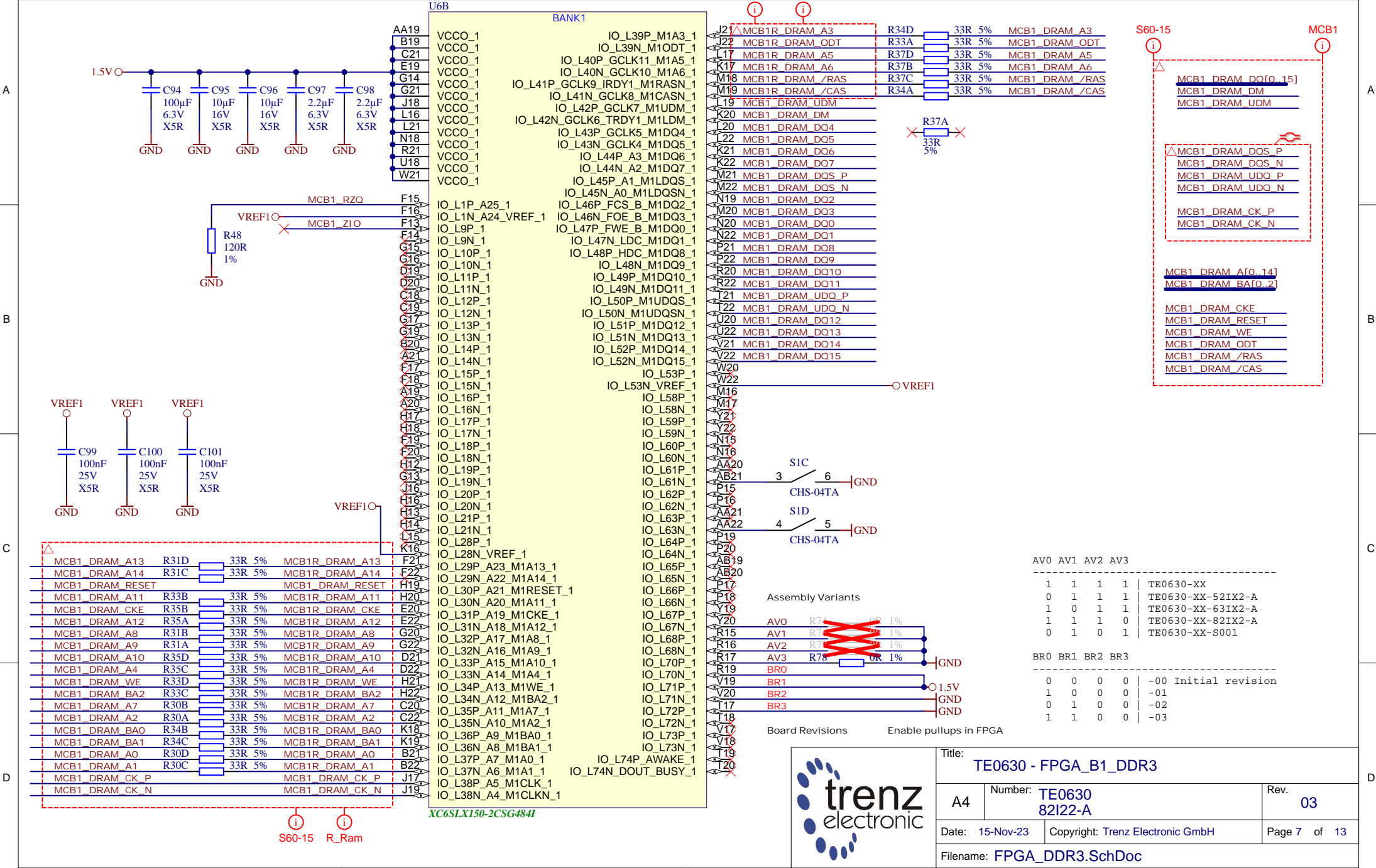
HSWAP = high --> No configuration pullups

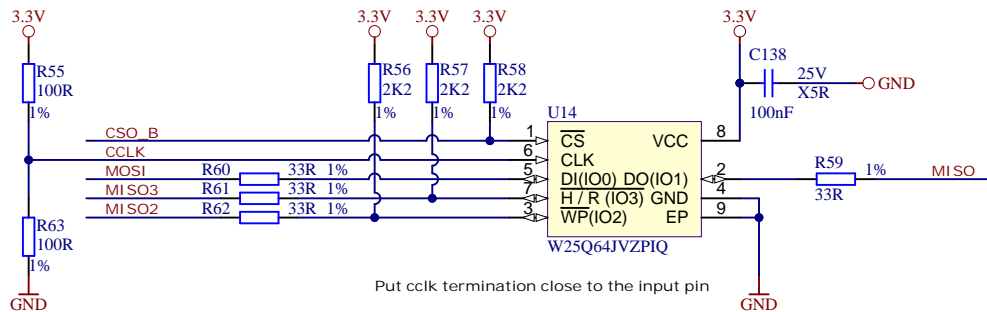
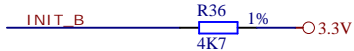
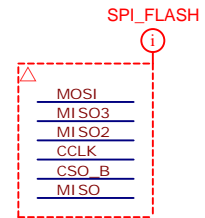
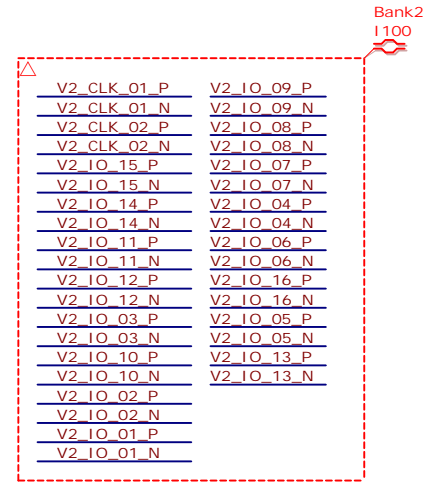
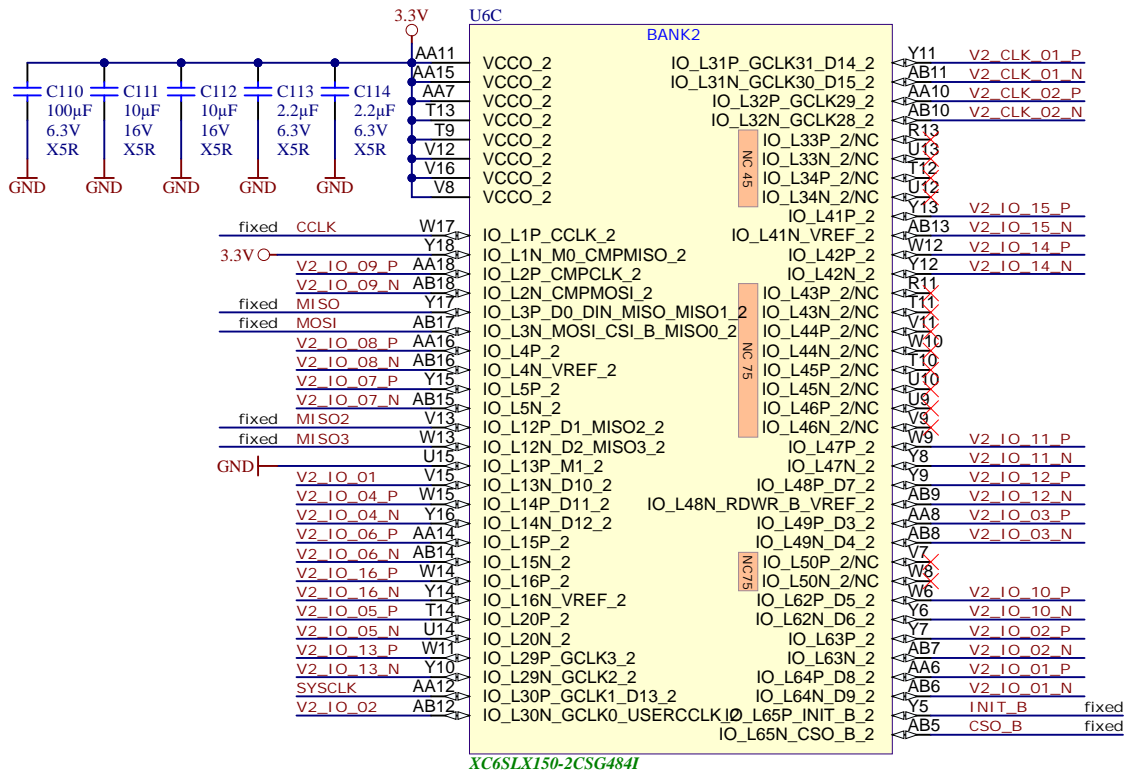
HSWAP = high: R49 populated, R70 DNP
 HSWAP = low: R49 DNP, R70 populated

XC6SLX150-2CSG484I



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Filename: FPGA_B0.SchDoc		

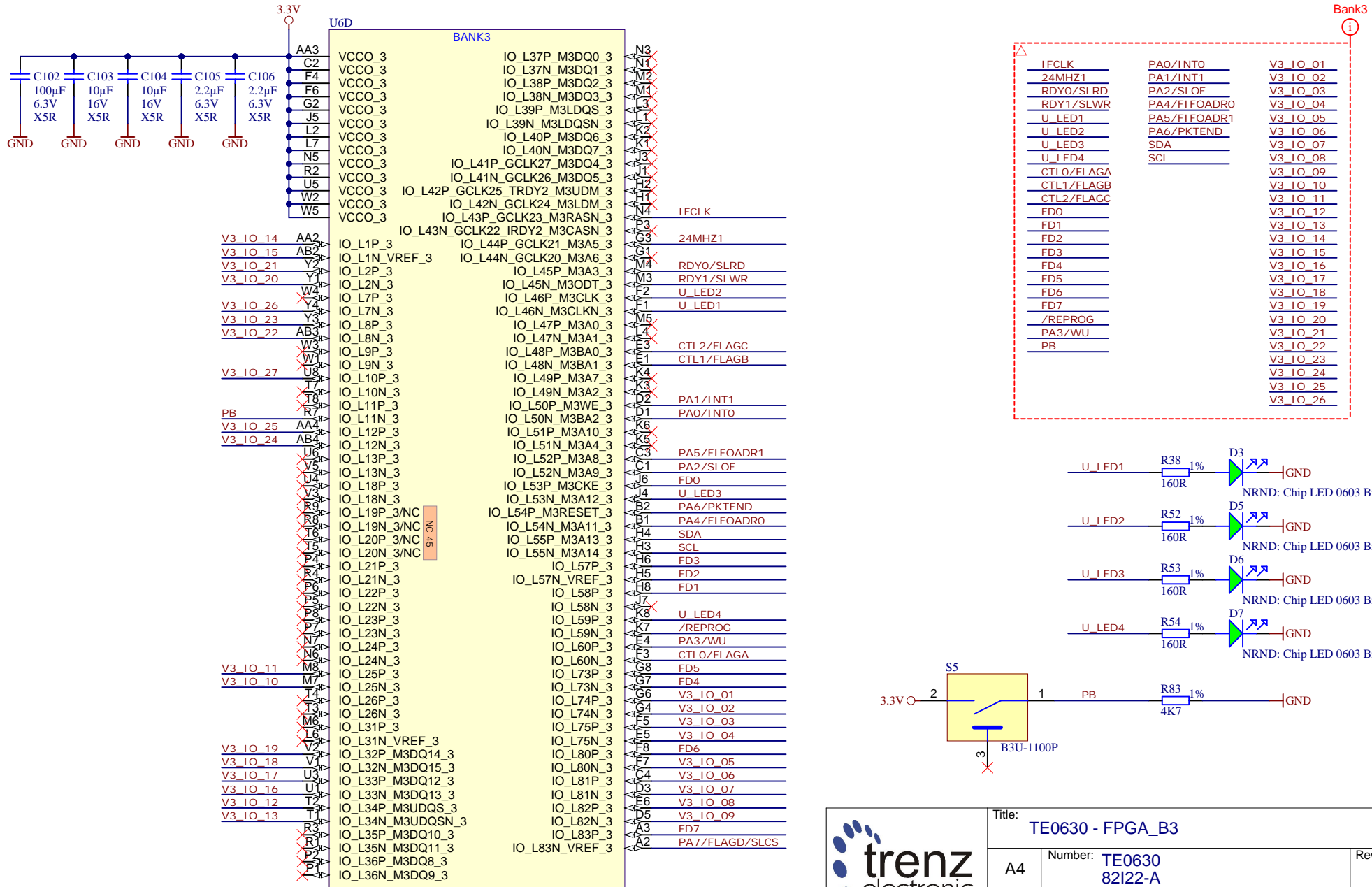




CSO_B TP16 Testpoint 0.8mm
MOSI TP18 Testpoint 0.8mm



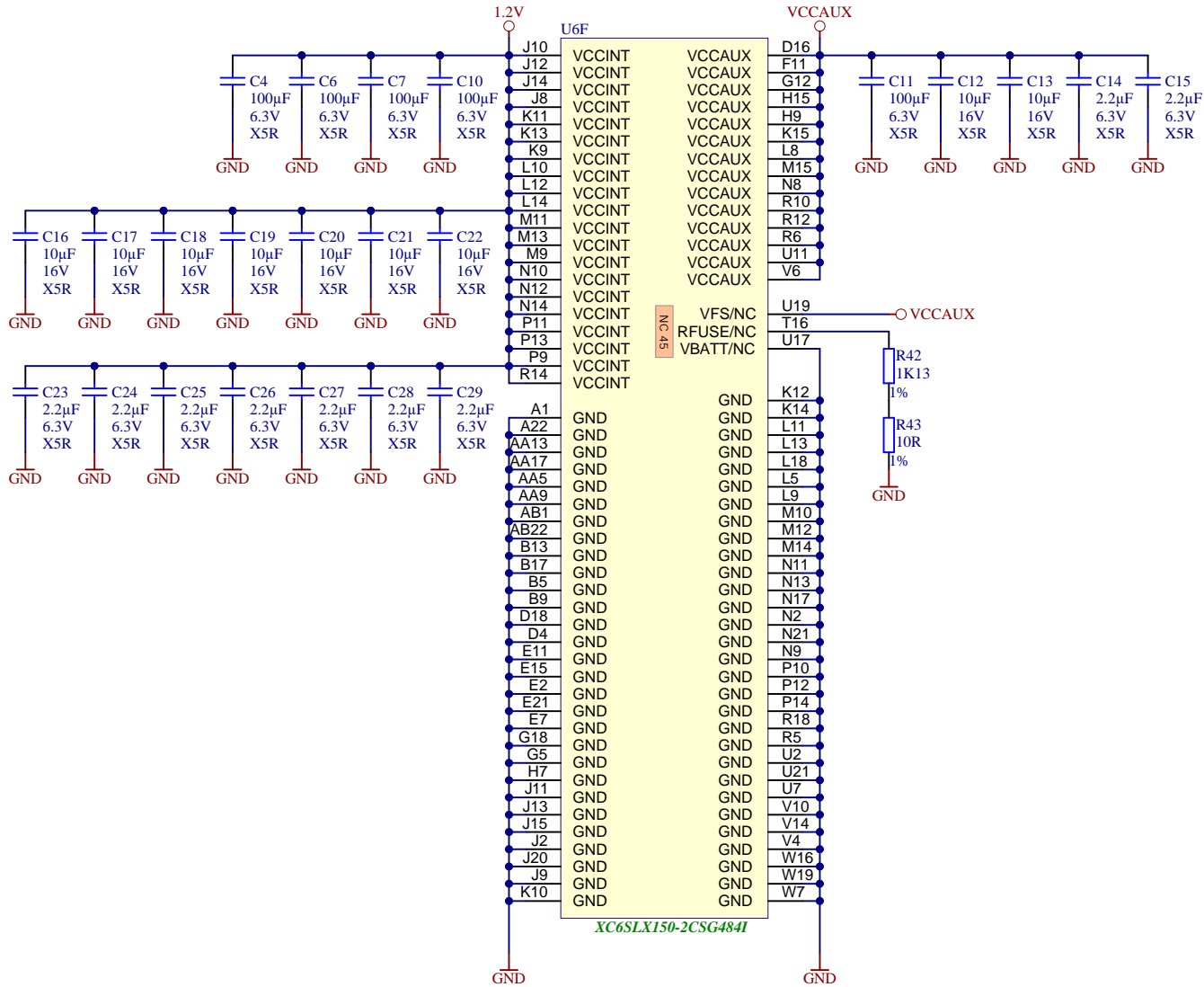
Title: TE0630 - FPGA_B2		
A4	Number: TE0630 82I22-A	Rev. 03
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Filename: FPGA_B2.SchDoc		




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Title: **TE0630 - FPGA_B3**

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XC6SLX150-2CSG484I

	Title: TE0630 - FPGA_PWR	
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Filename: FPGA_PWR.SchDoc		

A

B

C

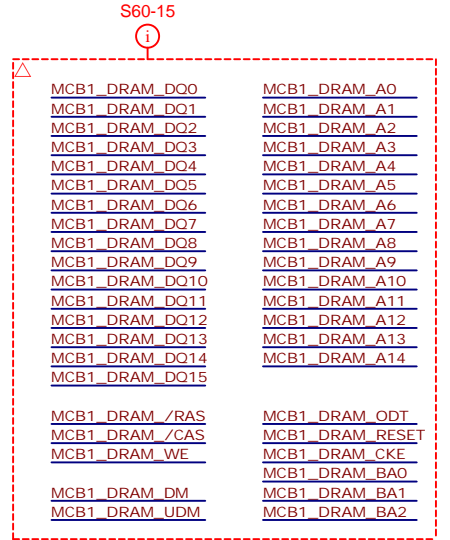
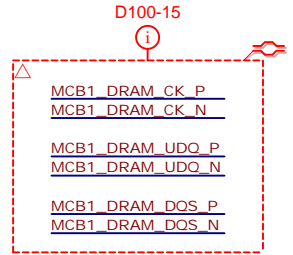
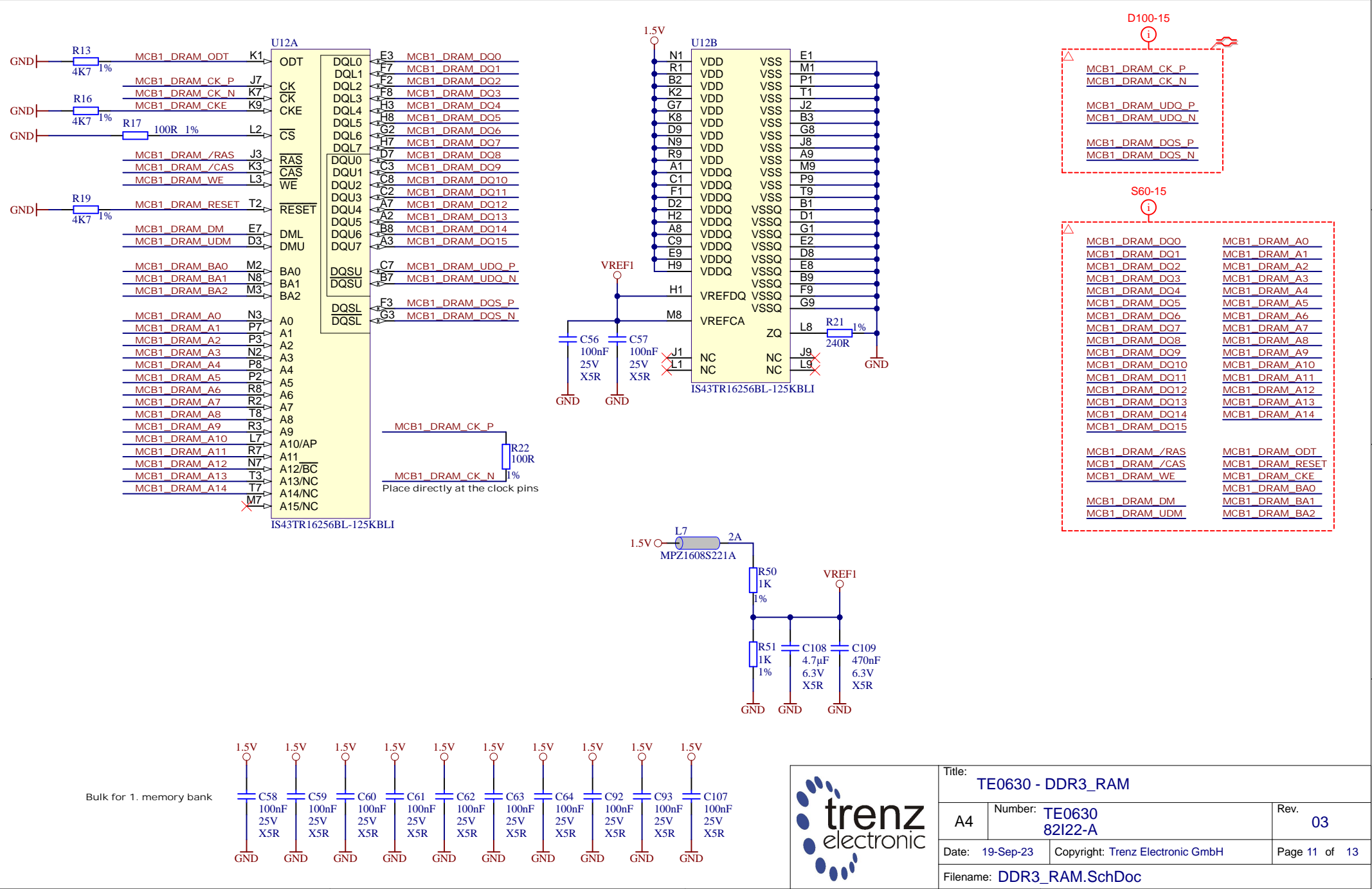
D

A

B

C

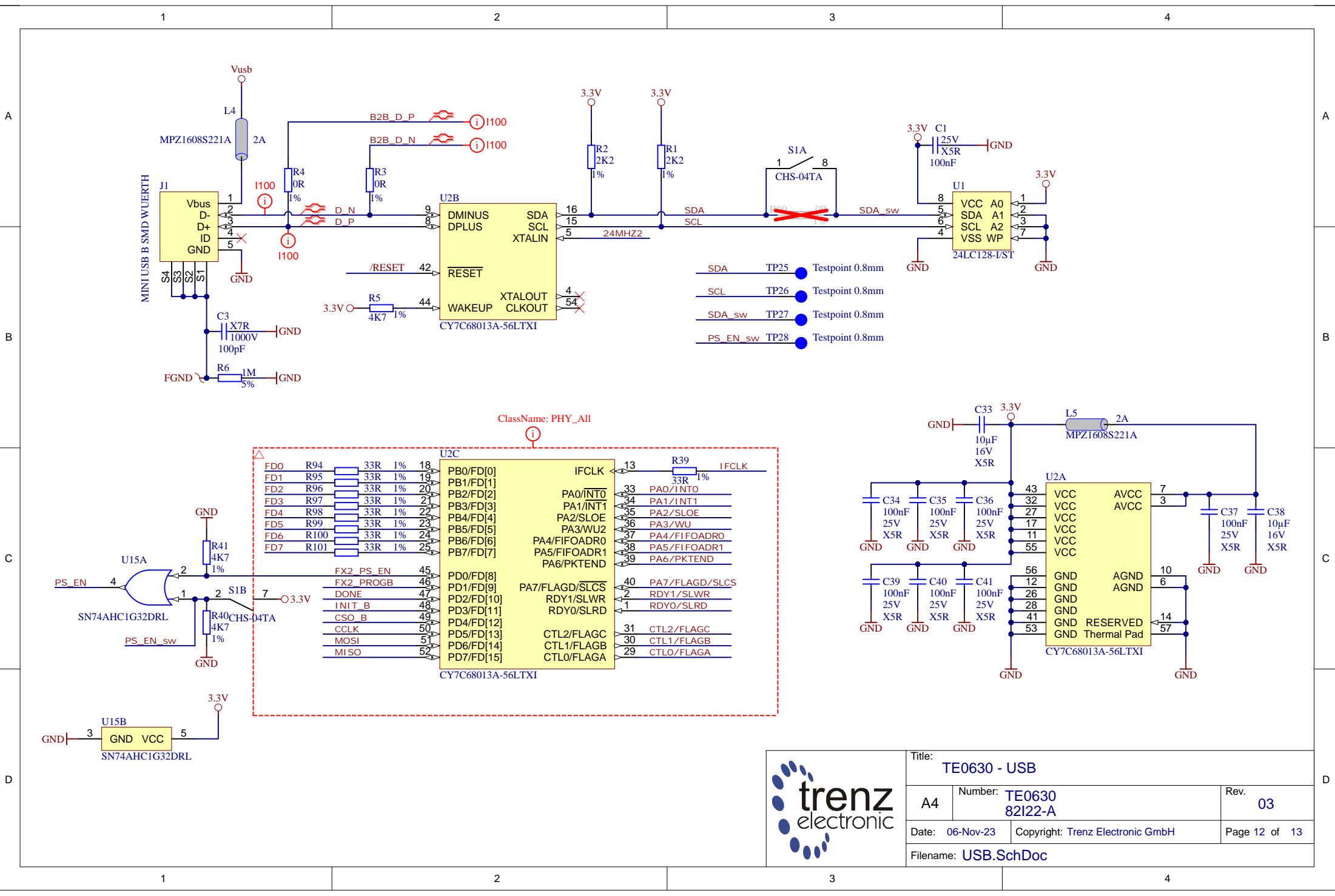
D



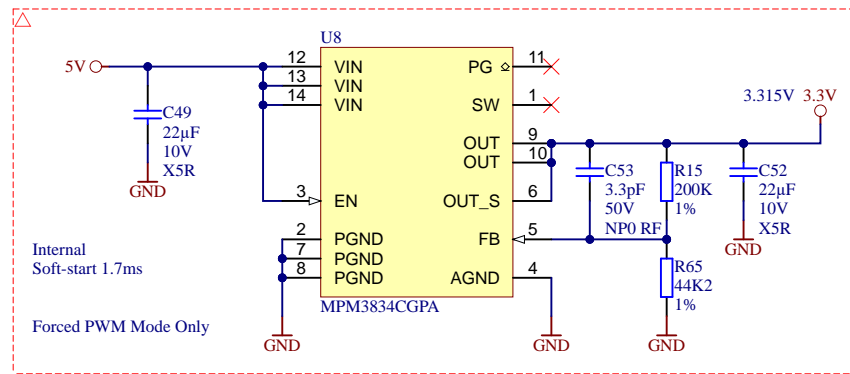
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Title: TE0630 - DDR3_RAM

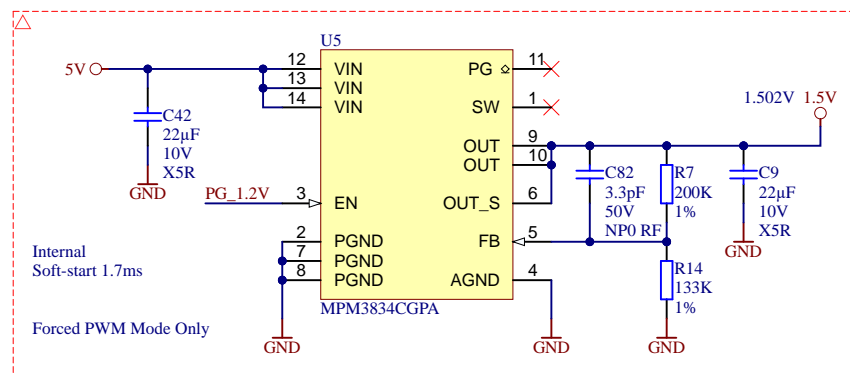
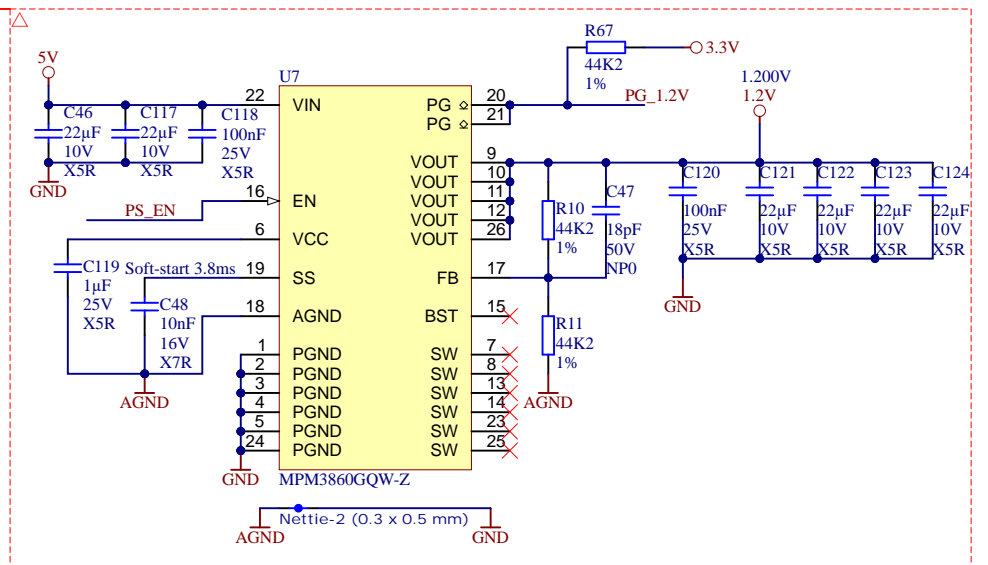
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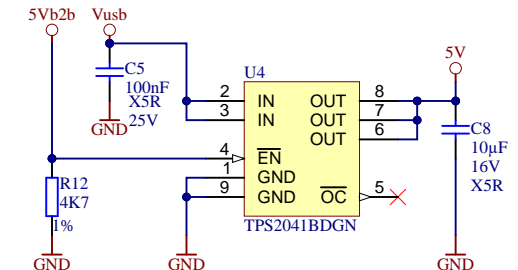
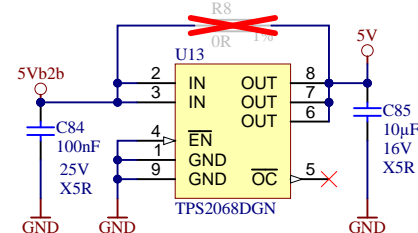
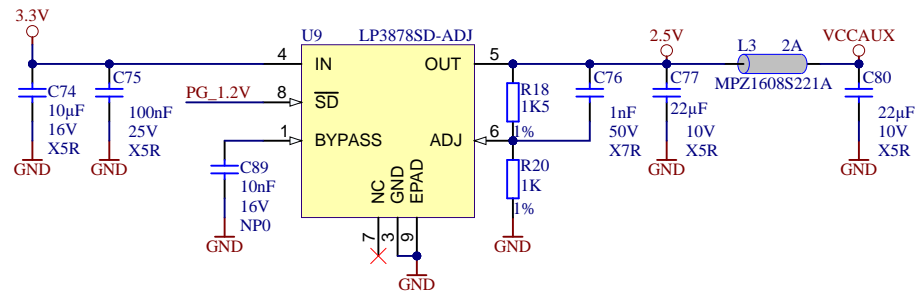
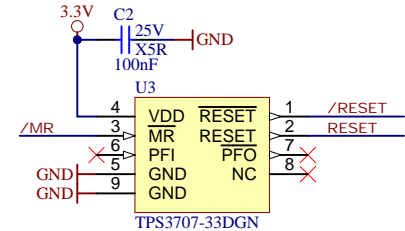
Title: TE0630 - USB		
A4	Number: TE0630 82122-A	Rev. 03
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REV3



REV3



	Title: TE0630 - POWER		
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