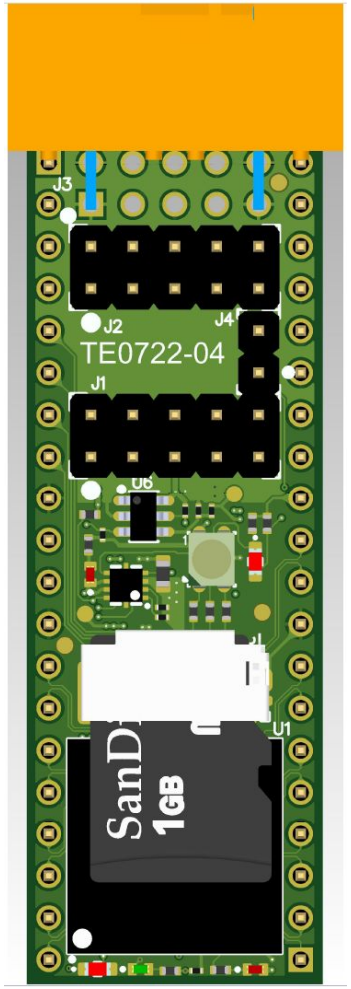

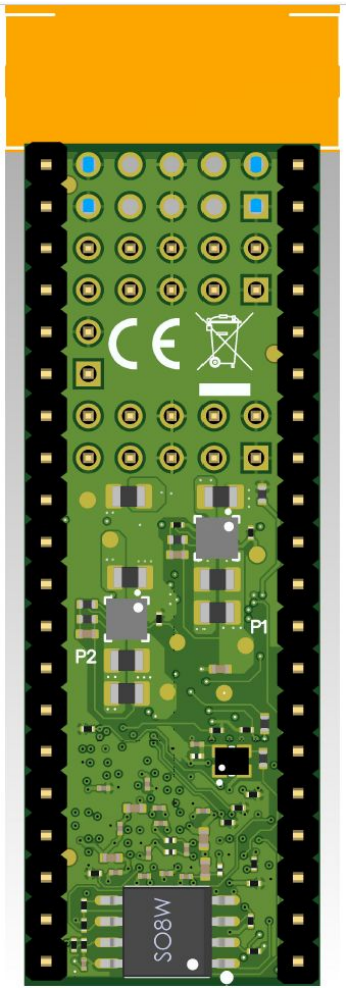

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Schematics and other handouts serve for informational purposes only!

Drawn by	VG
Checked by	IG
Assembly variant	41I-4-A
Created by	VG
Modified by	-
Modified at	16.03.2023

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Title: Legal Notices Modules		
A4	Number: TE0722 41I-4-A	Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH / TT	Page 1 of 10
Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02	1. component change: 1) replaced R7 on 10K, R15 on 19K1 2) added series resistors(33 Ohm) to RGB led (R29 .. R31) 3) added pull-up resistors (10K) to SD-card (R23 .. R28) 4) added series resistors 33 Ohm (R32, R21) 2. pin change: -functionality change: 1) Added testpoints for control voltages 2) Rebuilded all poligons 3) Changed voltage on resistor R7 (input sense supervisor) 3.3V -> 1.0V	
-03	1. U2, U3 EN5311QI were replaced by MPM3834CGPA 2. L1, L2, L4, L5 Ferrit beads BKP0603HS121-T replaced by MPZ0603S121HT000 3. Proximity/ambient light sensor Si1143-A11-GMR is EOL and not supported anymore 4. Clock generator SiT8008AI-73-XXS-33.333333E is replaced by SiT8008BI-73-XXS-33.333333E 5. Added Legal notices, power diagram	VG (15.03.2023)
-04	1. Added resistors R37, R38, R39 (DNP) 2. Added J4 (JTAG only Enable) 3. Added resistor R40 (10K) 4. The signals were renamed: - SPI-DQ0/M0 ---> SPI-DQ0/M3; - SPI-DQ3/M3 ---> SPI-DQ3/M0. According to AMD Table 6-4. 5. Added capacitor C27 (22µF). 6. Added testpoints TP6, TP9.	VG (20.09.2023)

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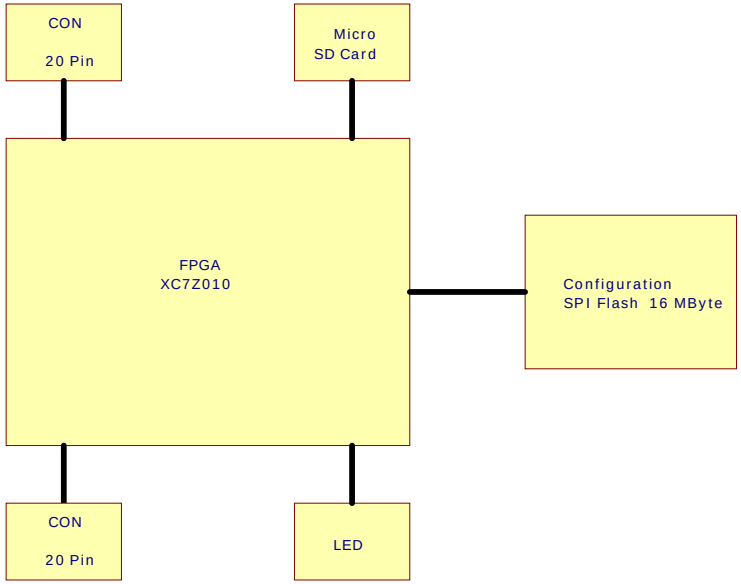
Title: Changes list

A4	Number: TE0722 41I-4-A	Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH	Page2 of 10
Filename: Revision_Changes.SchDoc		



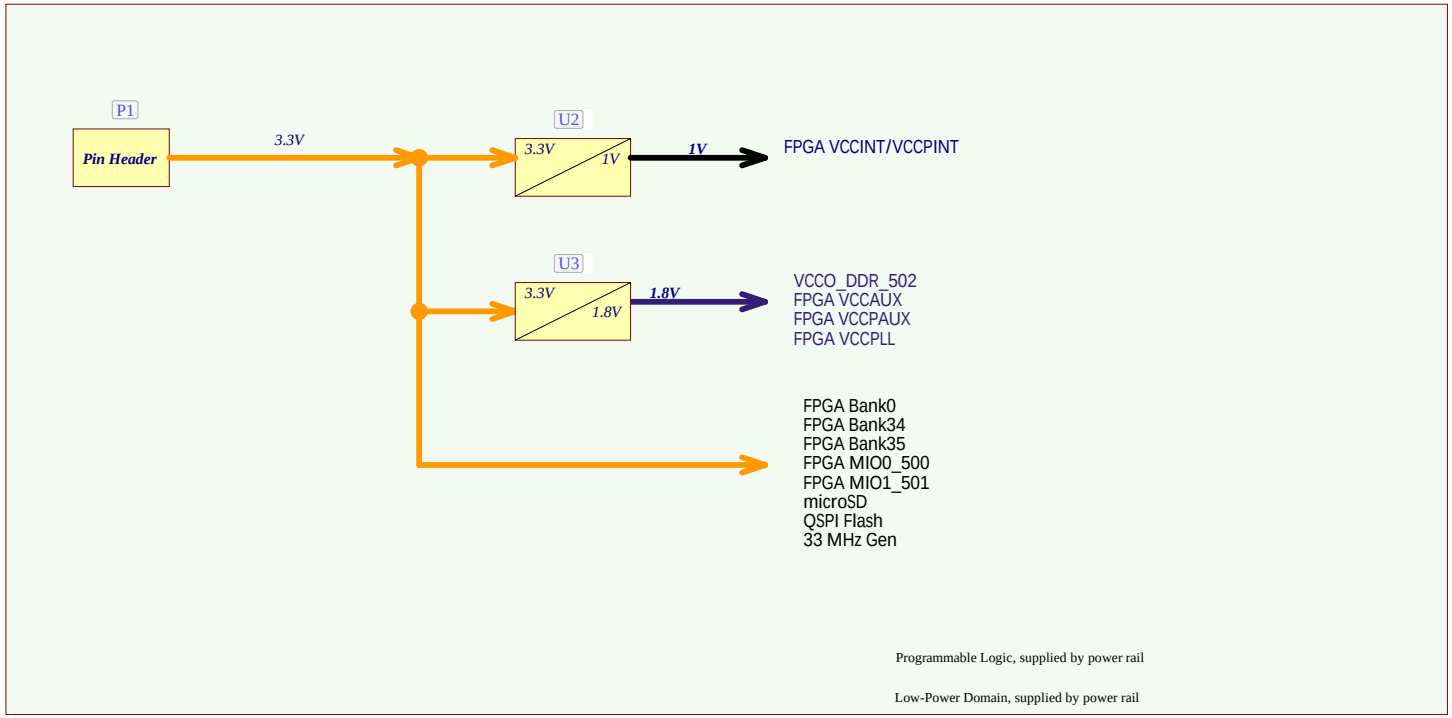
U_TE0722
TE0722.SchDoc

Serial
Serial
Serialnumber 6,3 x 6.3mm

UKCA1
CE Logo on Top Overlay
CE-TOPOVERLAY

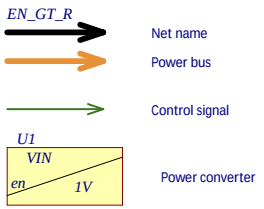
Title: Overview			
A4	Number: TE0722 41I-4-A		Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH		Page3 of 10
Filename: SoftPropeller_V1_40P14.SchDoc			

Power-on sequencing:

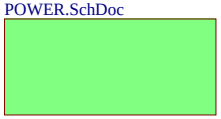


Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V from P1, P2	IN	3.3V	+/-3%	Micromodule Power	FPGA MIO0_500, MIO1_501, Bank0, Bank34, Bank35 micro SD, QSPI Flash, 33 MHz Gen



U_PowerSupply
POWER.SchDoc



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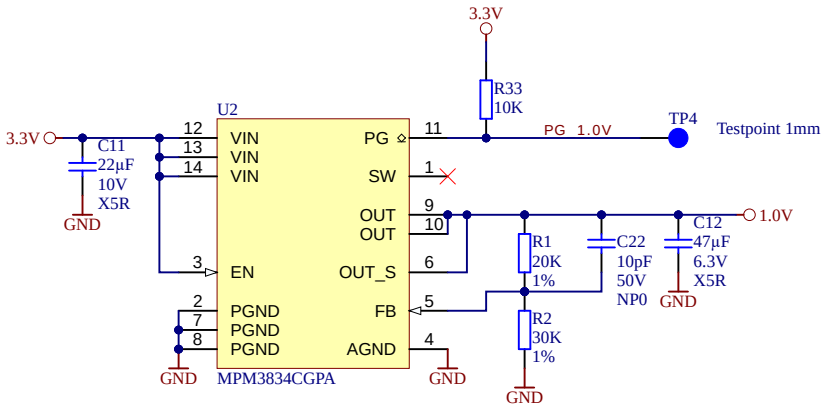
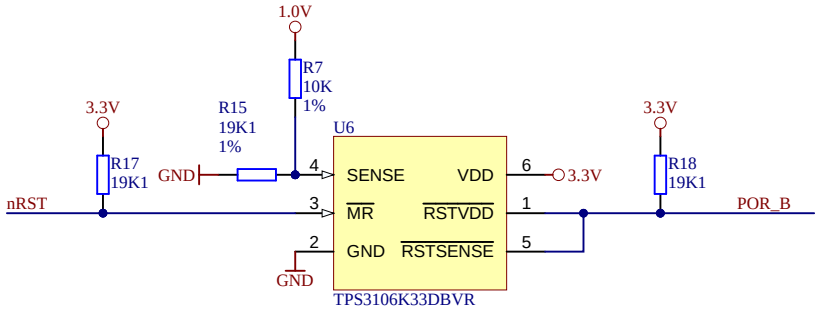
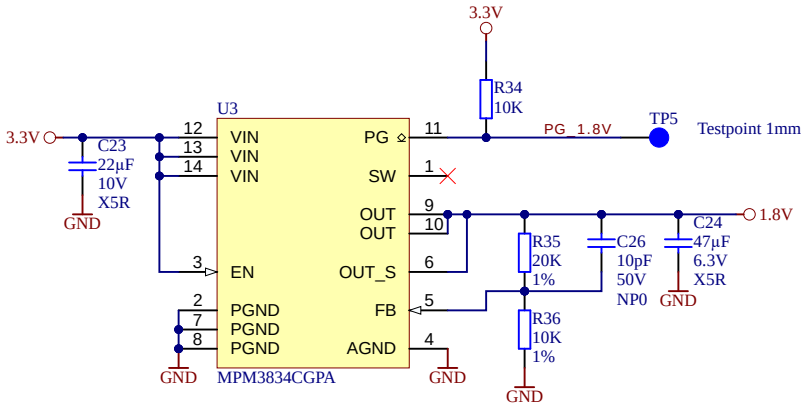
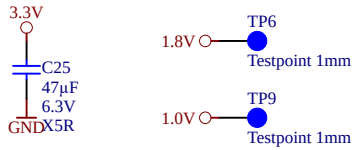
Title: Power Diagram			
A4	Number: TE0722 41I-4-A		Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH		Page4 of 10
Filename: Power_Diagram.SchDoc			









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Title: Power			
A4	Number: TE0722 41I-4-A		Rev. 04
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Filename: POWER.SchDoc			

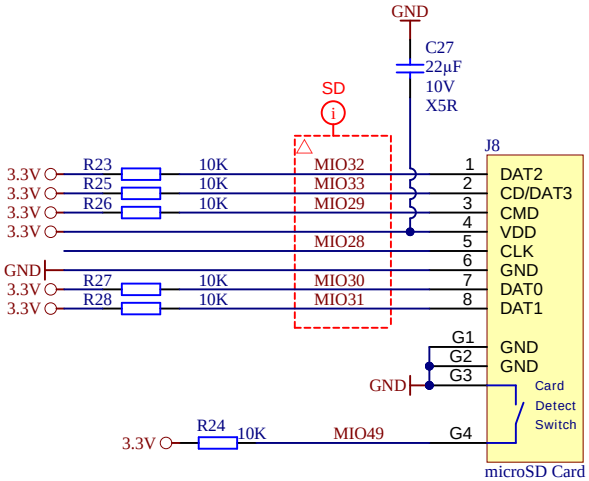
U_FPGA_B34
FPGA_B34.SchDoc

U_FPGA_B35
FPGA_B35.SchDoc

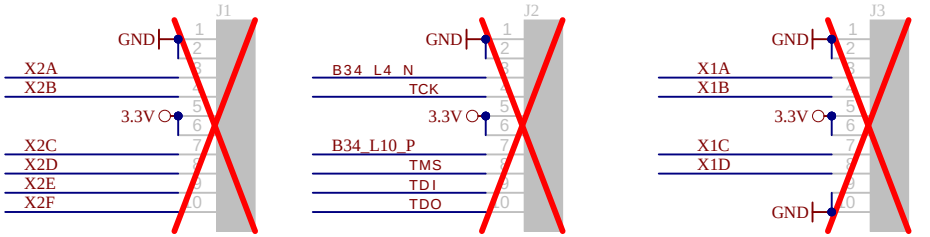
U_FPGA_MIO
FPGA_MIO.SchDoc

U_FPGA_PWR
FPGA_PWR.SchDoc

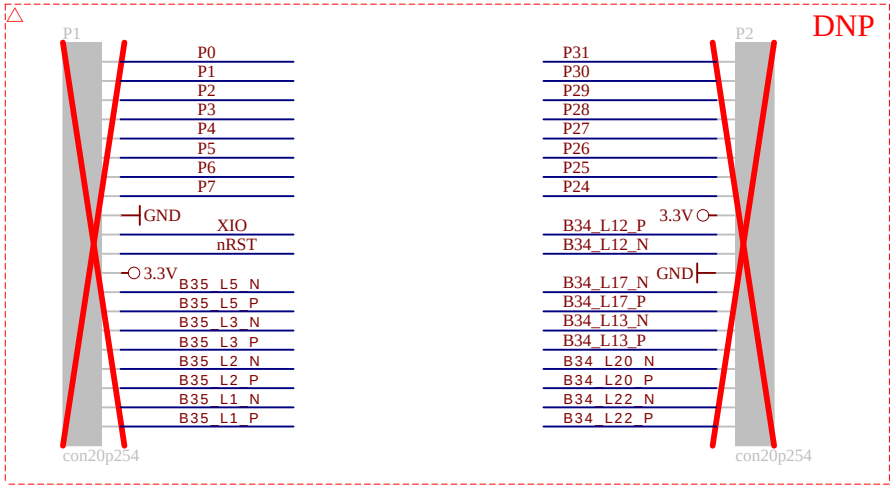
U_POWER
POWER.SchDoc

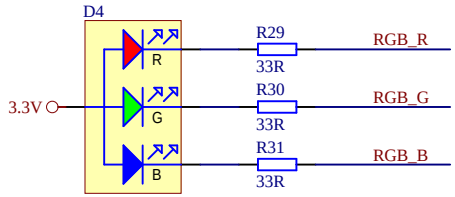


microSD Card Header with Detect Switch



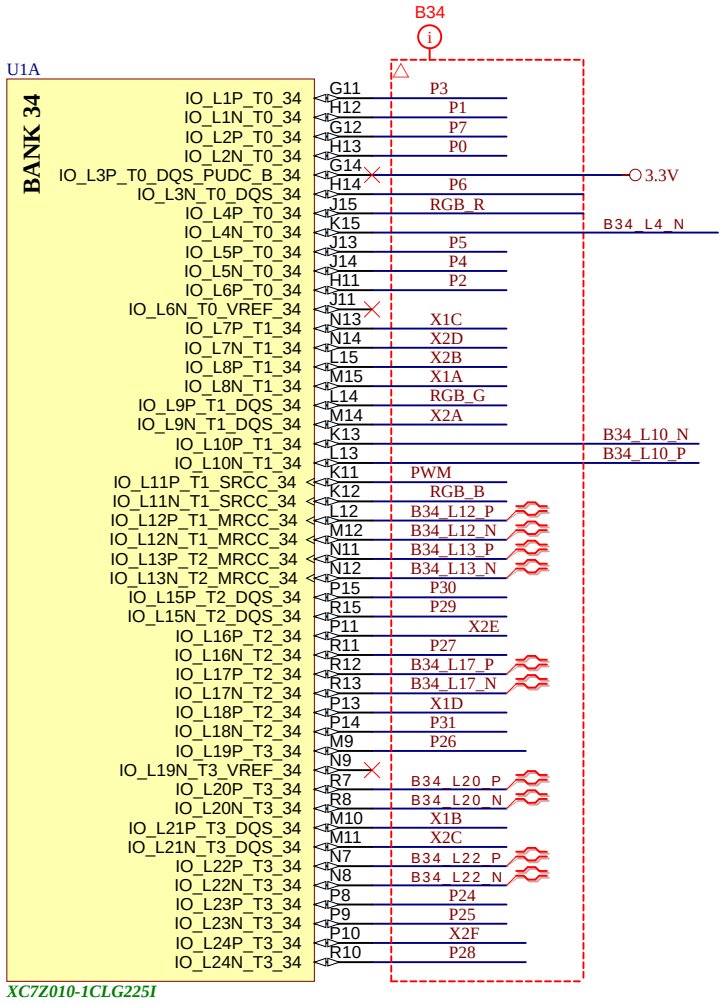
PM1 FIDU-DOT - mini
PM2 FIDU-DOT - mini
PM3 FIDU-DOT - mini
PM4 FIDU-DOT - mini
PM5 FIDU-DOT - mini
PM6 FIDU-DOT - mini



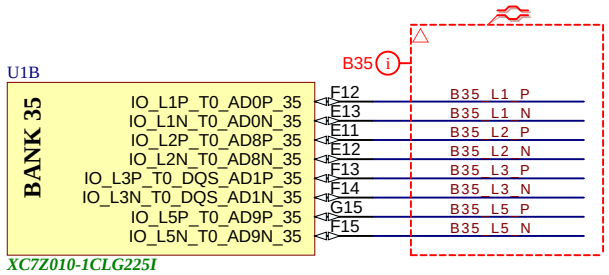


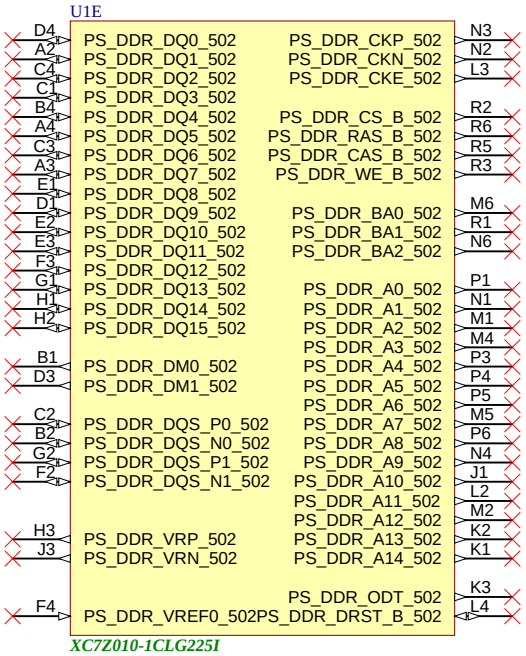
LED, RGB, 3528 PLCC

Title: Connectors			
A4	Number: TE0722 41I-4-A		Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH		Page6 of 10
Filename: TE0722.SchDoc			



trenz electronic	Title: B34		
	A4	Number: TE0722 41I-4-A	Rev. 04
	Date: 20.09.2023	Copyright: Trenz Electronic GmbH	Page7 of 10
	Filename: FPGA_B34.SchDoc		





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Title: B35			
A4	Number: TE0722 41I-4-A		Rev. 04
Date: 20.09.2023	Copyright: Trenz Electronic GmbH		Page 8 of 10
Filename: FPGA_B35.SchDoc			

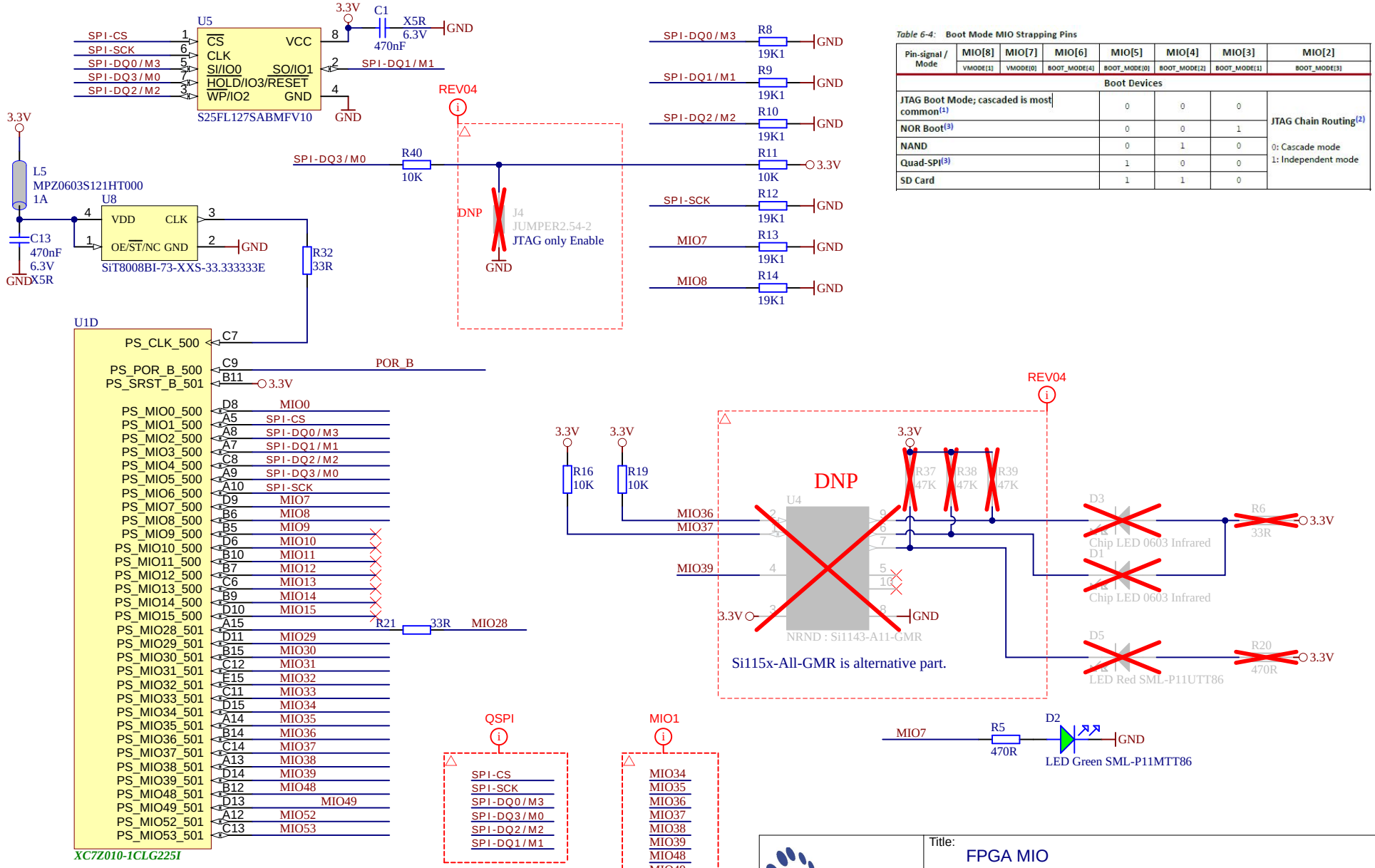

Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8] VMODE[1]	MIO[7] VMODE[0]	MIO[6] BOOT_MODE[4]	MIO[5] BOOT_MODE[0]	MIO[4] BOOT_MODE[2]	MIO[3] BOOT_MODE[1]	MIO[2] BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)	0	0	0				JTAG Chain Routing(2) 0: Cascade mode 1: Independent mode
NOR Boot(3)	0	0	1				
NAND	0	1	0				
Quad-SPI(3)	1	0	0				
SD Card	1	1	0				

Title: FPGA MIO			
A4	Number: TE0722 41I-4-A		Rev. 04
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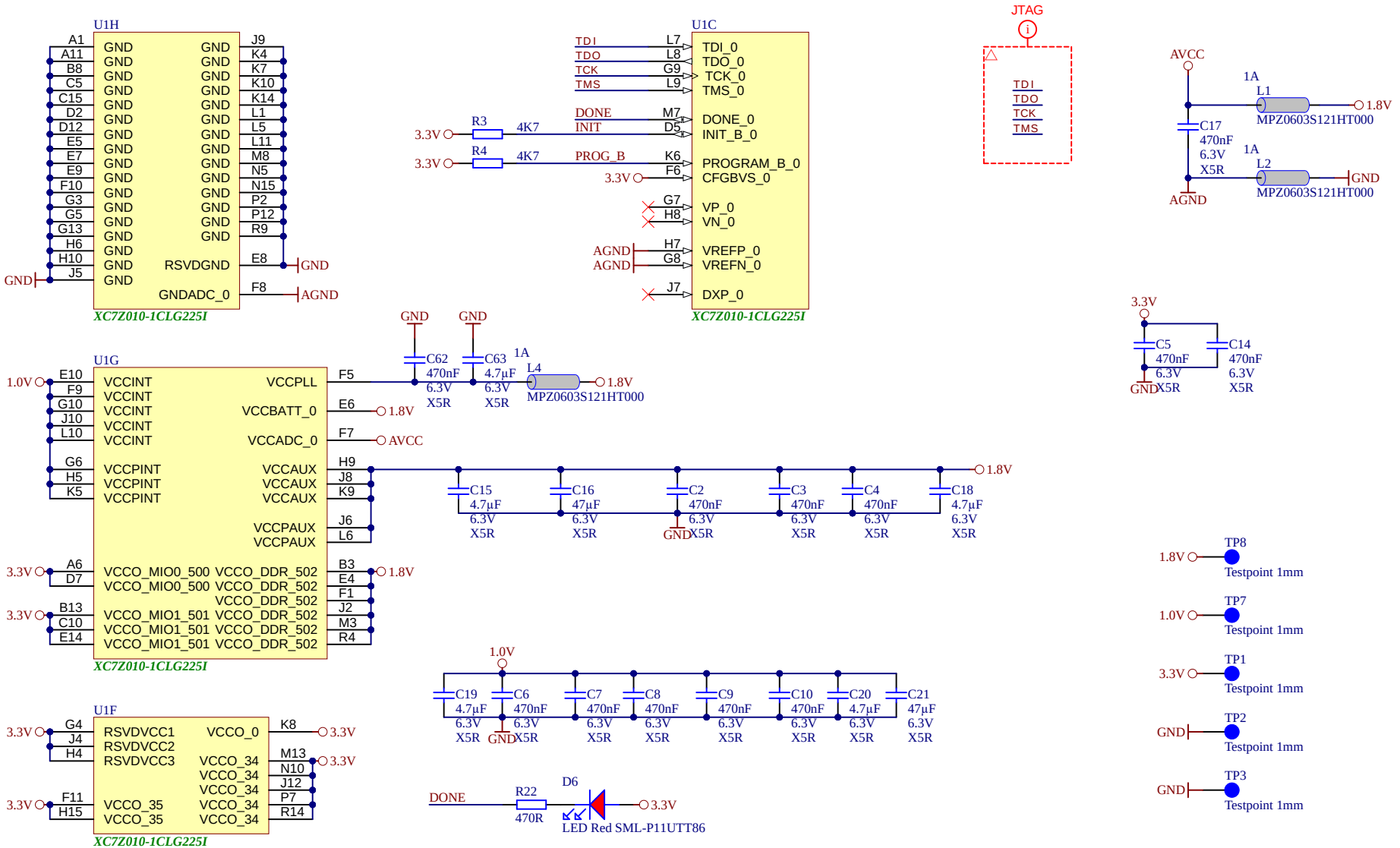
Filename: FPGA_MIO.SchDoc			



Title: FPGA PWR			
A4	Number: TE0722 41I-4-A		Rev. 04
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Filename: FPGA_PWR.SchDoc			