TE0722 Test Board

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Overview

Zynq PS Design with DDR Less FSBL Example.

Key Features

- UART
- QSPI
- Modified FSBL for DDR Less Zynq
- Special FSBL for QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2018-08-14	2018.2	TE0722-test_board-vivado_2018.2-build_02_20180815123557.zip TE0722-test_board_noprebuilt-vivado_2018.2-build_02_20180815123610.zip	John Hartfiel	initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Requirements

Software

Software	Version	Note
Vivado	2018.2	needed
SDK	2018.2	needed

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0722-02	10	REV02, REV01	--	16MB		
TE0722-02-I	10_i	REV02, REV01	--	16MB		

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0722-02-07S-1C	7s	REV02, REV01	--	16MB		

Design supports following carriers:

Carrier Model	Notes

Additional HW Requirements:

Additional Hardware	Notes
TE0790	for JTAG, UART
external 3.3V power supply	

Content

For general structure and of the reference design, see Project Delivery

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Additional Sources

Type	Location	Notes

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0722 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

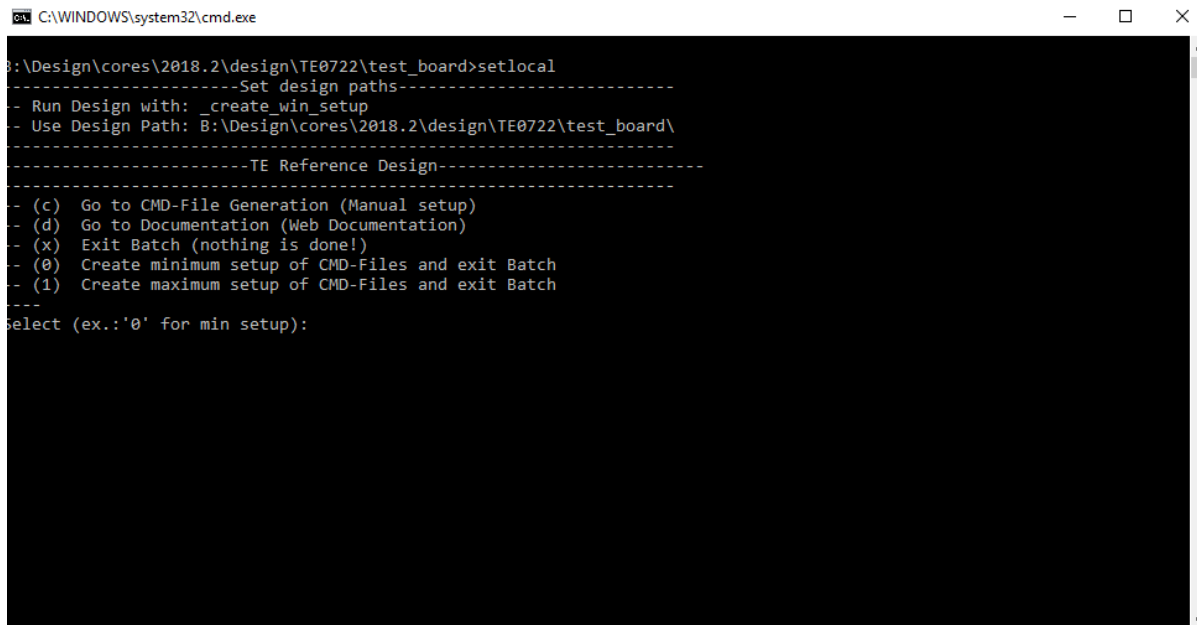Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)

4. Create Project
    a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
       Note: Select correct one, see TE Board Part Files
5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
       Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK
    a. Run on Vivado TCL: TE::sw_run_hsi
       Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
       Note: See SDK Projects

> ⓘ TE0722 is without DDR, so special FSBL (sources on reference designs) is needed, see also: DDR less ZYNQ Design

Launch

Basic Information, see TE0722 Getting Started

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp fsbl_app
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot only

JTAG

Not used on this Example.

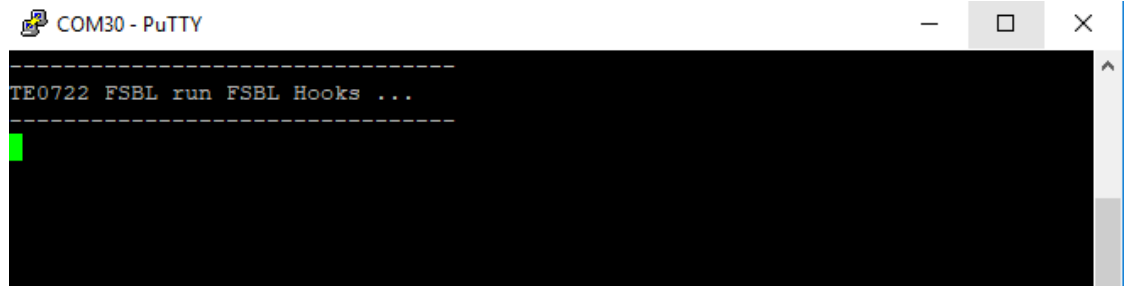## Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from QSPI into OCM, 2. FSBL loads bitfile from qsi, 3. FSBL starts application

Baremetal App

Note: UART over J2 is used, this is only available, if PL part is configured.

1. Open Serial Console (e.g. putty)
    a. Speed: 115200
    b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Output:
    a. Default output appears only one time. Reboot device: force ResN Pin to GND for short time, location see: TE0722 Getting Started
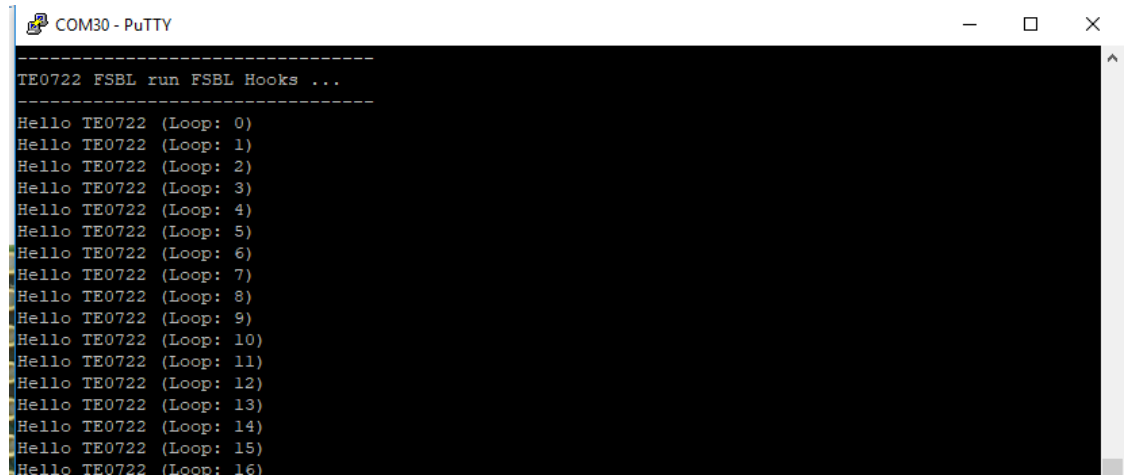
```
COM30 - PuTTY                                        —    □    ×
------------------------------
TE0722 FSBL run FSBL Hooks ...
------------------------------
```

    b. alternately Hello TE0722 loop (for 100sec): uncomment loop in fsbl example (fsbl_hooks.c) and regenerate FSBL and Boot.bin
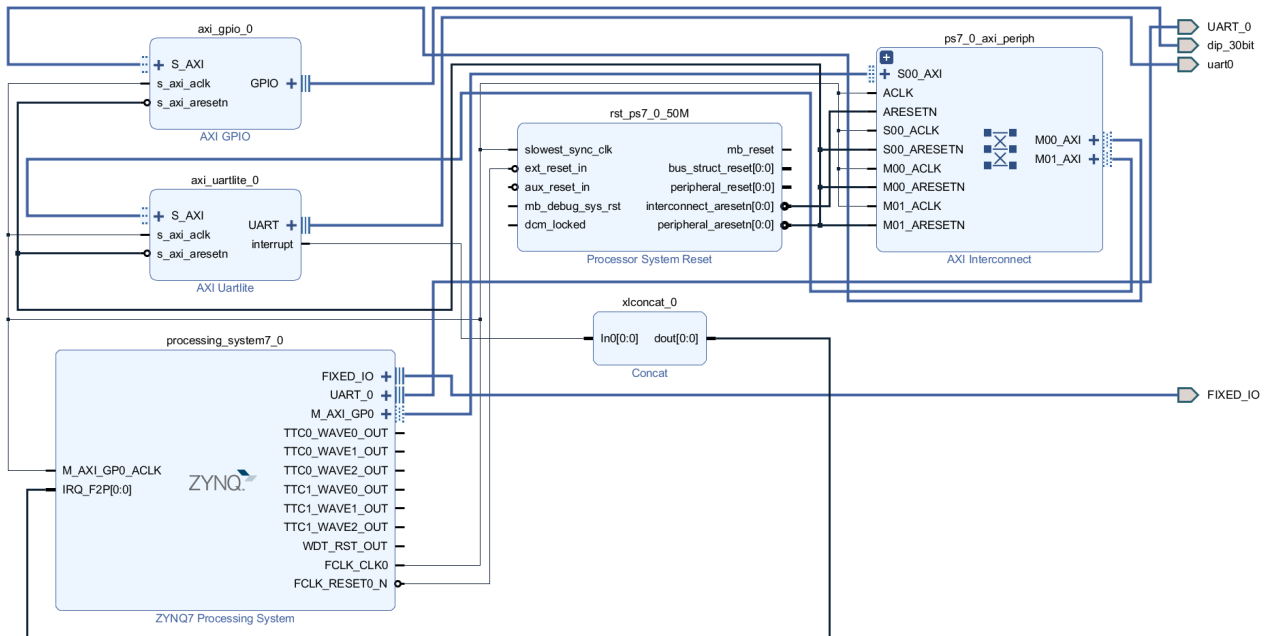
```
COM30 - PuTTY                                        —    □    ×
------------------------------
TE0722 FSBL run FSBL Hooks ...
------------------------------
Hello TE0722 (Loop: 0)
Hello TE0722 (Loop: 1)
Hello TE0722 (Loop: 2)
Hello TE0722 (Loop: 3)
Hello TE0722 (Loop: 4)
Hello TE0722 (Loop: 5)
Hello TE0722 (Loop: 6)
Hello TE0722 (Loop: 7)
Hello TE0722 (Loop: 8)
Hello TE0722 (Loop: 9)
Hello TE0722 (Loop: 10)
Hello TE0722 (Loop: 11)
Hello TE0722 (Loop: 12)
Hello TE0722 (Loop: 13)
Hello TE0722 (Loop: 14)
Hello TE0722 (Loop: 15)
Hello TE0722 (Loop: 16)
```

System Design - Vivado

Block Design

PS Interfaces

Type	Note
DDR	Disabled!
QSPI	MIO
SD	MIO
UART0	EMIO
I2C1	MIO
GPIO	MIO
SWDT0	EMIO
TTC0..1	EMIO

Constrains

Basic module constrains

```
_i_bitgen_common.xdc

#
# Common BITGEN related settings for TE0722
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

Design specific constrain

```
_iuart_j2xmod.xdc

set_property PACKAGE_PIN K15 [get_ports UART_0_txd]
set_property PACKAGE_PIN L13  [get_ports UART_0_rxd]

set_property IOSTANDARD LVCMOS33 [get_ports UART_0_*]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

Source location: \sw_lib\sw_apps

zynqmp_fsbl

TE modified 2018.2 FSBL

Changes:

- Disable Memory initialisation on main.c
- add addition console output to fsbl_hooks.c

zynqmp_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2019-05-14	v.6 Unbekanntes Makro: 'metadata'	John Hartfiel	• 2018.2 release
2018-10-14	v.1	John Hartfiel	• Initial release
	All	John Hartfiel	

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