

1

2

3

4

U_A-Headers
A-Headers.SchDoc



U_Analog
Analog.SchDoc



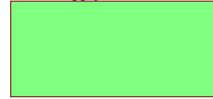
U_DDR3-RAM
DDR3-RAM.SchDoc



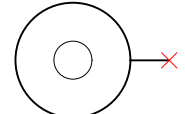
U_USB-PHY
USB-PHY.SchDoc



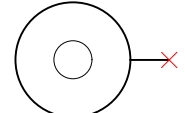
U_PowerSupply
PowerSupply.SchDoc



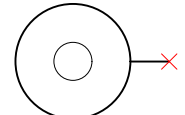
U_FTDI
FTDI.SchDoc



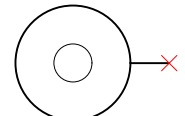
Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)

A

A

U_FPGA_B34
FPGA_B34.SchDoc



U_FPGA_B35
FPGA_B35.SchDoc



B

B

U_FPGA_MIO
FPGA_MIO.SchDoc



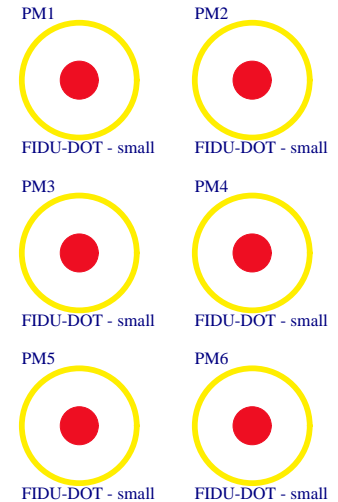
U_FPGA_RAM
FPGA_RAM.SchDoc



C

C

U_FPGA_PWR
FPGA_PWR.SchDoc



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm

D

D



Title: TE0723		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page1 of 12
Filename: TE0723.SchDoc		

1

2

3

4

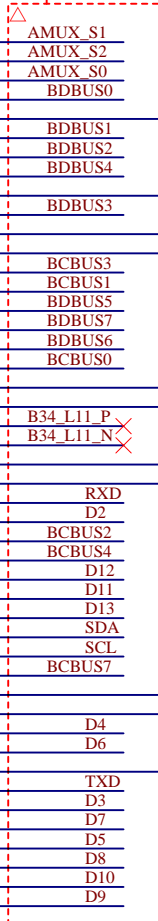
U1A

BANK 34

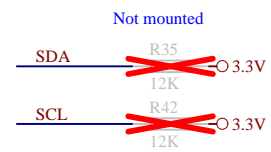
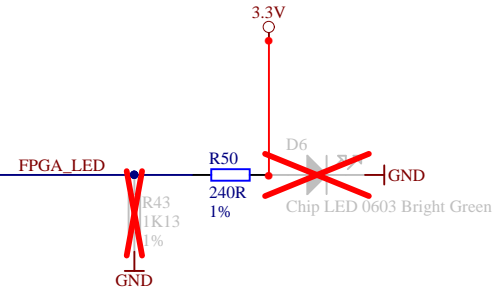
IO_L1P_T0_34	G11	AMUX_S1	Analog MUX
IO_L1N_T0_34	H12	AMUX_S2	Analog MUX
IO_L2P_T0_34	G12	AMUX_S0	Analog MUX
IO_L2N_T0_34	H13	BDBUS0	FTDI PORT B
IO_L3P_T0_DQS_PUDC_B_34	G14		
IO_L3N_T0_DQS_34	H14	BDBUS1	FTDI PORT B
IO_L4P_T0_34	J15	BDBUS2	FTDI PORT B
IO_L4N_T0_34	K15	BDBUS4	FTDI PORT B
IO_L5P_T0_34	J13		PIO_04 PMOD
IO_L5N_T0_34	J14	BDBUS3	FTDI PORT B
IO_L6P_T0_34	H11		PIO_08 PMOD
IO_L6N_T0_VREF_34	J11		PIO_07 PMOD
IO_L7P_T1_34	N13	BCBUS3	FTDI PORT B
IO_L7N_T1_34	N14	BCBUS1	FTDI PORT B
IO_L8P_T1_34	L15	BDBUS5	FTDI PORT B
IO_L8N_T1_34	M15	BDBUS7	FTDI PORT B
IO_L9P_T1_DQS_34	L14	BDBUS6	FTDI PORT B
IO_L9N_T1_DQS_34	M14	BCBUS0	FTDI PORT B
IO_L10P_T1_34	K13		PIO_03 PMOD
IO_L10N_T1_34	L13		HOST_MODE_EN SELECT usb mode
IO_L11P_T1_SRCC_34	K11	B34_L11_P	NC
IO_L11N_T1_SRCC_34	K12	B34_L11_N	NC
IO_L12P_T1_MRCC_34	L12		R44 33R 1% AIN_FPGA
IO_L12N_T1_MRCC_34	M12		PIO_06 PMOD
IO_L13P_T2_MRCC_34	N11	RXD	DIGITAL HEADER
IO_L13N_T2_MRCC_34	N12	D2	DIGITAL HEADER
IO_L15P_T2_DQS_34	P15	BCBUS2	FTDI PORT B
IO_L15N_T2_DQS_34	R15	BCBUS4	FTDI PORT B
IO_L16P_T2_34	P11	D12	DIGITAL HEADER
IO_L16N_T2_34	R11	D11	DIGITAL HEADER
IO_L17P_T2_34	R12	D13	DIGITAL HEADER
IO_L17N_T2_34	R13	SDA	DIGITAL HEADER
IO_L18P_T2_34	P13	SCL	DIGITAL HEADER
IO_L18N_T2_34	P14	BCBUS7	FTDI PORT B
IO_L19P_T3_34	M9		PIO_01 PMOD
IO_L19N_T3_VREF_34	N9		PIO_05 PMOD
IO_L20P_T3_34	R7	D4	DIGITAL HEADER
IO_L20N_T3_34	R8	D6	DIGITAL HEADER
IO_L21P_T3_DQS_34	M10		PIO_02 PMOD
IO_L21N_T3_DQS_34	M11	TXD	DIGITAL HEADER
IO_L22P_T3_34	N7	D3	DIGITAL HEADER
IO_L22N_T3_34	N8	D7	DIGITAL HEADER
IO_L23P_T3_34	P8	D5	DIGITAL HEADER
IO_L23N_T3_34	P9	D8	DIGITAL HEADER
IO_L24P_T3_34	P10	D10	DIGITAL HEADER
IO_L24N_T3_34	R10	D9	DIGITAL HEADER

XC7Z010-1CLG225C

B34



PCB patch for variant TE0723-02C:



Title: TE0723 - FPGA B34		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page2 of 12
Filename: FPGA_B34.SchDoc		

1

2

3

4

A

A

B

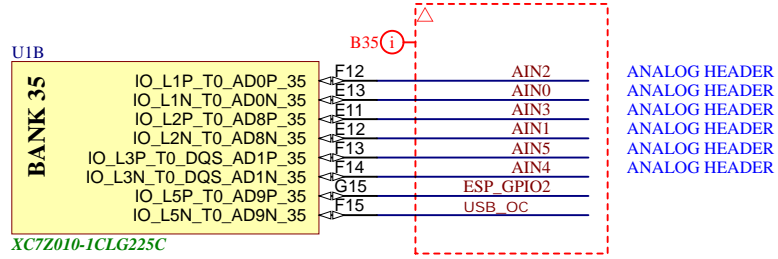
B


C

C

D

D



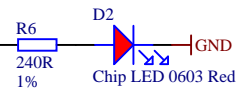
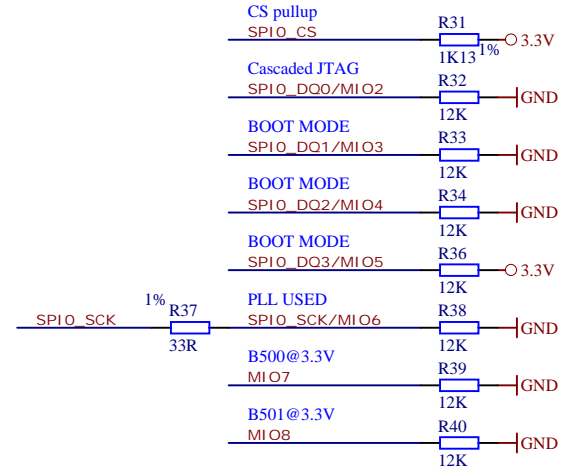
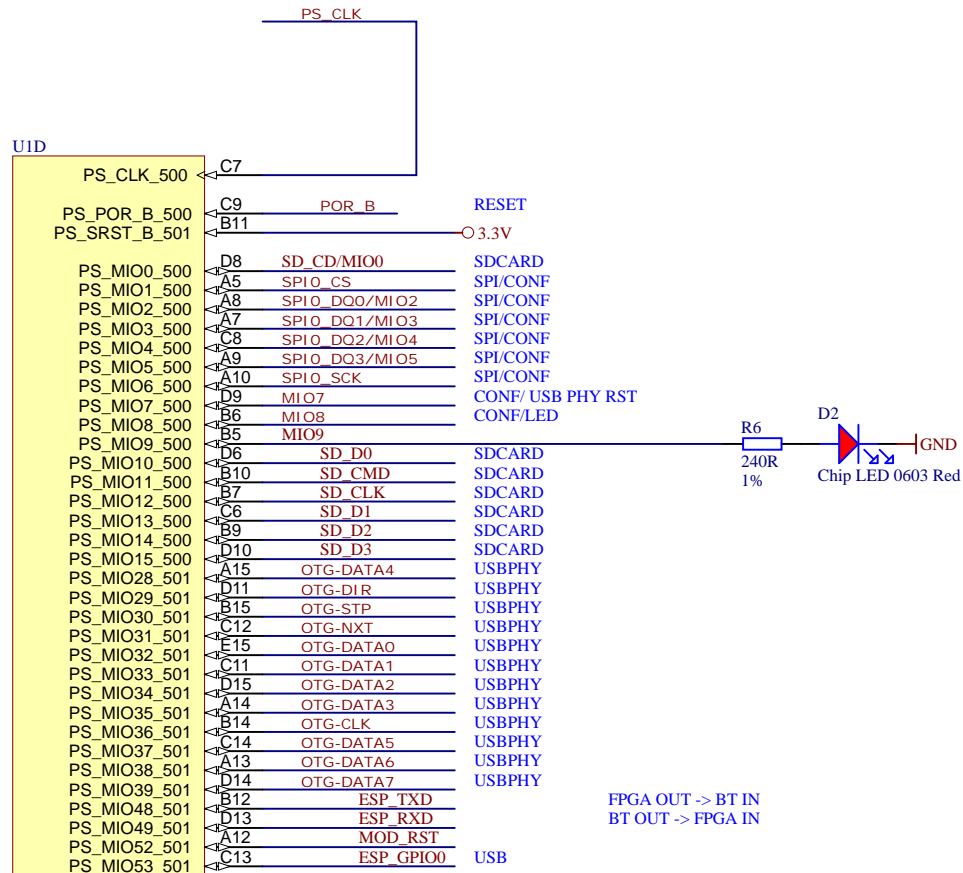
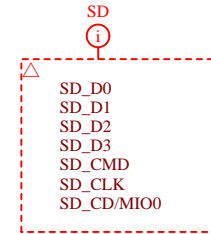
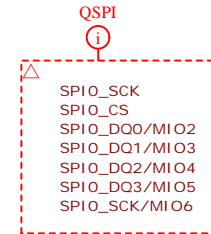
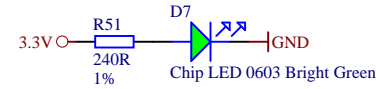
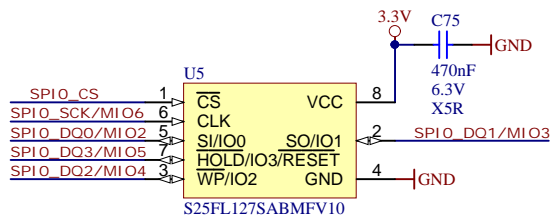
	Title: TE0723 - FPGA B35		
	A4	Number: TE0723 TE0723_C	Rev. 02
	Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page 3 of 12
	Filename: FPGA_B35.SchDoc		

1

2

3

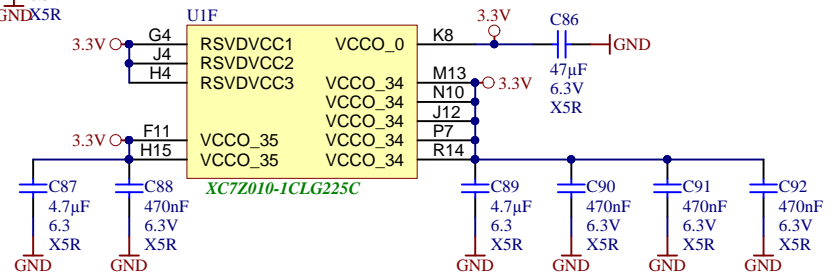
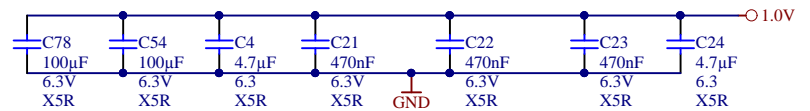
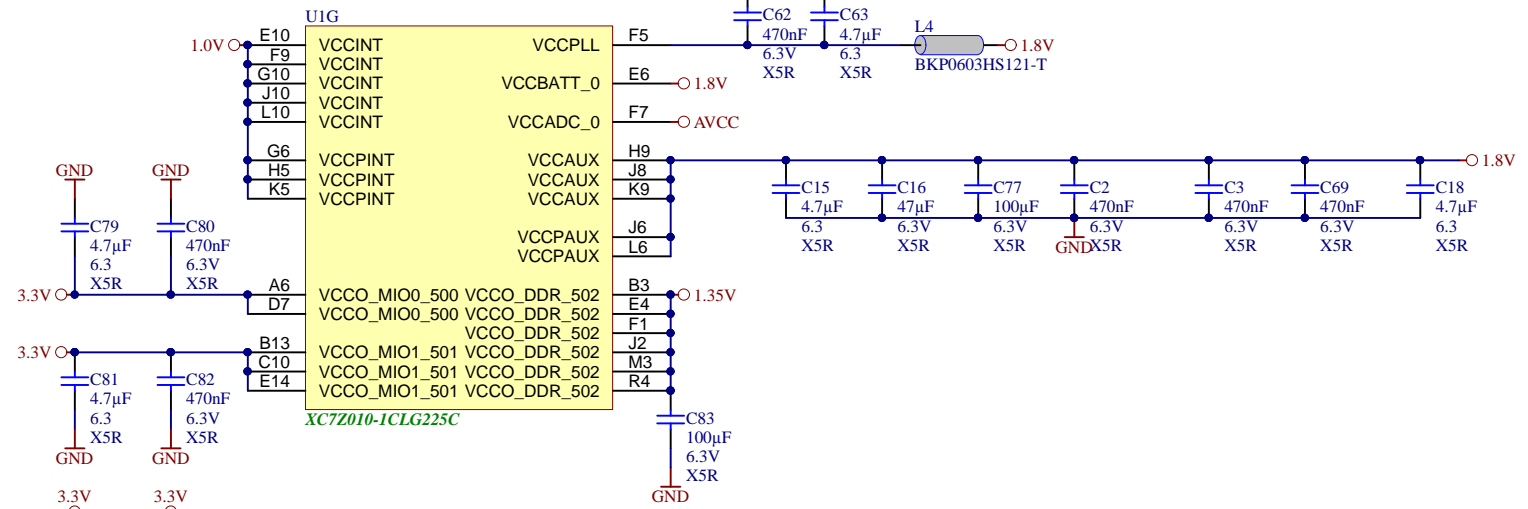
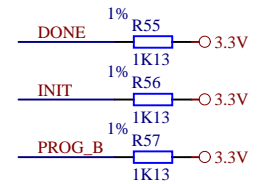
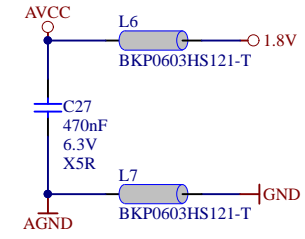
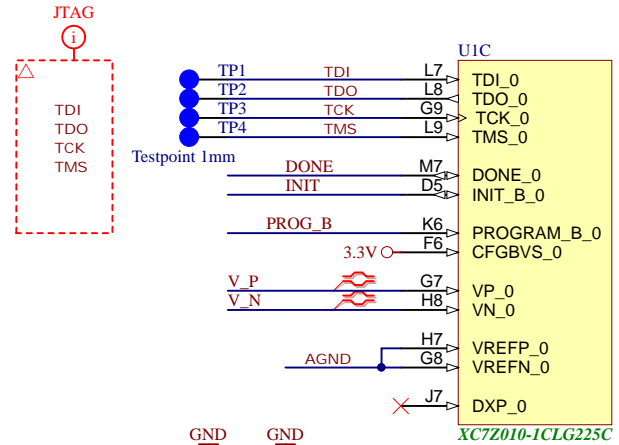
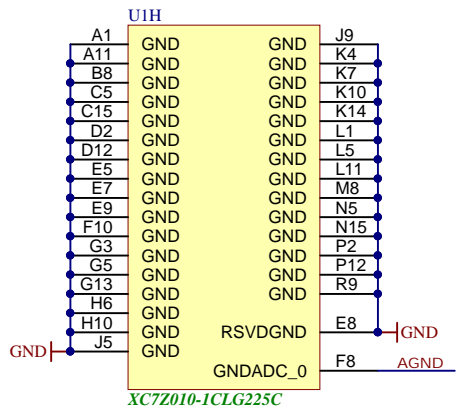
4



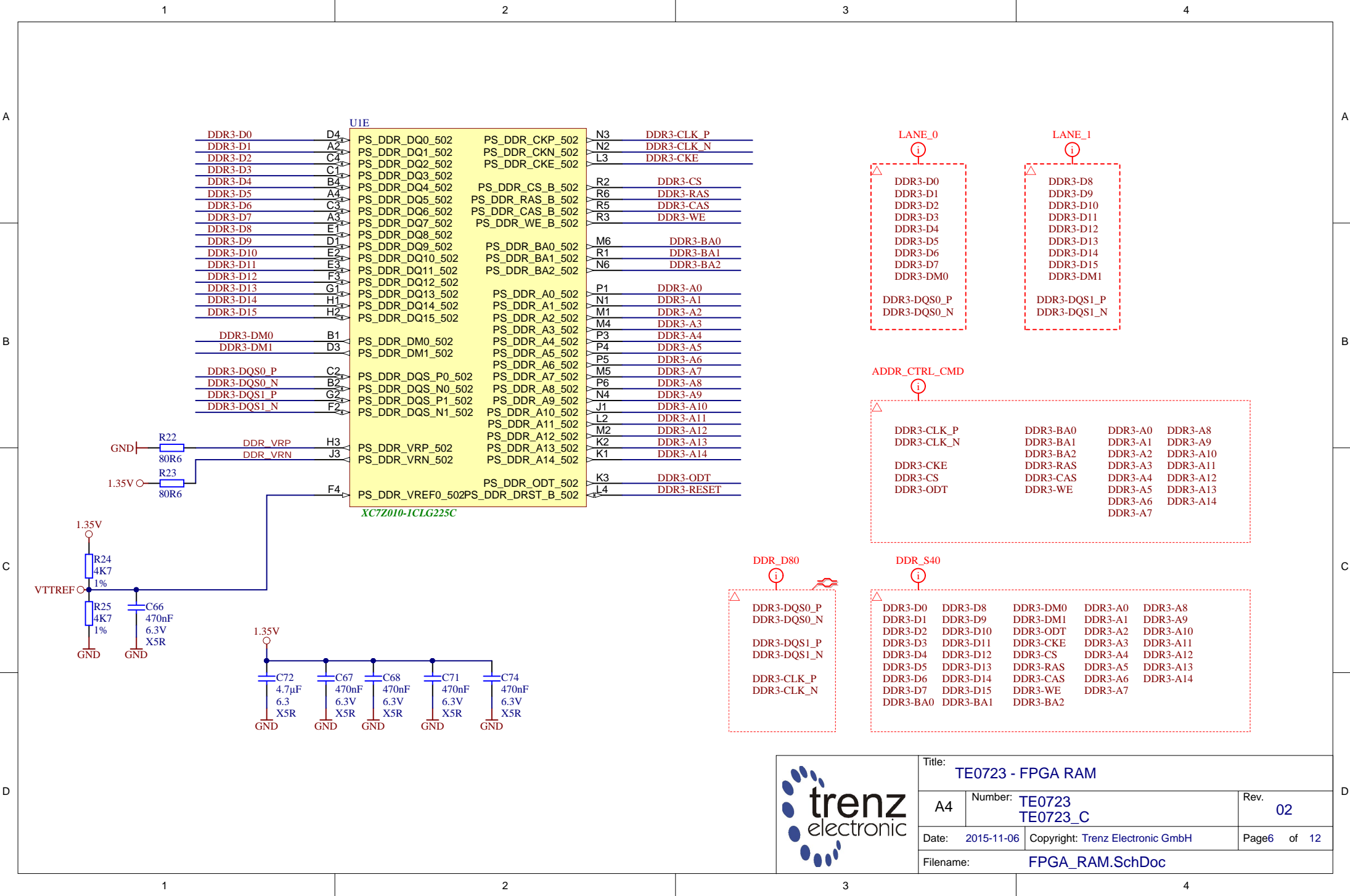
FPGA OUT -> BT IN
BT OUT -> FPGA IN

		Title: TE0723 - FPGA MIO	
		A4	Number: TE0723 TE0723_C
Date: 2015-11-06		Copyright: Trenz Electronic GmbH	
Page 4 of 12		Page 4 of 12	
Filename: FPGA_MIO.SchDoc			

XC7Z010-1CLG225C



Title: TE0723 - FPGA PWR		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page5 of 12
Filename: FPGA_PWR.SchDoc		



A

B

C

D

1

2

3

4

A

B

C

D

U1E

DDR3-D0	D4	PS_DDR_DQ0_502	PS_DDR_CKP_502	N3	DDR3-CLK_P
DDR3-D1	A2	PS_DDR_DQ1_502	PS_DDR_CKN_502	N2	DDR3-CLK_N
DDR3-D2	C4	PS_DDR_DQ2_502	PS_DDR_CKE_502	L3	DDR3-CKE
DDR3-D3	C1	PS_DDR_DQ3_502		R2	DDR3-CS
DDR3-D4	B4	PS_DDR_DQ4_502	PS_DDR_CS_B_502	R6	DDR3-RAS
DDR3-D5	A4	PS_DDR_DQ5_502	PS_DDR_RAS_B_502	R5	DDR3-CAS
DDR3-D6	C3	PS_DDR_DQ6_502	PS_DDR_CAS_B_502	R3	DDR3-WE
DDR3-D7	A3	PS_DDR_DQ7_502	PS_DDR_WE_B_502		
DDR3-D8	E1	PS_DDR_DQ8_502		M6	DDR3-BA0
DDR3-D9	D1	PS_DDR_DQ9_502	PS_DDR_BA0_502	R1	DDR3-BA1
DDR3-D10	E2	PS_DDR_DQ10_502	PS_DDR_BA1_502	N6	DDR3-BA2
DDR3-D11	E3	PS_DDR_DQ11_502	PS_DDR_BA2_502		
DDR3-D12	F3	PS_DDR_DQ12_502		P1	DDR3-A0
DDR3-D13	G1	PS_DDR_DQ13_502	PS_DDR_A0_502	N1	DDR3-A1
DDR3-D14	H1	PS_DDR_DQ14_502	PS_DDR_A1_502	M1	DDR3-A2
DDR3-D15	H2	PS_DDR_DQ15_502	PS_DDR_A2_502	M4	DDR3-A3
DDR3-DM0	B1	PS_DDR_DM0_502	PS_DDR_A3_502	P3	DDR3-A4
DDR3-DM1	D3	PS_DDR_DM1_502	PS_DDR_A4_502	P4	DDR3-A5
DDR3-DQS0_P	C2	PS_DDR_DQS_P0_502	PS_DDR_A5_502	P5	DDR3-A6
DDR3-DQS0_N	B2	PS_DDR_DQS_N0_502	PS_DDR_A6_502	M5	DDR3-A7
DDR3-DQS1_P	G2	PS_DDR_DQS_P1_502	PS_DDR_A7_502	P6	DDR3-A8
DDR3-DQS1_N	F2	PS_DDR_DQS_N1_502	PS_DDR_A8_502	N4	DDR3-A9
			PS_DDR_A9_502	J1	DDR3-A10
			PS_DDR_A10_502	L2	DDR3-A11
			PS_DDR_A11_502	M2	DDR3-A12
			PS_DDR_A12_502	K2	DDR3-A13
			PS_DDR_A13_502	K1	DDR3-A14
			PS_DDR_A14_502		
			PS_DDR_ODT_502	K3	DDR3-ODT
			PS_DDR_DRST_B_502	L4	DDR3-RESET

XC7Z010-1CLG225C

LANE_0

LANE_1

DDR3-D0
DDR3-D1
DDR3-D2
DDR3-D3
DDR3-D4
DDR3-D5
DDR3-D6
DDR3-D7
DDR3-DM0
DDR3-DQS0_P
DDR3-DQS0_N

DDR3-D8
DDR3-D9
DDR3-D10
DDR3-D11
DDR3-D12
DDR3-D13
DDR3-D14
DDR3-D15
DDR3-DM1
DDR3-DQS1_P
DDR3-DQS1_N

ADDR_CTRL_CMD

DDR3-CLK_P	DDR3-BA0	DDR3-A0	DDR3-A8
DDR3-CLK_N	DDR3-BA1	DDR3-A1	DDR3-A9
DDR3-CKE	DDR3-BA2	DDR3-A2	DDR3-A10
DDR3-CS	DDR3-RAS	DDR3-A3	DDR3-A11
DDR3-ODT	DDR3-CAS	DDR3-A4	DDR3-A12
	DDR3-WE	DDR3-A5	DDR3-A13
		DDR3-A6	DDR3-A14
		DDR3-A7	

DDR_D80

DDR_S40

DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-CLK_P
DDR3-CLK_N

DDR3-D0	DDR3-D8	DDR3-DM0	DDR3-A0	DDR3-A8
DDR3-D1	DDR3-D9	DDR3-DM1	DDR3-A1	DDR3-A9
DDR3-D2	DDR3-D10	DDR3-ODT	DDR3-A2	DDR3-A10
DDR3-D3	DDR3-D11	DDR3-CKE	DDR3-A3	DDR3-A11
DDR3-D4	DDR3-D12	DDR3-CS	DDR3-A4	DDR3-A12
DDR3-D5	DDR3-D13	DDR3-RAS	DDR3-A5	DDR3-A13
DDR3-D6	DDR3-D14	DDR3-CAS	DDR3-A6	DDR3-A14
DDR3-D7	DDR3-D15	DDR3-WE	DDR3-A7	
DDR3-BA0	DDR3-BA1	DDR3-BA2		



Title: TE0723 - FPGA RAM			
A4	Number: TE0723 TE0723_C	Rev. 02	
Date: 2015-11-06	Copyright: Trenz Electronic GmbH		Page 6 of 12
Filename: FPGA_RAM.SchDoc			

1

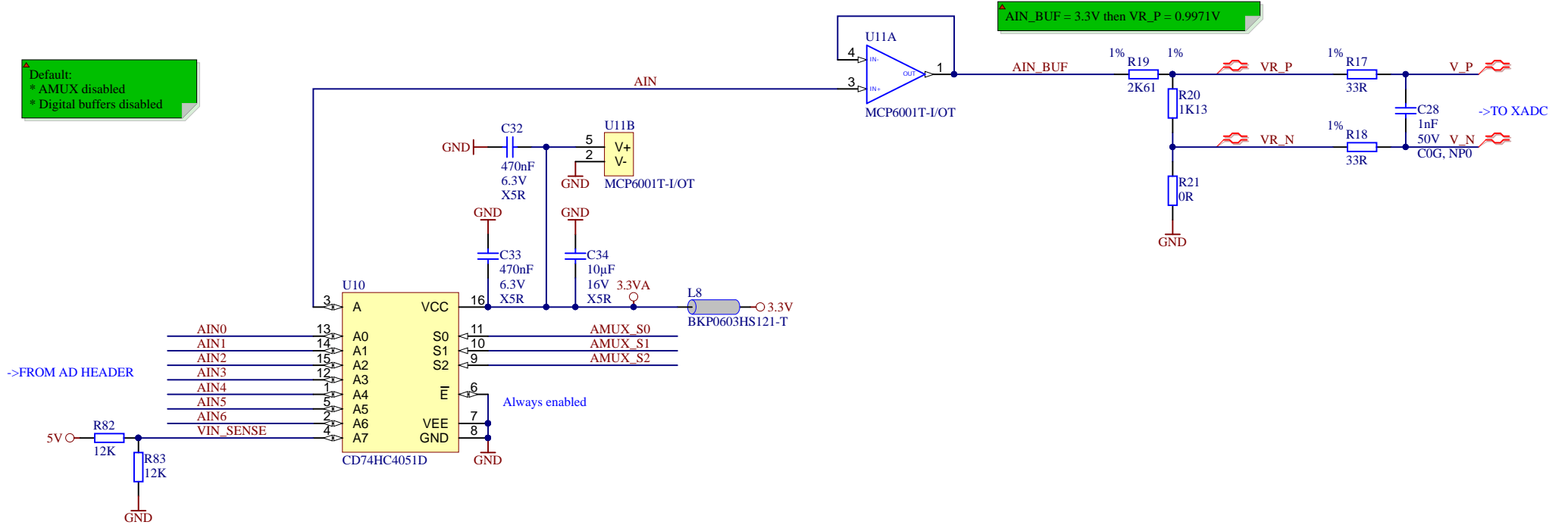
2


3

4

Default:
 * AMUX disabled
 * Digital buffers disabled

AIN_BUF = 3.3V then VR_P = 0.9971V



		Title: TE0723 - Analog Input	
		A4	Number: TE0723 TE0723_C
Date: 2015-11-06		Copyright: Trenz Electronic GmbH	
Filename: Analog.SchDoc		Page 7 of 12	

A

A

B

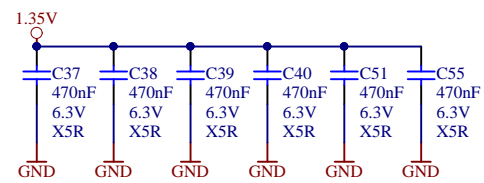
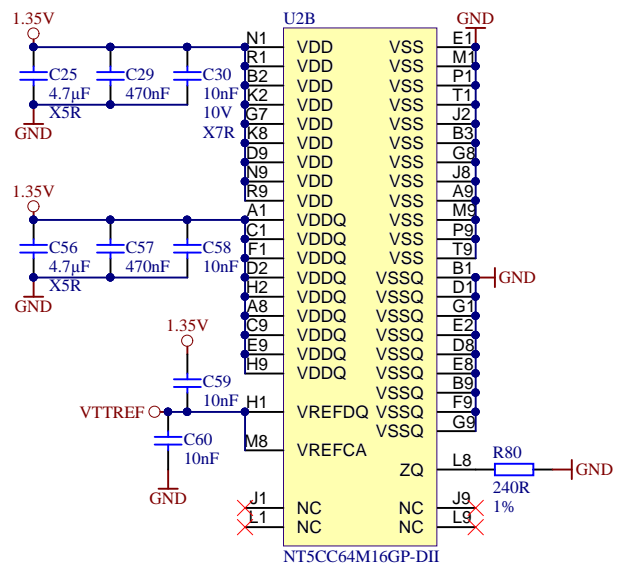
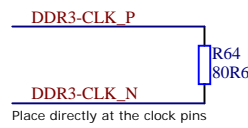
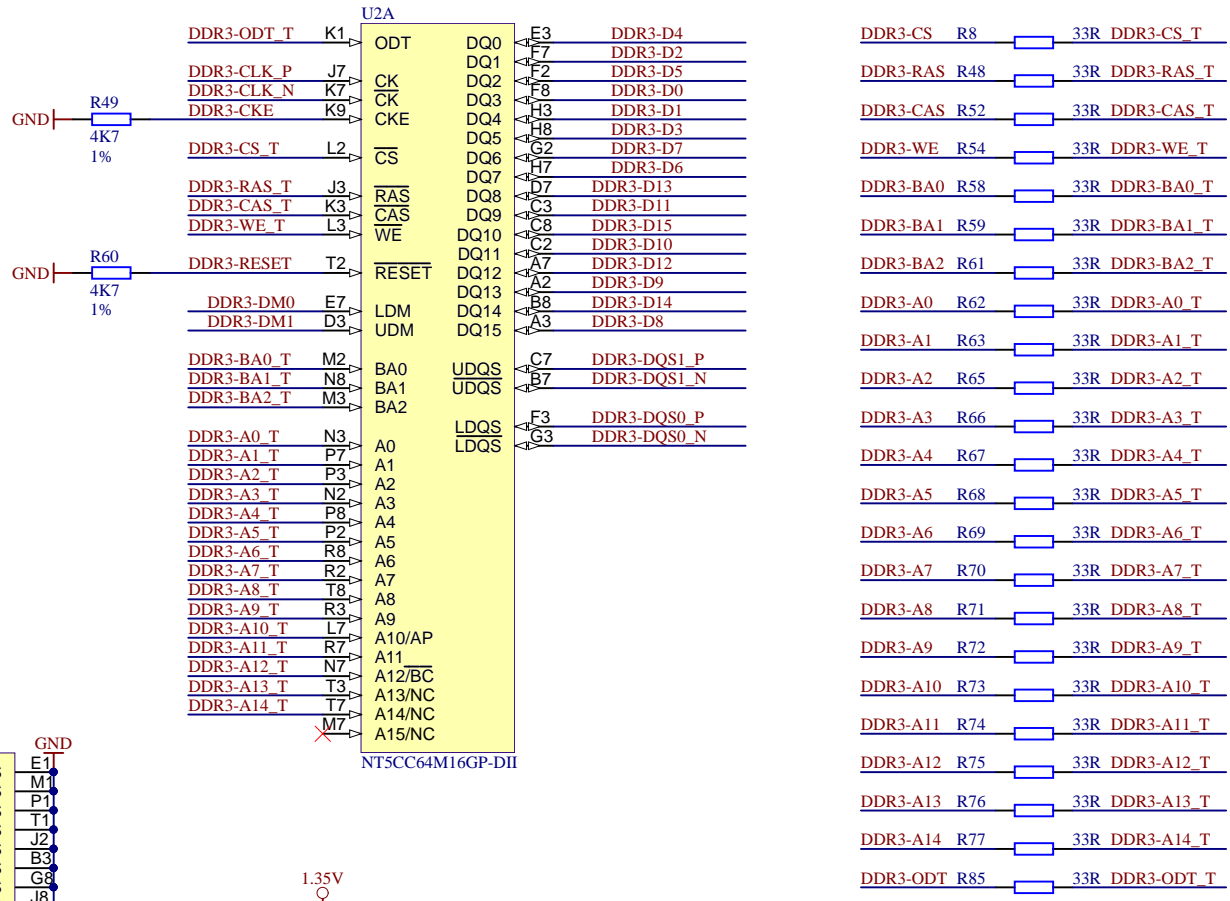
B

C

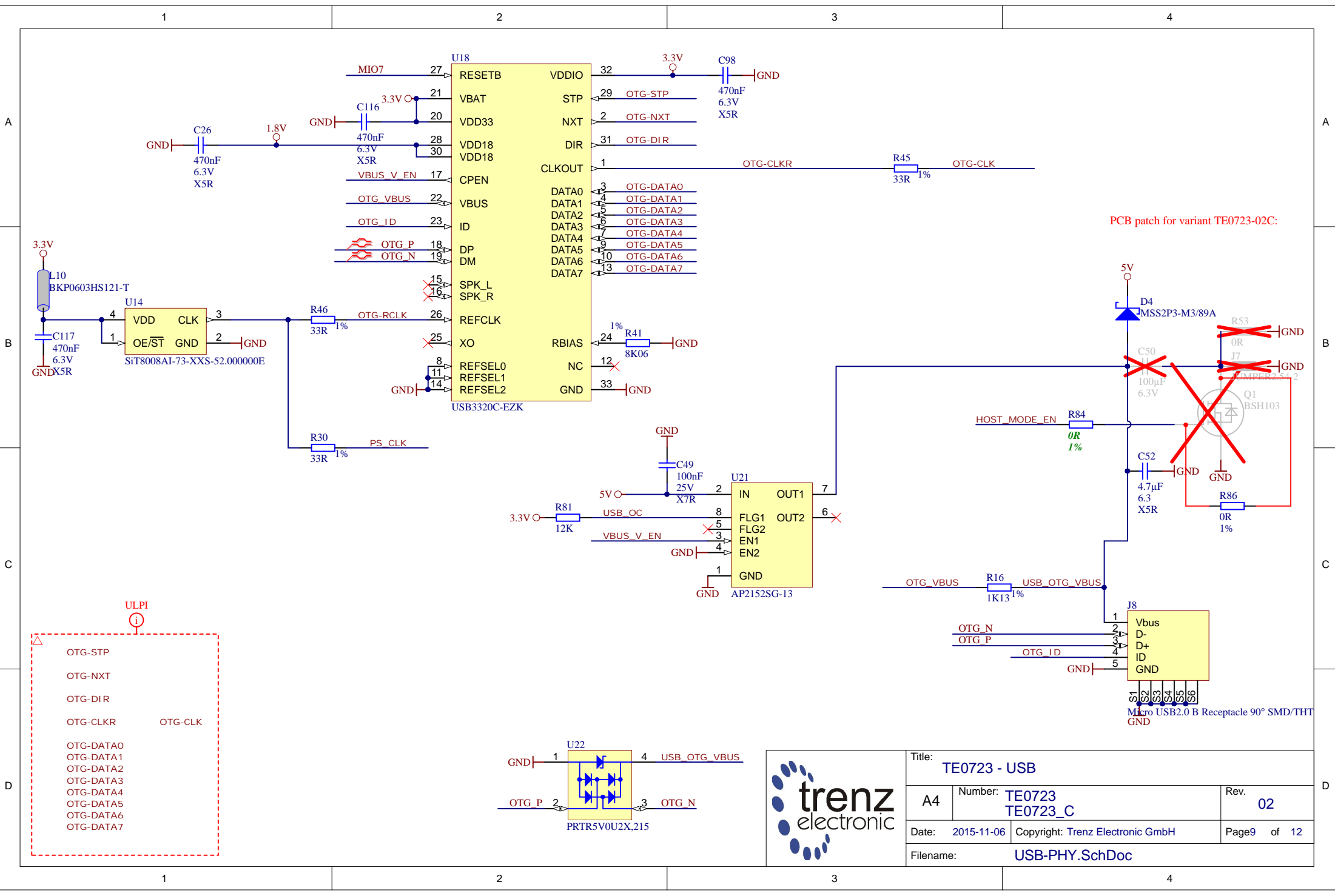
C

D

D



Title: TE0723 - DDR Memory		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page8 of 12
Filename: DDR3-RAM.SchDoc		



ULPI

OTG-STP

OTG-NXT

OTG-DIR

OTG-CLKR OTG-CLK

OTG-DATA0

OTG-DATA1

OTG-DATA2

OTG-DATA3

OTG-DATA4

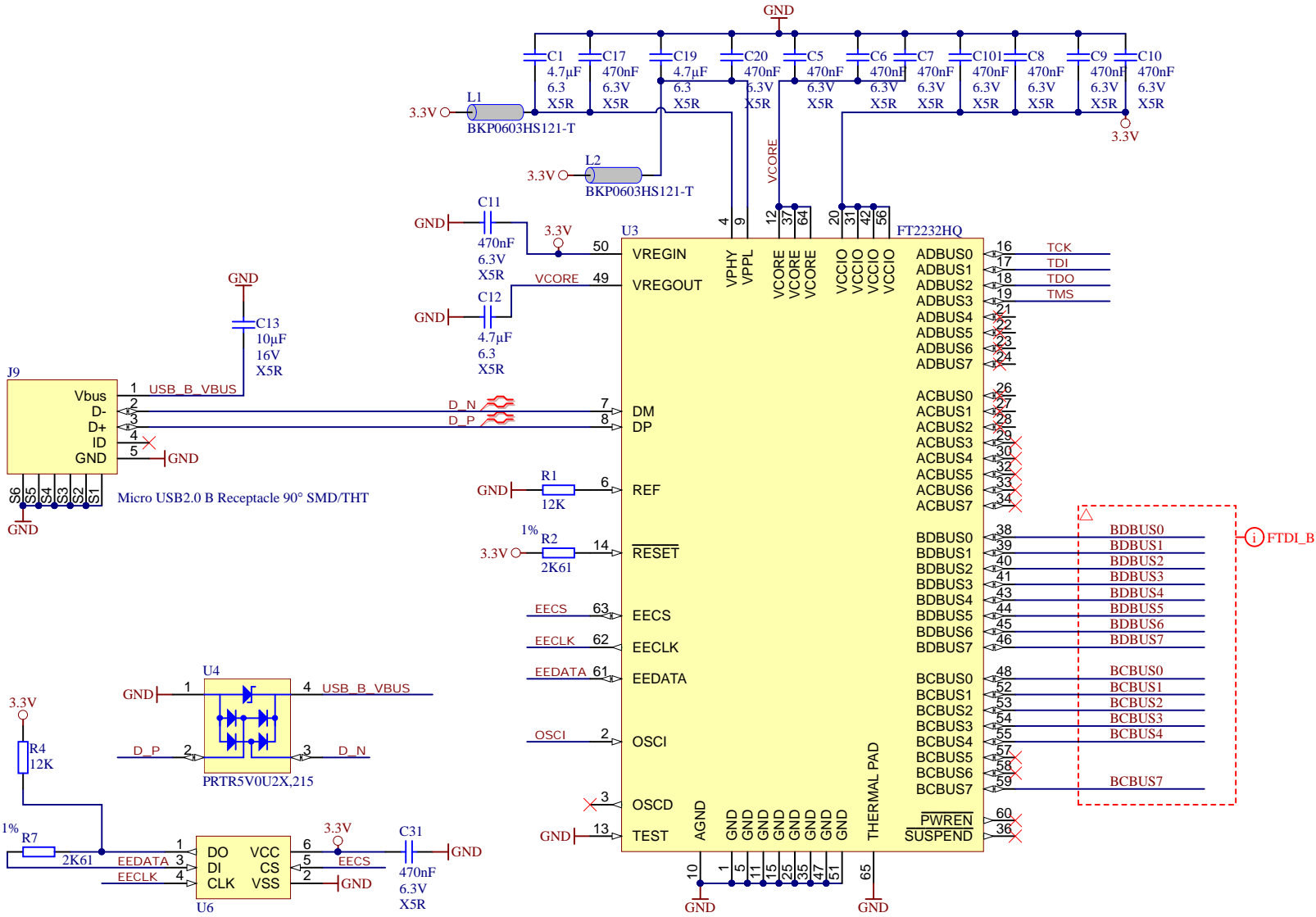
OTG-DATA5

OTG-DATA6

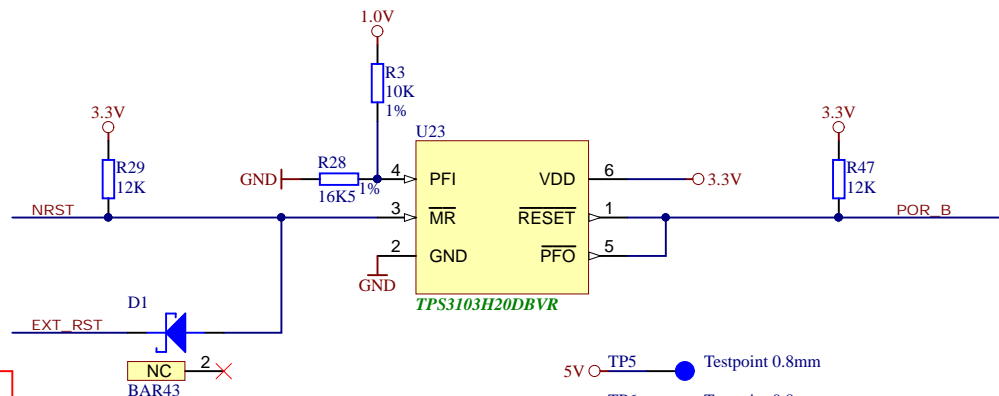
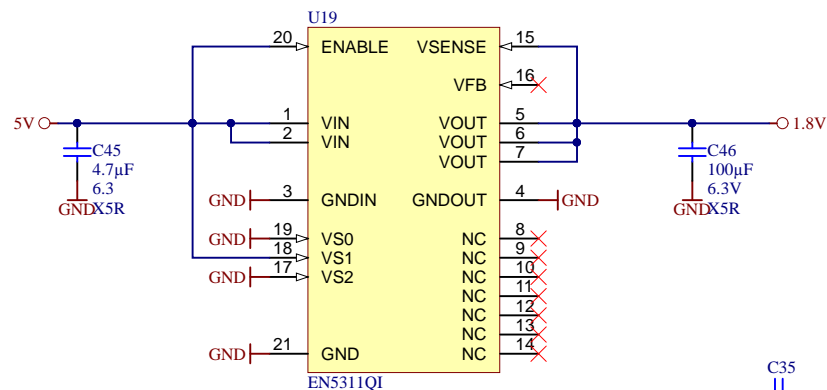
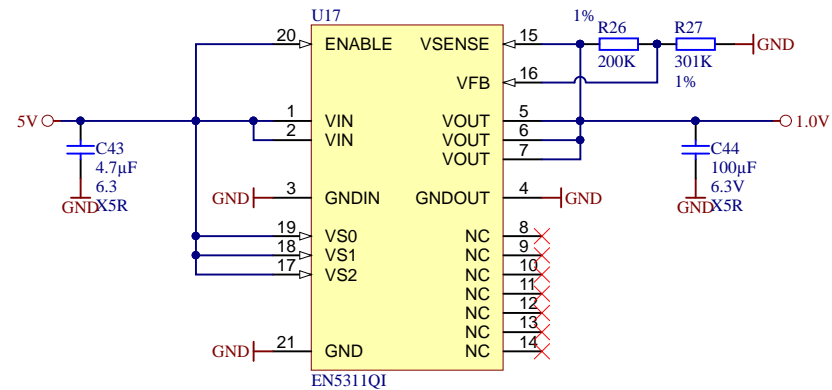
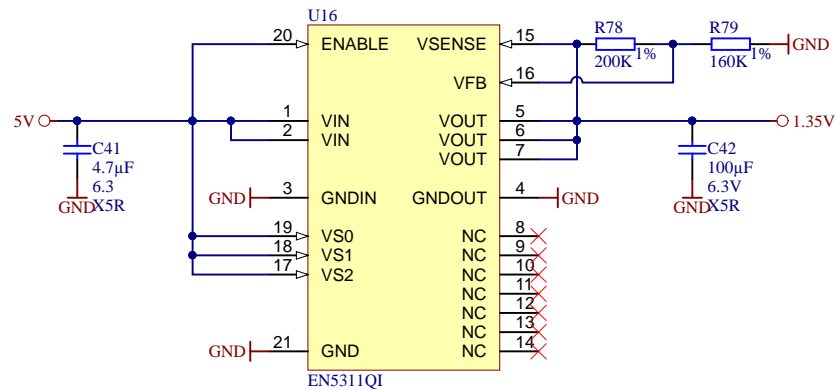
OTG-DATA7



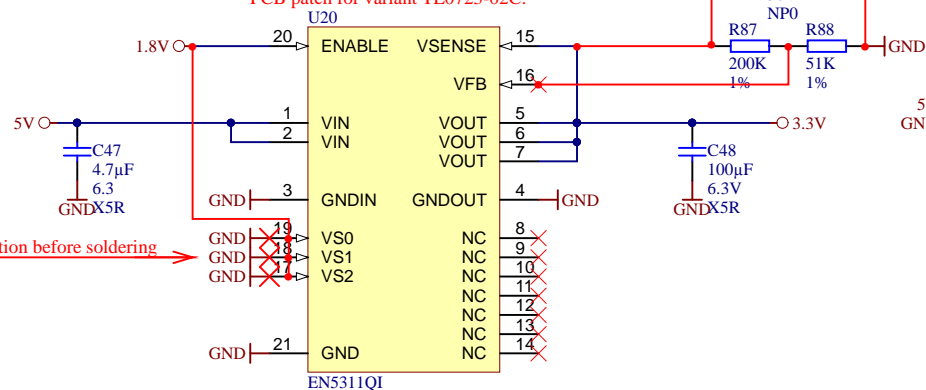
Title: TE0723 - USB		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page9 of 12
Filename: USB-PHY.SchDoc		



Title: TE0723 - FTDI		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page 10 of 12
Filename: FTDI.SchDoc		



PCB patch for variant TE0723-02C:



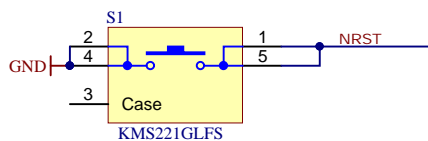
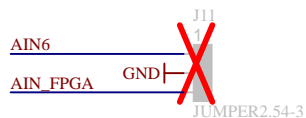
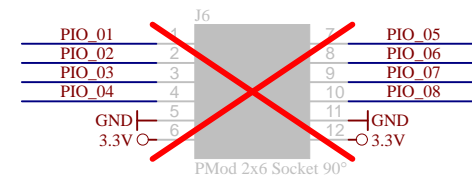
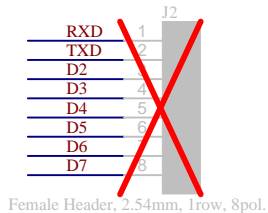
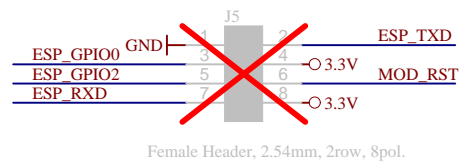
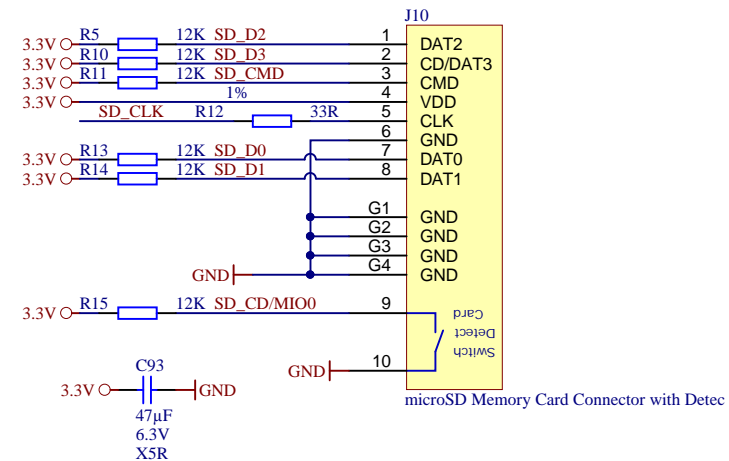
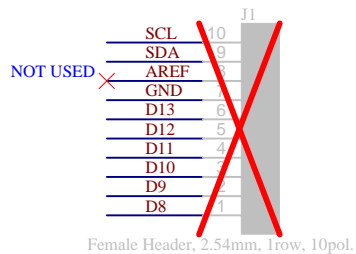
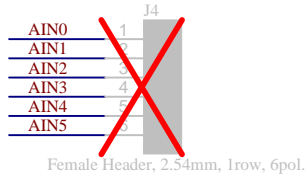
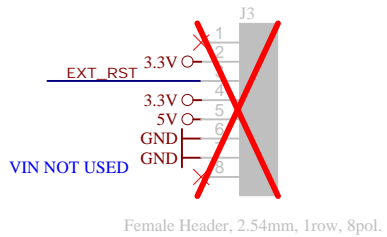
!!! Modification before soldering →



- 5V → TP5 ● Testpoint 0.8mm
- 3.3V → TP6 ● Testpoint 0.8mm
- 1.8V → TP7 ● Testpoint 0.8mm
- 1.35V → TP8 ● Testpoint 0.8mm
- 1.0V → TP9 ● Testpoint 0.8mm
- GND → TP10 ● Testpoint 0.8mm
- GND → TP11 ● Testpoint 0.8mm
- GND → TP12 ● Testpoint 0.8mm
- GND → TP13 ● Testpoint 0.8mm



Title: TE0723 - PowerSupply		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page 11 of 12
Filename: PowerSupply.SchDoc		



Title: TE0723 - Connectors		
A4	Number: TE0723 TE0723_C	Rev. 02
Date: 2015-11-06	Copyright: Trenz Electronic GmbH	Page 12 of 12
Filename: A-Headers.SchDoc		