



Regarding the usage of our schematics and alike documentation for Trenz module TE0726

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0726 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: Legal Notices Modules		
	A4	Number: TE0726 41194-A	Rev. 04
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH / TT	Page 1 of 18
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02	<ol style="list-style-type: none"> 1. CSI CLK line moved to MRCC pin, CSI lanes swap -> DONE 2. CSI camera GPIO moved to MIO GPIO -> DONE 3. RPi GPIO 14,15 moved from MIO to PL -> DONE 4. add C for SD Card VCC (required by SD spec) 47uF ->DONE 5. add C for RPi camera - prevent voltage drop at camera init - 47uF ? or R + 47uf ->DONE 6. fix MODE pin strapping -> DONE 7. LED change 0603 (cheaper) -> DONE 8. add POWER connector 2 pin -> DONE (2pin 2.54mm) 9. change HDMI ESD to ESD+EMI -> DONE (replaced on EMI4192) 10. fix HDMI HPD and backpower? how? -> fix reset 11. DSI find solution for LS mode 12. fix XADC power caps -> DONE 13. change LPDDR2 ->> DDR3L -> DONE 	
-03	<ol style="list-style-type: none"> 1. make variants: <ol style="list-style-type: none"> a) default with DDR3L 128Mb; b) TE0726-03M with DDR3L 512Mb; c) TE0726-03L with DDR3L 128Mb, without usb's, eth_phy, connectors usb, RJ-45, CSI,DSI,HDMI, jack 3.5mm -> done 2. replace FTDI on 56pins package -> done 3. move LED's as raspberry pi 3 -> done 4. replace POWER connector on right angle connector -> done (not fitted) 5. make corect conection PUDC pin -> done 6. optimize BOM, replace on cheaper components -> done (replace HDMI, DSI/CSI connector, USB stacked connectors, RJ-45, power connector) 	
-03a	<ol style="list-style-type: none"> 1. VBUS Resistor R94 replaced by 10k ohm (was 12k1) 	VY (08.04.2019)
-04	<ol style="list-style-type: none"> 1. EOL components U16, U17, U19, U20 (EN5311QI) were replaced by MPM3834CGPA; 2. Added MIC bias power L12, C114, R151 (Page 16); 3. Added Legal notices (Page 1); 4. Added power diagram (Page 4); 5. Added S1 switch and R152 for "JTAG only mode" enable (Page 8); 6. The signals were renamed: - SPI-DQ0/M0 ----> SPI-DQ0/M3, - SPI-DQ3/M3 ----> SPI-DQ3/M0 according to AMD Table 6-4 (Page 8); 7. ECC function has been added for U8 (Page 11); 7.1 Added I2C level shifter U12 for DDR3 ECC function (Page 11); 7.2 Added Buffers U24, U25 to match the level of signals (Page 6); 7.3. Added Diode D7, resistors R155, R160. 8. EOL components L1, L2, L3, L4, L6, L7, L9, L10 BKP0603HS121-T replaced by MPZ0603S121HT000. 9. EOL components D8, D9 SP5001-04TTG replaced by EM18042MUTAG. 10. Resistors R80-R82 replaced by 10k ohm (was 1k43). 11. Added Testpoints TP15 - TP20. 12. The type of testpoints TP1 - TP14 was updated. Diameter changed from 0.8 mm to 1 mm. 13. CEC function is not supported. L11 was removed. C127, D5, R140, R42 are DNP. 14. Power-up sequencing was updated for new DC-DC supplies. 15. Capacitors C29, C32, C33 replaced by 470nF (was 100nF). 	VG (06.10.2023)

	Title: Revision_Changes		
	A4	Number: TE0726 41194-A	Rev. 04
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page2 of 18
	Filename: Revision_Changes.SchDoc		

1

2

3

4

A

A

B

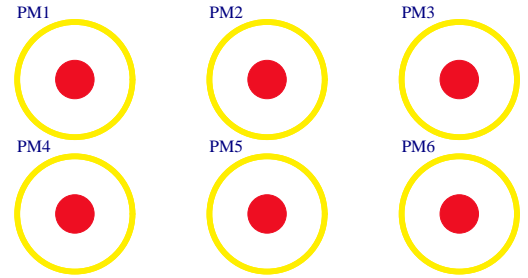
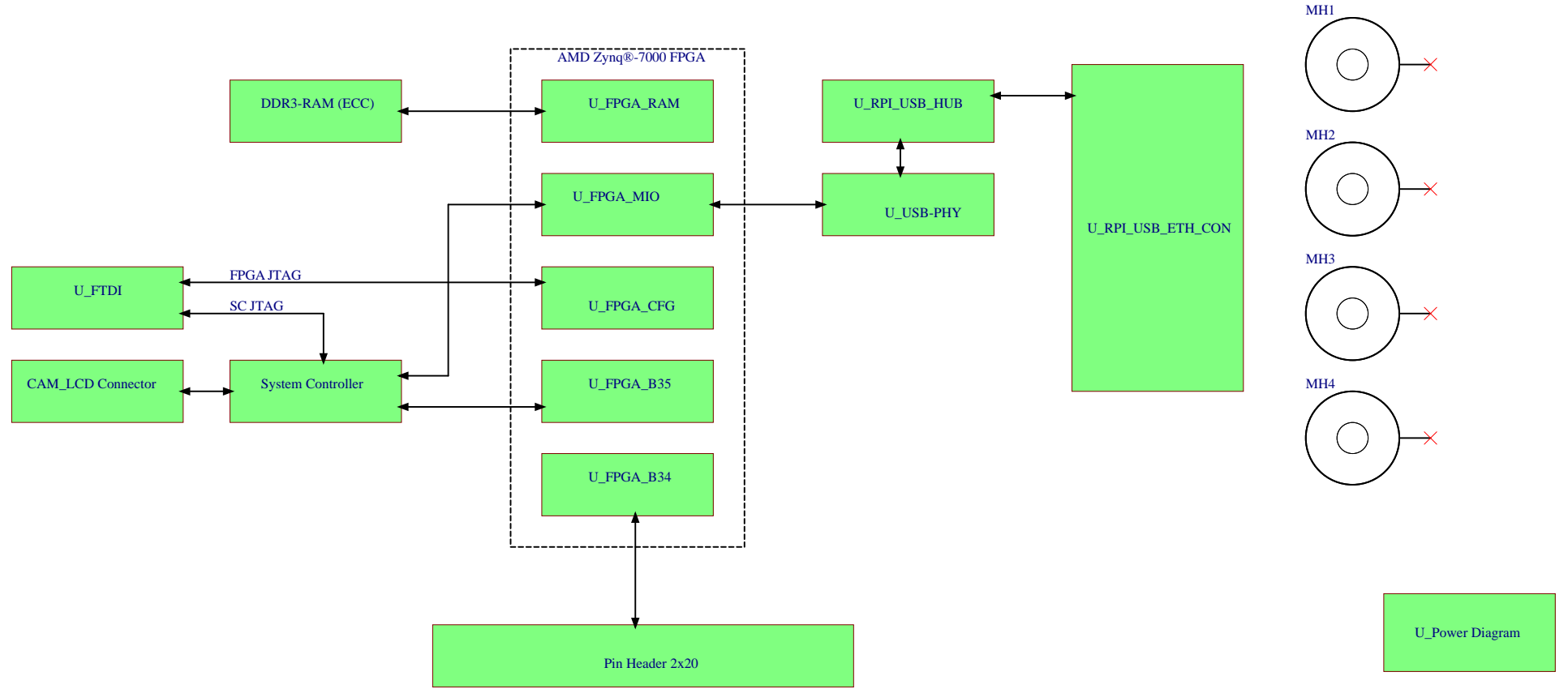
B

C

C

D

D



Serial
 Serialnumber 6,3 x 6.3mm

MECH1
 TE Address Overlay
 LOGO ADDRESS

UKCA
 UKCA Logo on Top Overlay
 UKCA-TOOVERLAY

LOGO1
 TE Logo PRINT Layer
 LOGO PRINT

CE
 CE Logo on Top Overlay
 CE-TOOVERLAY

Drawn by	VG
Checked by	IG
Assembly variant	41194-A
Created by	VG
Modified by	VG
Modified at	2023-09-28



Title: Overview		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 3 of 18
Filename: TE0726.SchDoc		

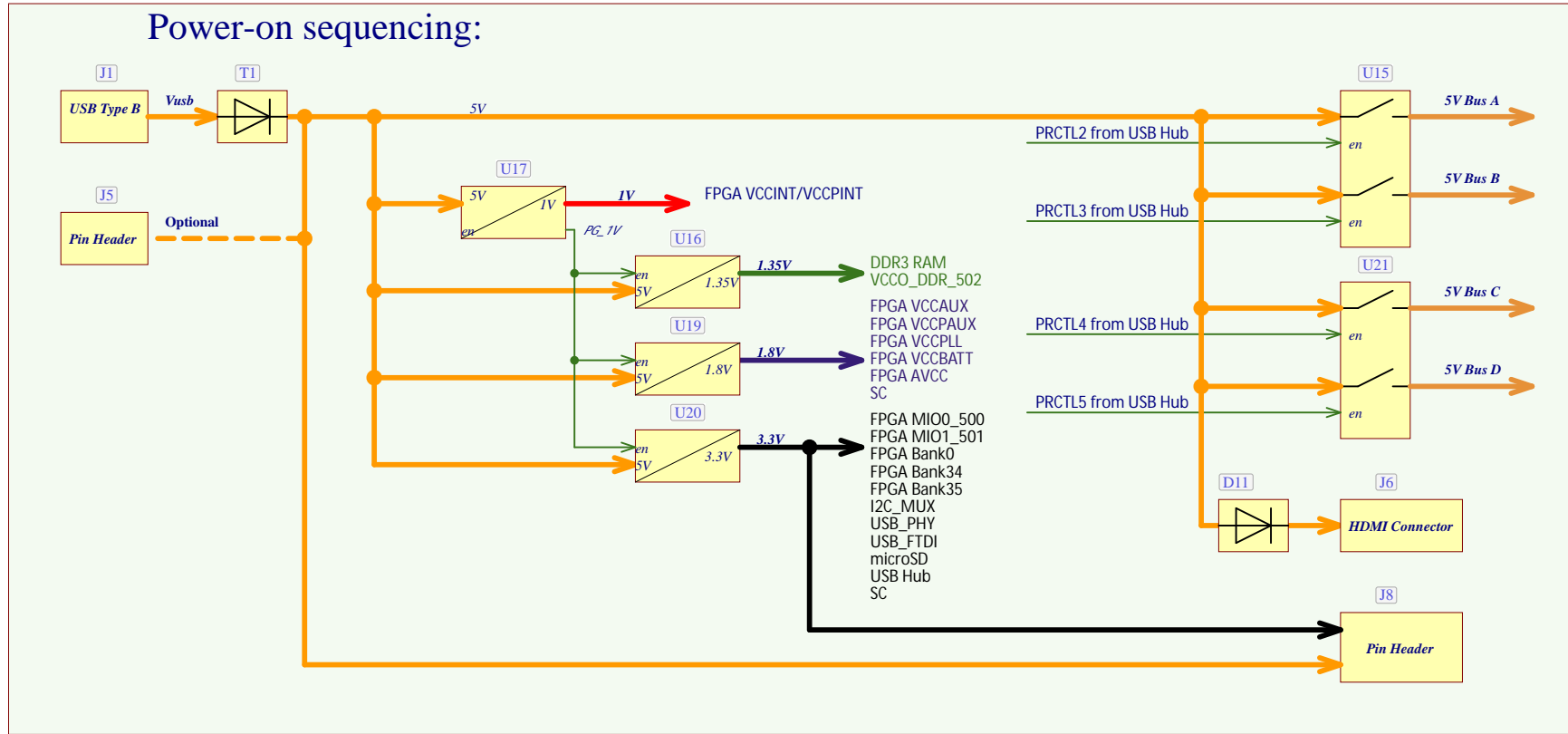
1

2

3

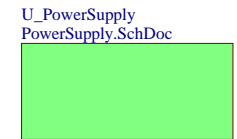
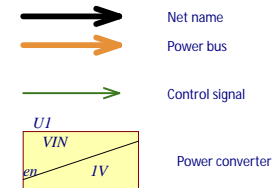
4

Power-on sequencing:

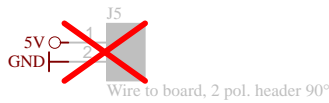
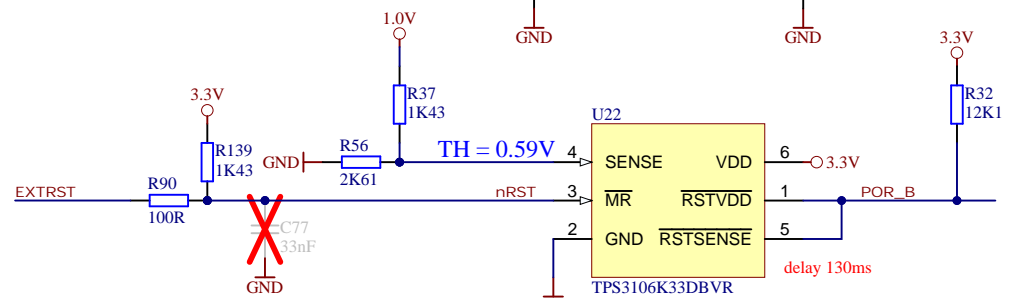
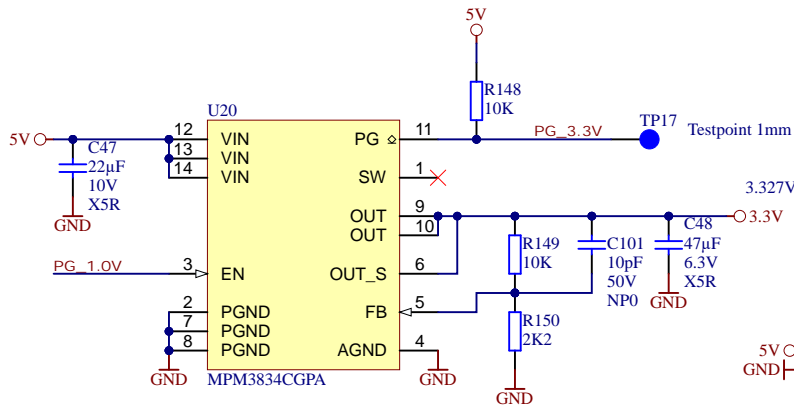
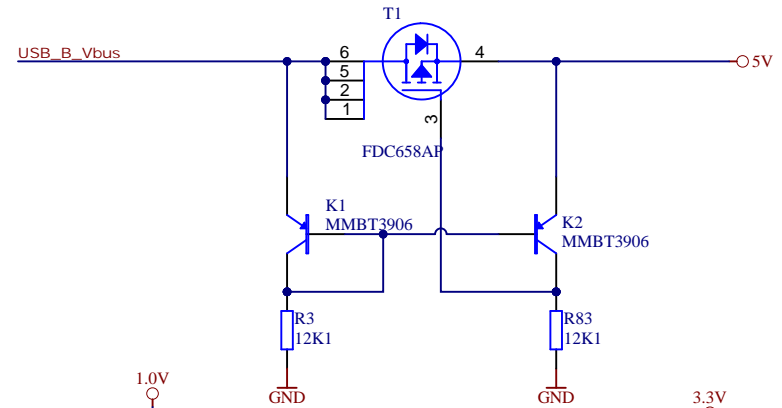
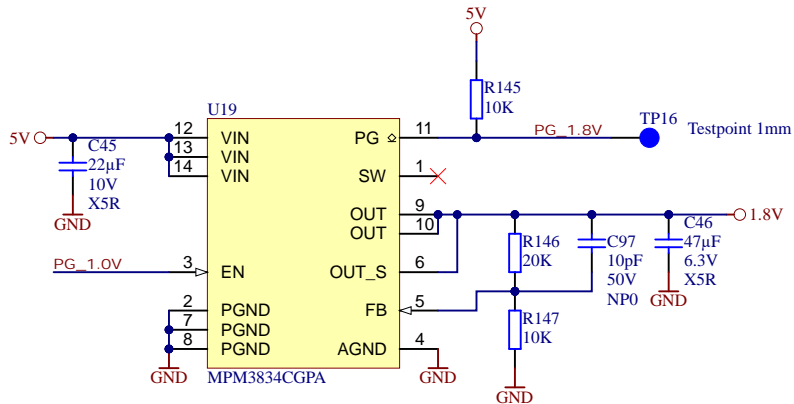
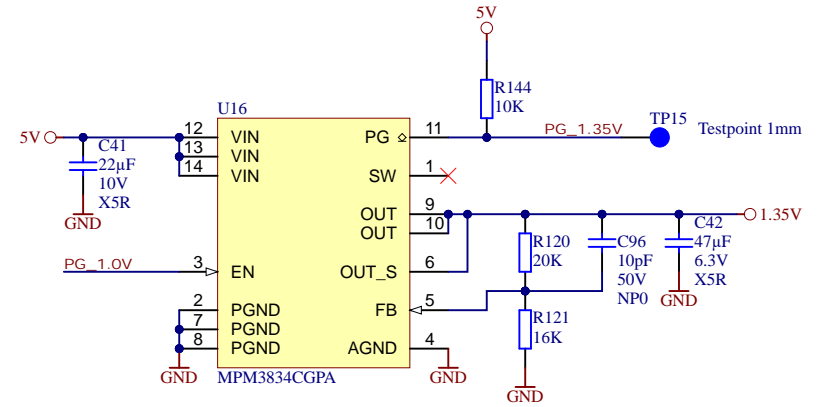
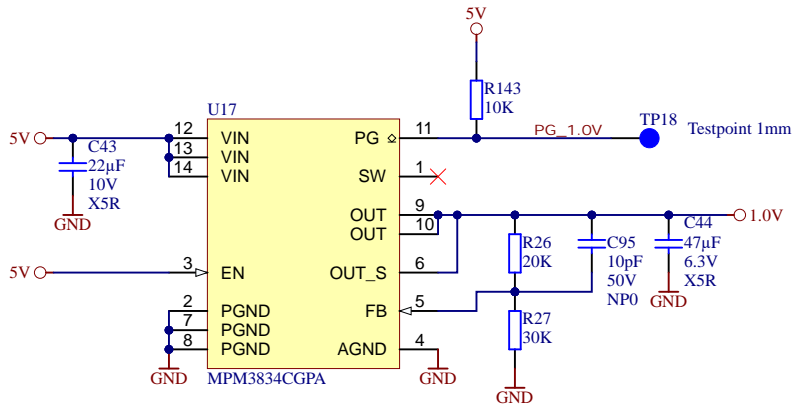


Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V	OUT	5V	+/-5%	Micromodule Power	-
USB_B_Vbus	IN	5V	+/-5%	Micromodule Power	-
3.3V	OUT	3.3V	+/-3%	Micromodule Power	-



Title: Power_Diagram		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 4 of 18
Filename: Power_Diagram.SchDoc		

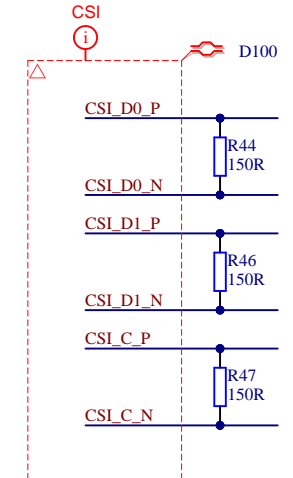
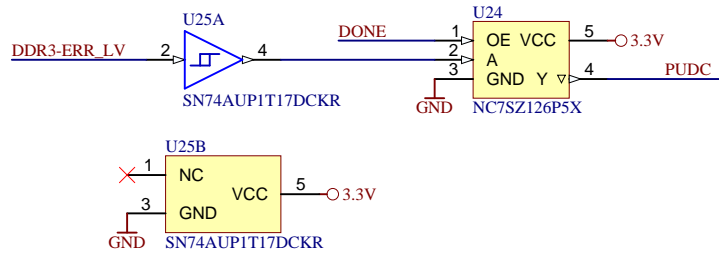
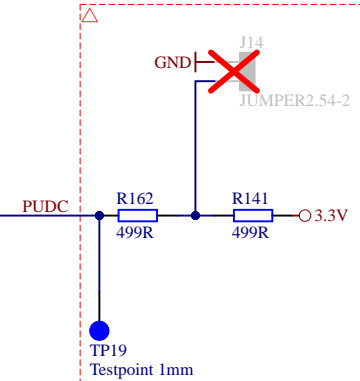


			Title: PowerSupply	
			A4	Number: TE0726 41194-A
Date: 30.06.2023		Copyright: Trenz Electronic GmbH		Rev. 04
Filename: PowerSupply.SchDoc			Page 5 of 18	

BANK 34

- IO_L1P_T0_34
- IO_L1N_T0_34
- IO_L2P_T0_34
- IO_L2N_T0_34
- IO_L3P_T0_DQS_PUDC_B_34
- IO_L3N_T0_DQS_34
- IO_L4P_T0_34
- IO_L4N_T0_34
- IO_L5P_T0_34
- IO_L5N_T0_34
- IO_L6P_T0_34
- IO_L6N_T0_VREF_34
- IO_L7P_T1_34
- IO_L7N_T1_34
- IO_L8P_T1_34
- IO_L8N_T1_34
- IO_L9P_T1_DQS_34
- IO_L9N_T1_DQS_34
- IO_L10P_T1_34
- IO_L10N_T1_34
- IO_L11P_T1_SRCC_34
- IO_L11N_T1_SRCC_34
- IO_L12P_T1_MRCC_34
- IO_L12N_T1_MRCC_34
- IO_L13P_T2_MRCC_34
- IO_L13N_T2_MRCC_34
- IO_L15P_T2_DQS_34
- IO_L15N_T2_DQS_34
- IO_L16P_T2_34
- IO_L16N_T2_34
- IO_L17P_T2_34
- IO_L17N_T2_34
- IO_L18P_T2_34
- IO_L18N_T2_34
- IO_L19P_T3_34
- IO_L19N_T3_VREF_34
- IO_L20P_T3_34
- IO_L20N_T3_34
- IO_L21P_T3_DQS_34
- IO_L21N_T3_DQS_34
- IO_L22P_T3_34
- IO_L22N_T3_34
- IO_L23P_T3_34
- IO_L23N_T3_34
- IO_L24P_T3_34
- IO_L24N_T3_34

- G11 GPIO17
- H12 GPIO4
- G12 GPIO27
- H13 GPIO22
- G14
- H14 GPIO10
- J15 GPIO11
- K15 GPIO2
- J13 GPIO9
- J14 GPIO3
- H11 GPIO18
- J11 GPIO23
- N13 GPIO15
- N14 GPIO5
- L15 GPIO8
- M15 GPIO12
- L14 GPIO7
- M14 GPIO20
- K13 GPIO25
- L13 GPIO16
- K11 GPIO24
- K12
- L12 GPIO26
- M12 GPIO14
- N11
- N12
- P15 GPIO21
- R15 GPIO6
- P11
- R11
- R12 GPIO19
- R13 GPIO13
- P13
- P14
- M9
- N9
- R7
- R8
- M10
- M11
- N7
- N8
- P8
- P9
- P10
- R10



XC7Z010-1CLG225I



Title: FPGA B34		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page6 of 18
Filename: FPGA_B34.SchDoc		

1

2

3

4

A

A

B

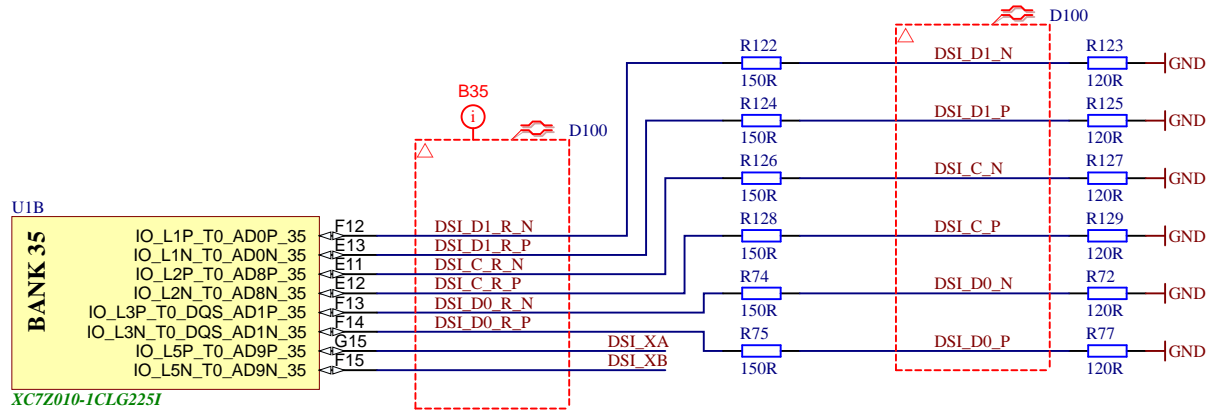
B


C

C

D

D



	Title: FPGA B35		
	A4	Number: TE0726 41194-A	Rev. 04
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 7 of 18
	Filename: FPGA_B35.SchDoc		

1

2

3

4

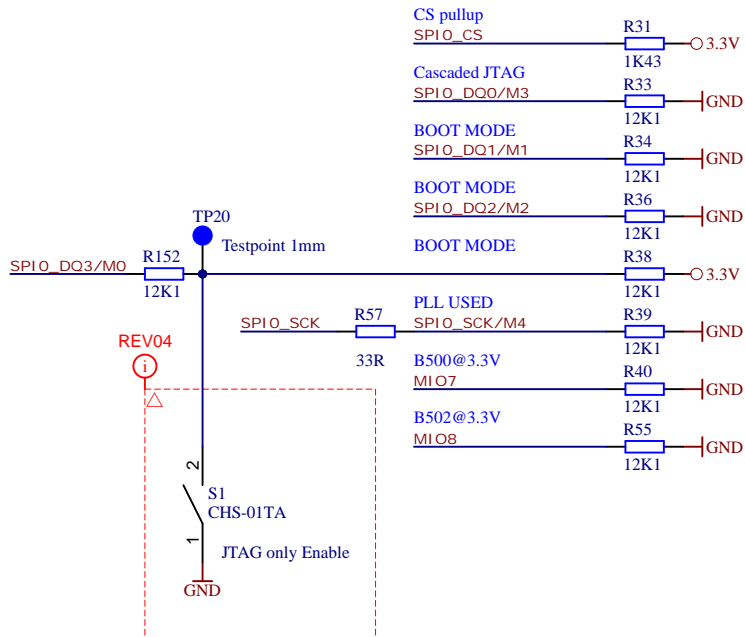
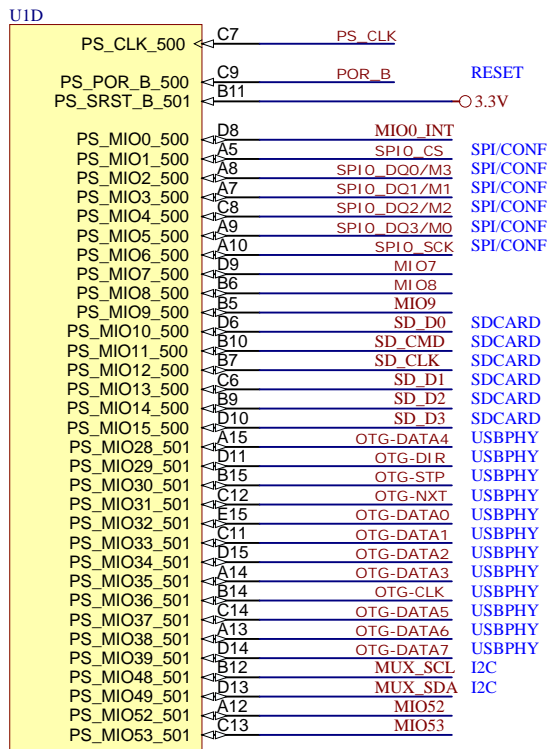
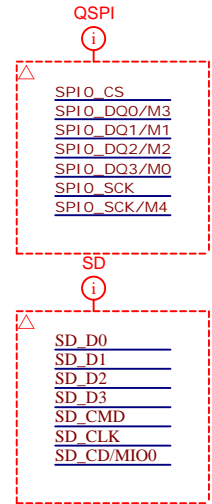
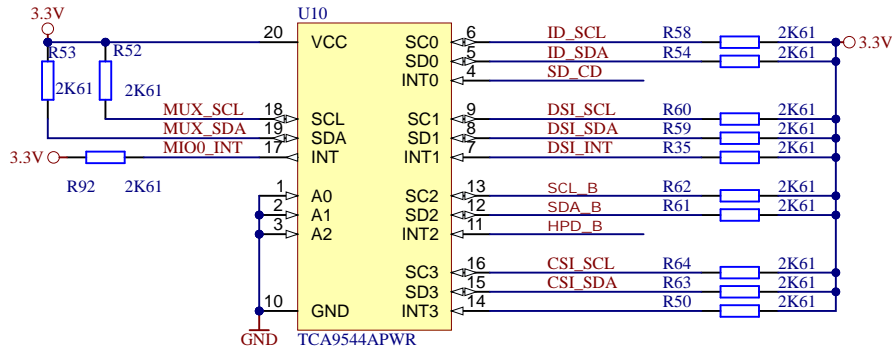
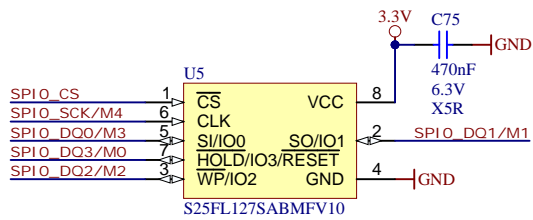


Table 6-4: Boot Mode MIO Strapping Pins

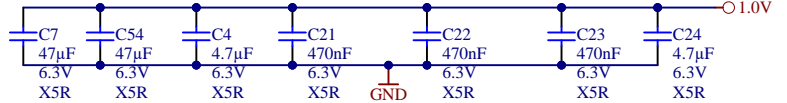
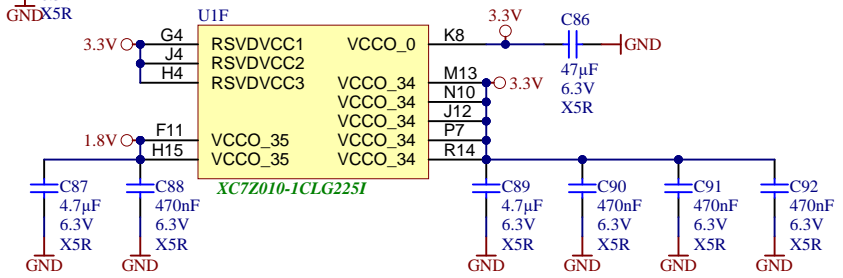
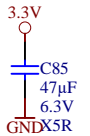
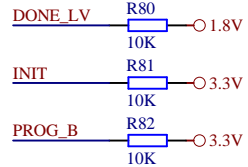
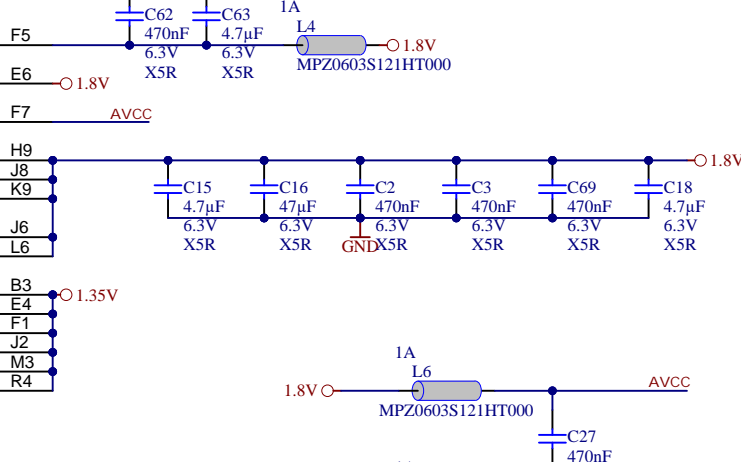
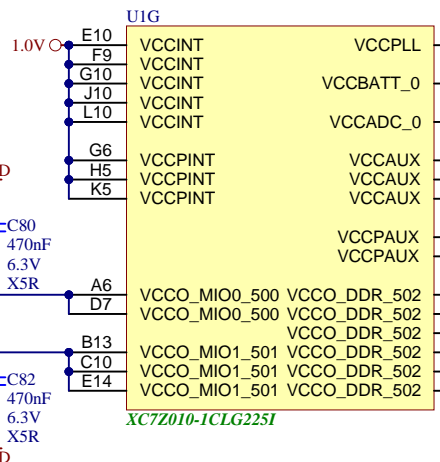
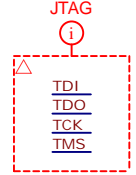
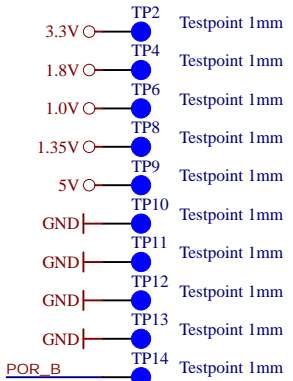
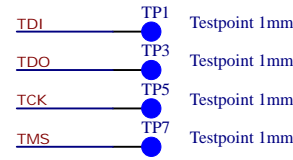
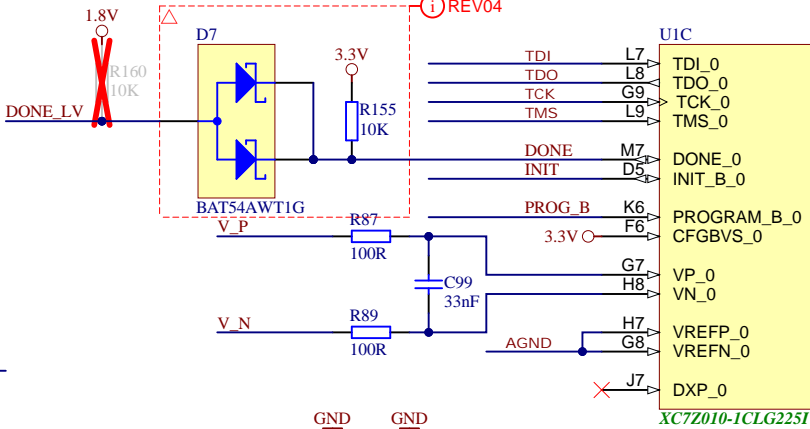
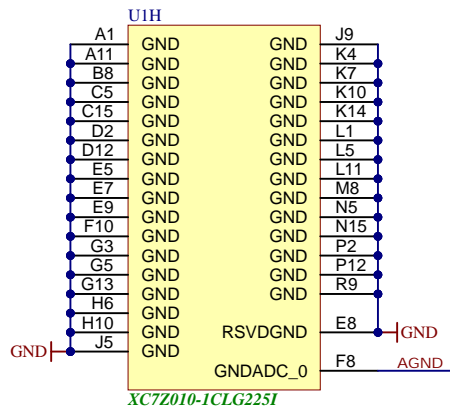
Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common ⁽¹⁾		0		0		0	
NOR Boot ⁽³⁾		0		0		1	
NAND		0		1		0	
Quad-SPI ⁽³⁾		1		0		0	
SD Card		1		1		0	

0: Cascade mode
1: Independent mode

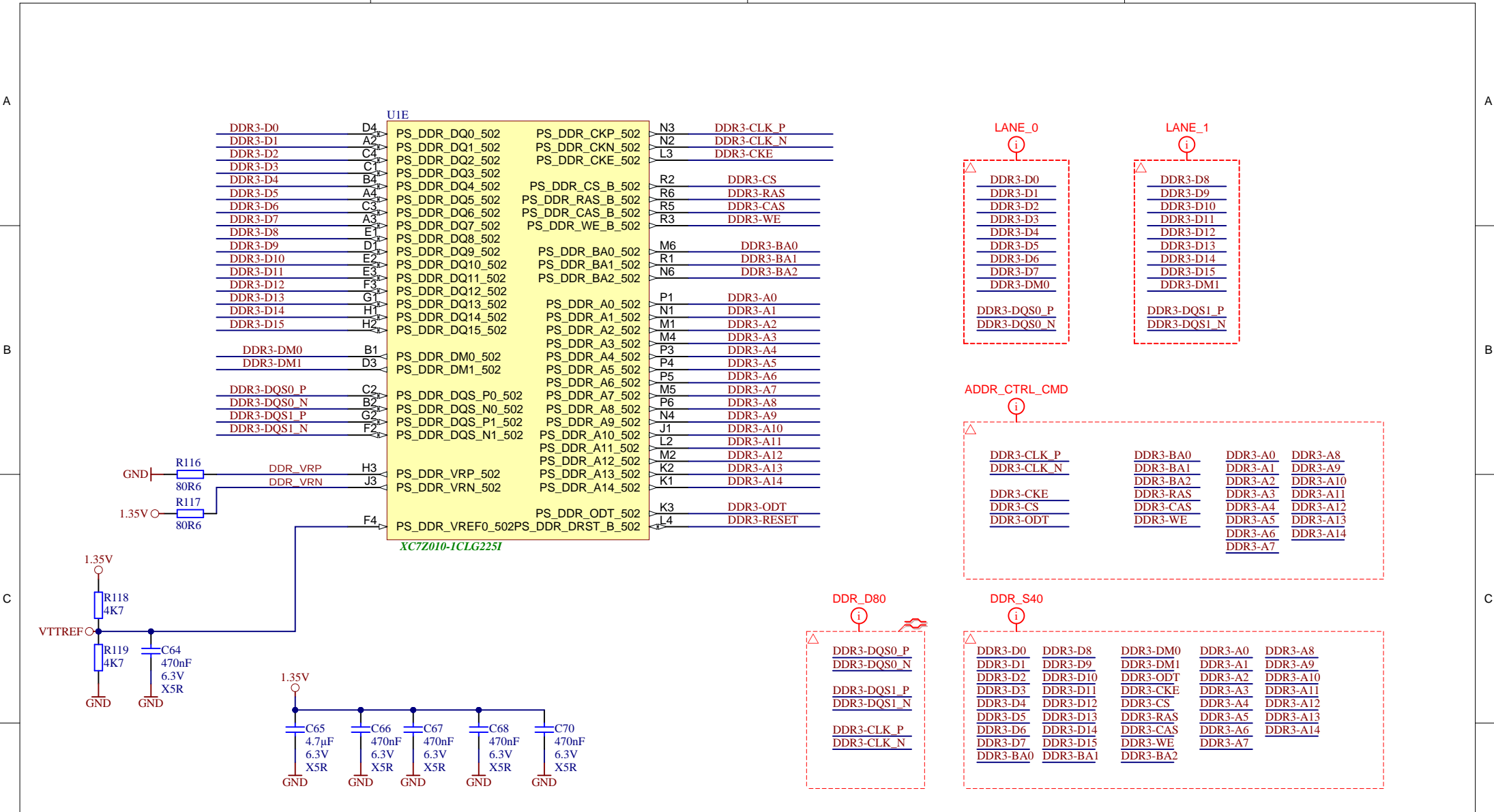
Title: **FPGA MIO**

A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 8 of 18
Filename: FPGA_MIO.SchDoc		

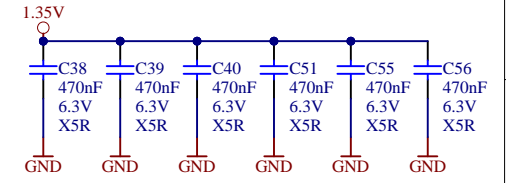
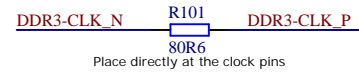
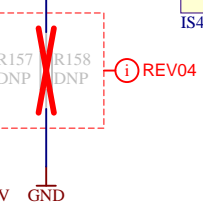
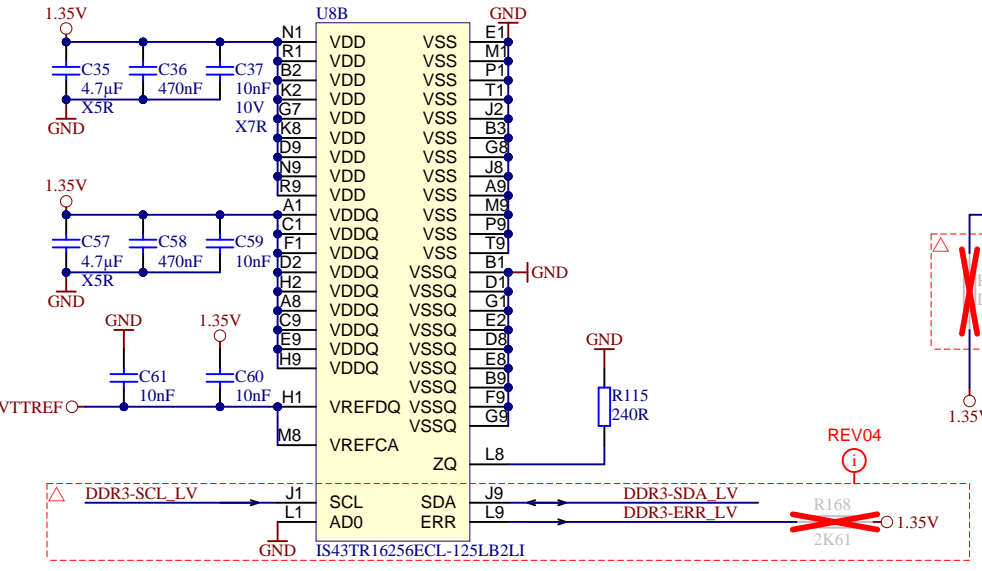
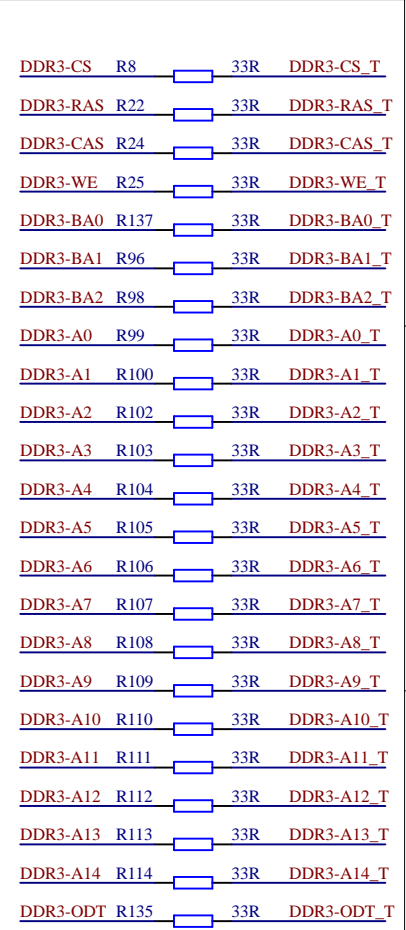
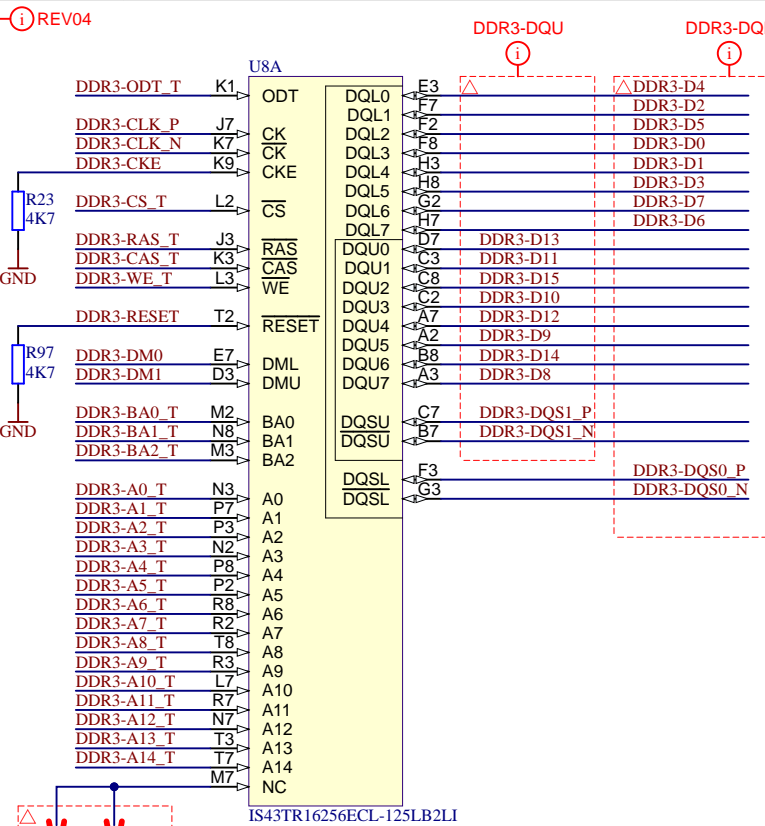
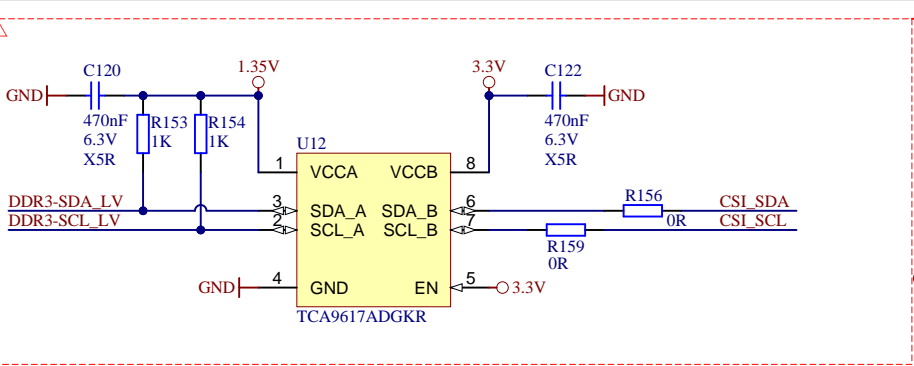
XC7Z010-1CLG225I



Title: FPGA PWR		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 9 of 18
Filename: FPGA_CFG.SchDoc		



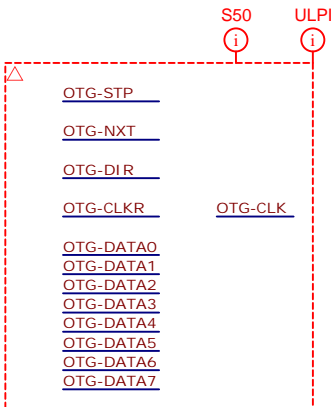
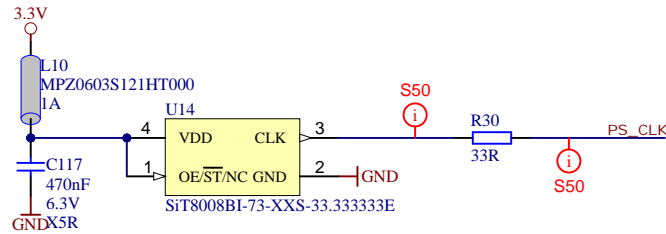
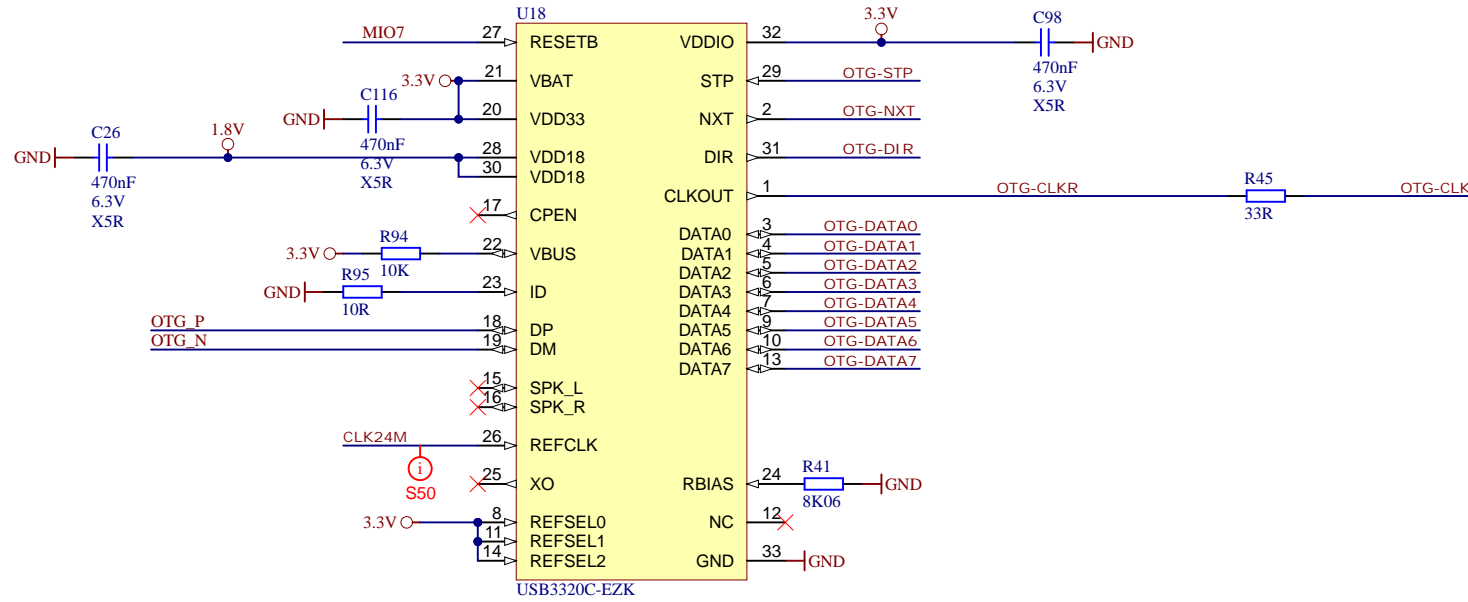
	Title: FPGA RAM		
	A4	Number: TE0726 41194-A	Rev. 04
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 10 of 18
	Filename: FPGA_RAM.SchDoc		



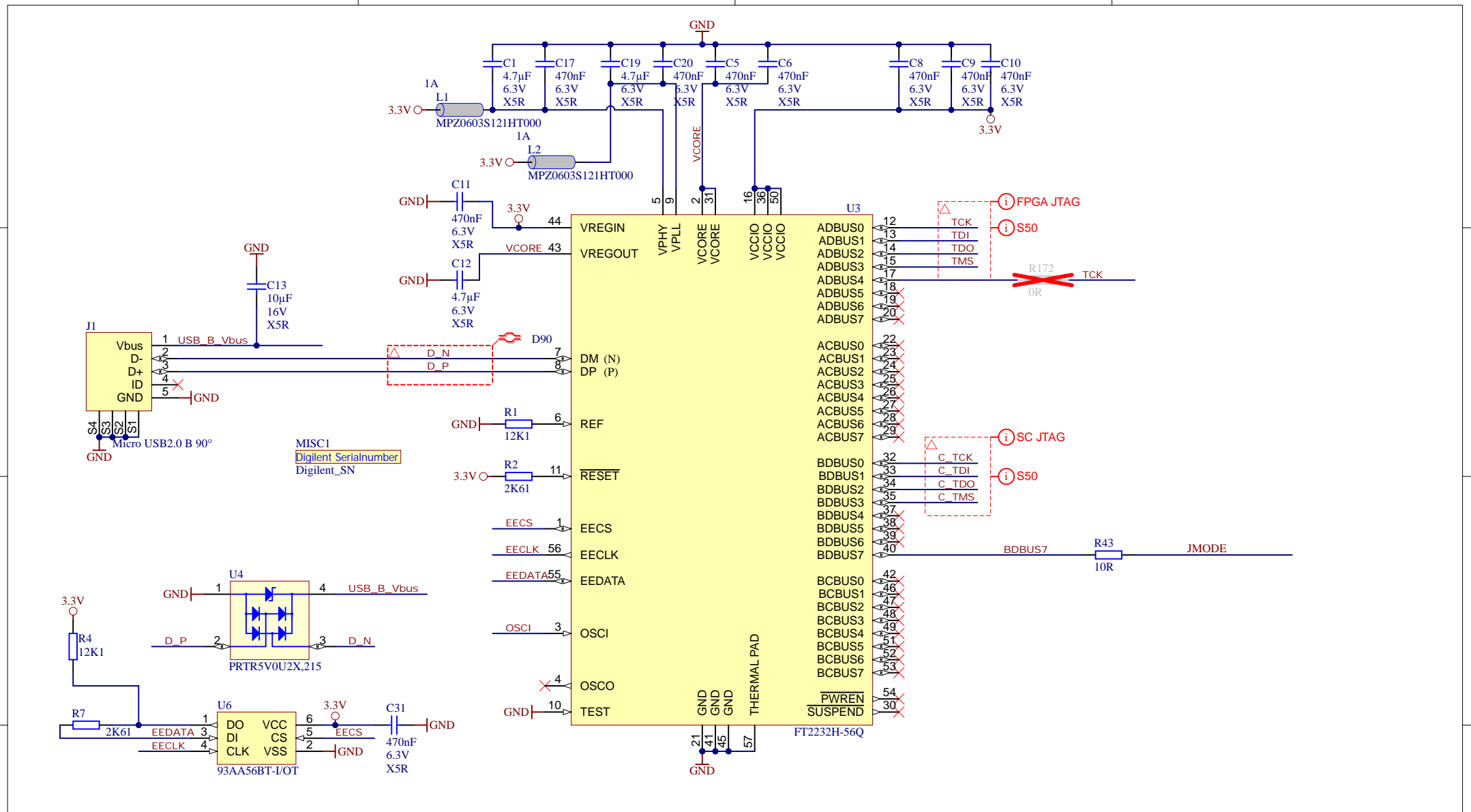
I2C Address: 0x18



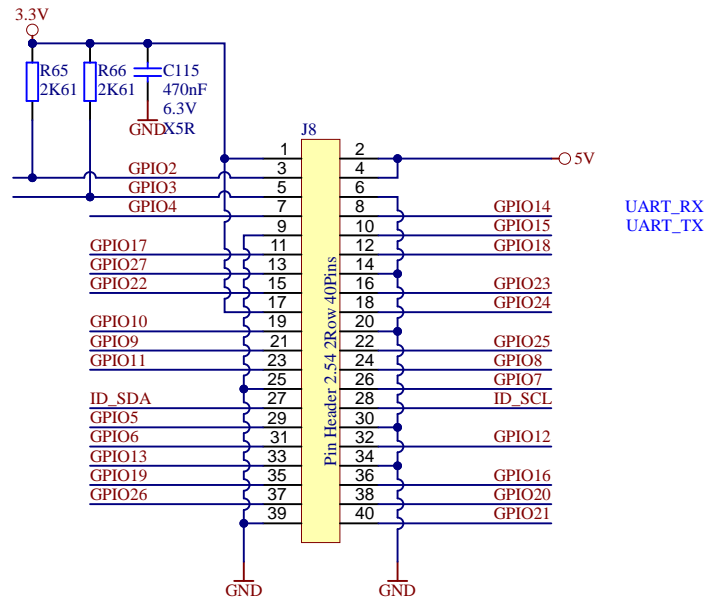
Title: DDR Memory		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 11 of 18
Filename: DDR3-RAM.SchDoc		



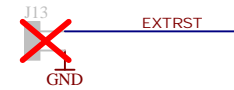
Title: USB		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 12 of 18
Filename: USB-PHY.SchDoc		



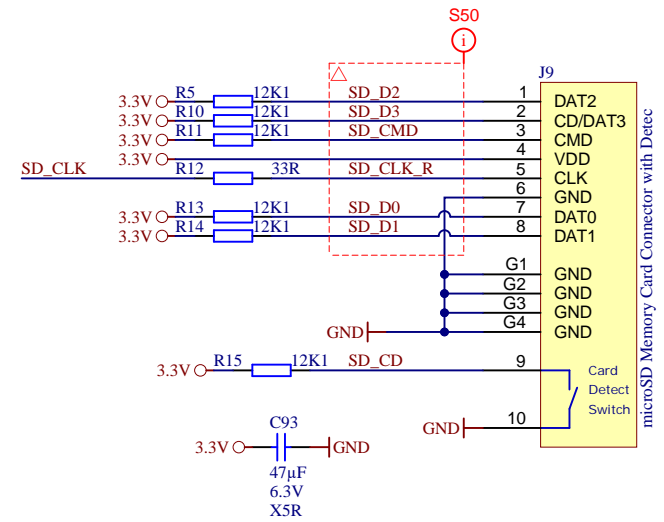
Title: FTDI		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 13 of 18
Filename: FTDI.SchDoc		




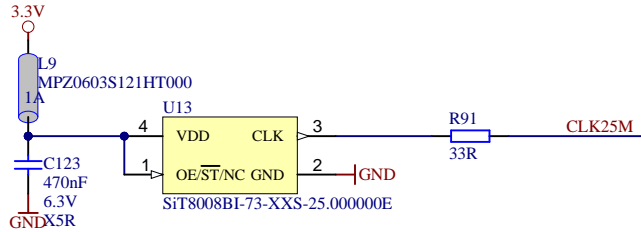
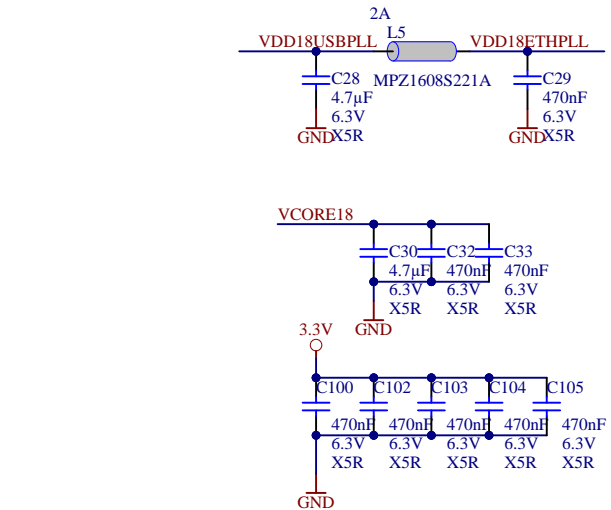
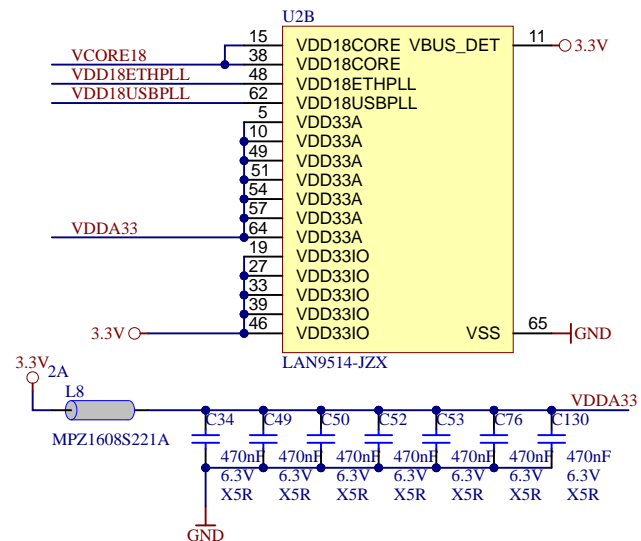
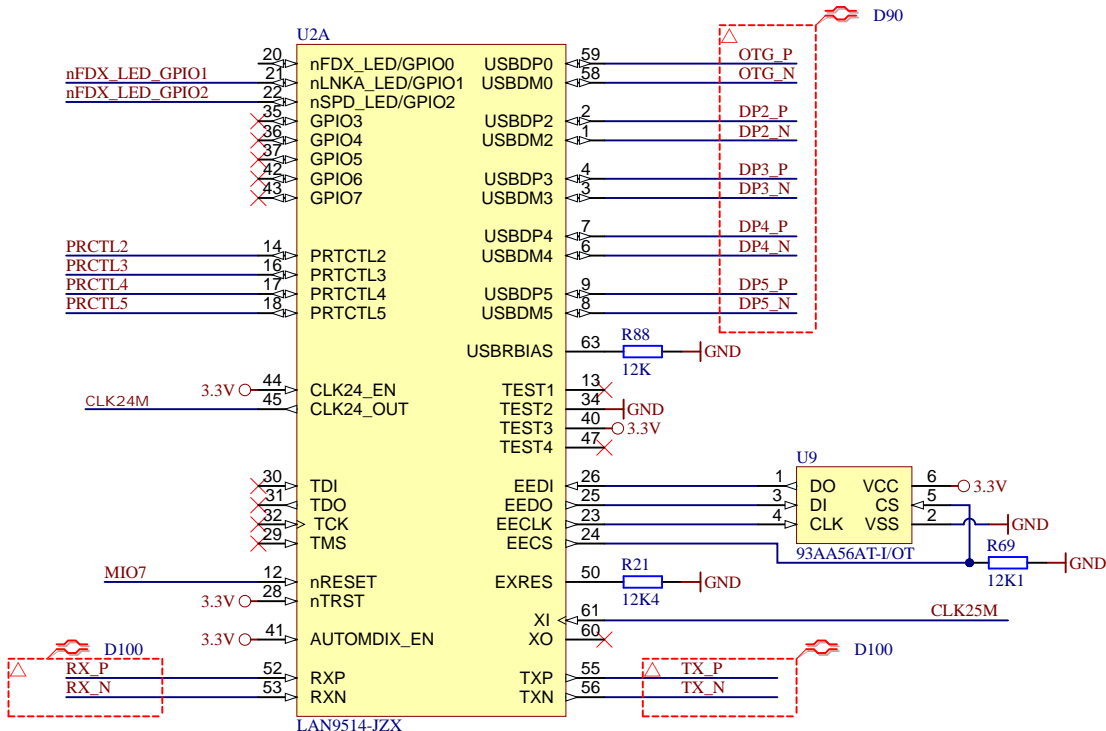
UART_RX
UART_TX



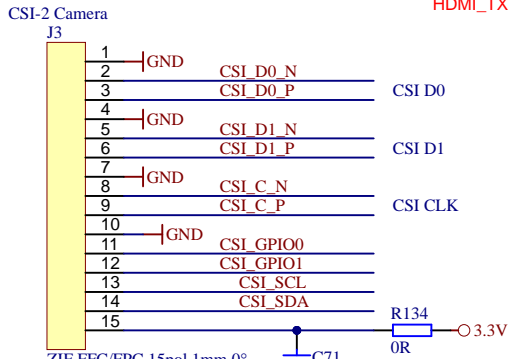
JUMPER2.54-2



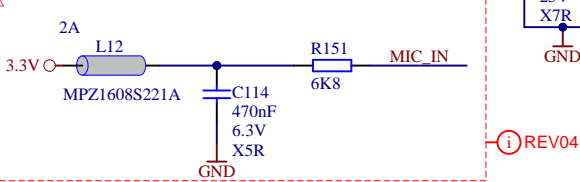
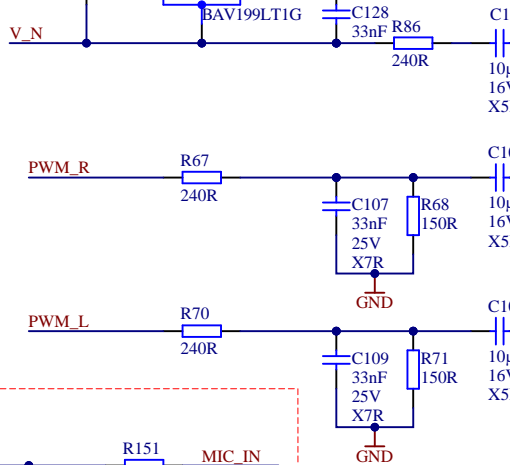
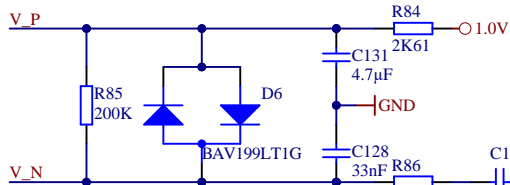
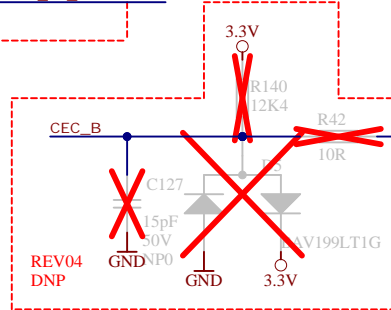
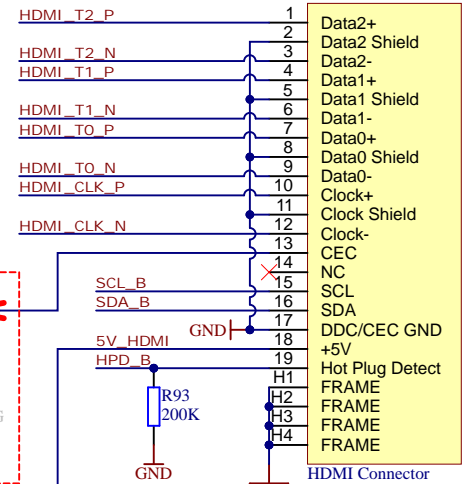
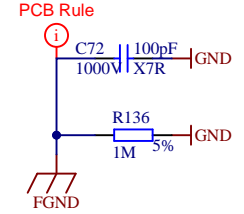
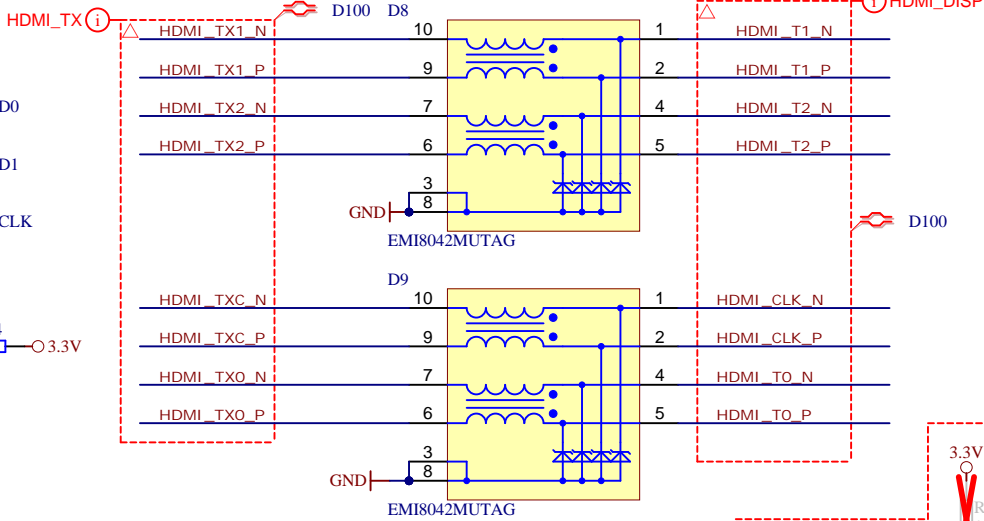
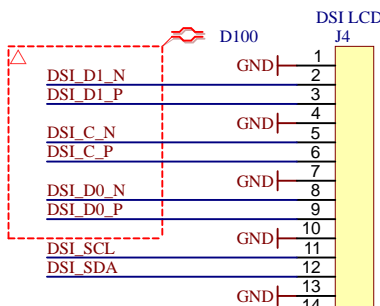
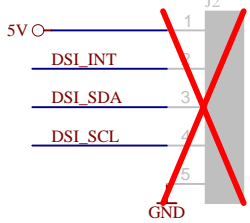
			Title: Connectors	
			A4	Number: TE0726 41194-A
Date: 2023-03-20		Copyright: Trenz Electronic GmbH		Page 14 of 18
Filename: RPi-Headers.SchDoc				



	Title: Connectors		
	A4	Number: TE0726 41194-A	Rev. 04
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page 15 of 18
	Filename: RPi-USB-HUB.SchDoc		



CSI Camera: 0x64
CSI Camera sensor: 0x10



Title: Connectors		
A4	Number: TE0726 41194-A	Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH	Page16 of 18
Filename: RPi-CAM-LCD.SchDoc		

1

2

3

4

A

A

B

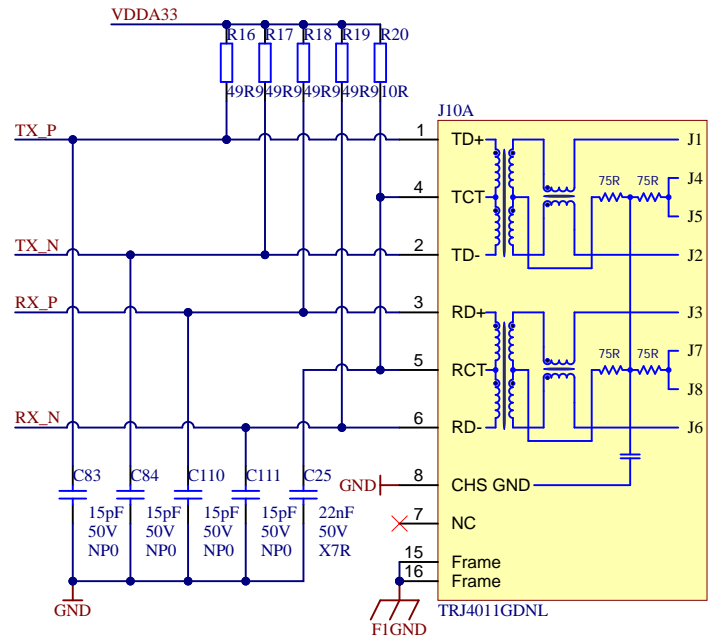
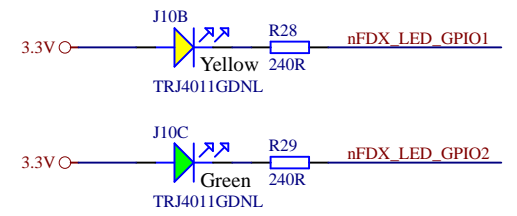
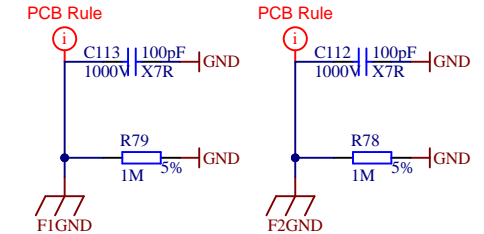
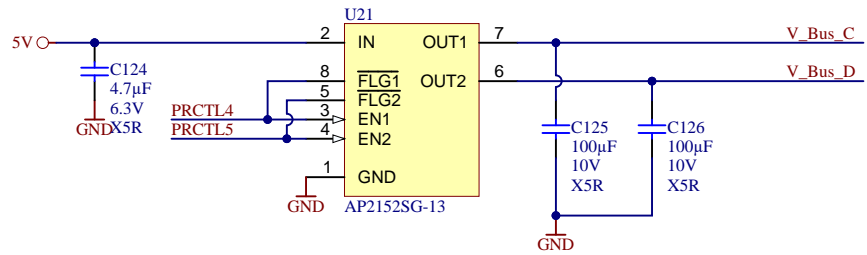
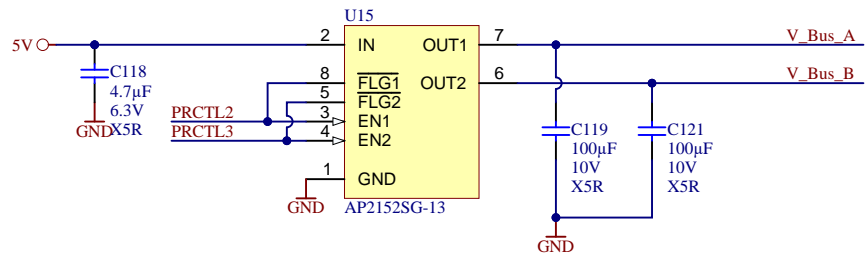
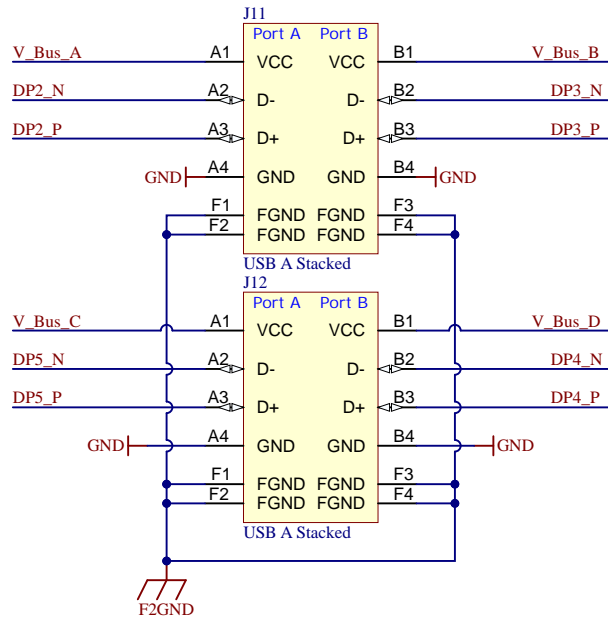
B

C

C

D

D



	Title: USB ETHERNET	
	A4	Number: TE0726 41194-A
	Date: 2023-03-20	Copyright: Trenz Electronic GmbH
	Filename: PRI-USB-ETH-CON.SchDoc	
	Rev. 04	Page 17 of 18

1

2

3

4

1

2

3

4

A

A

B

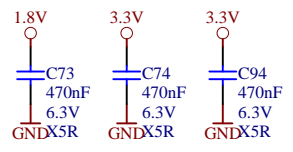
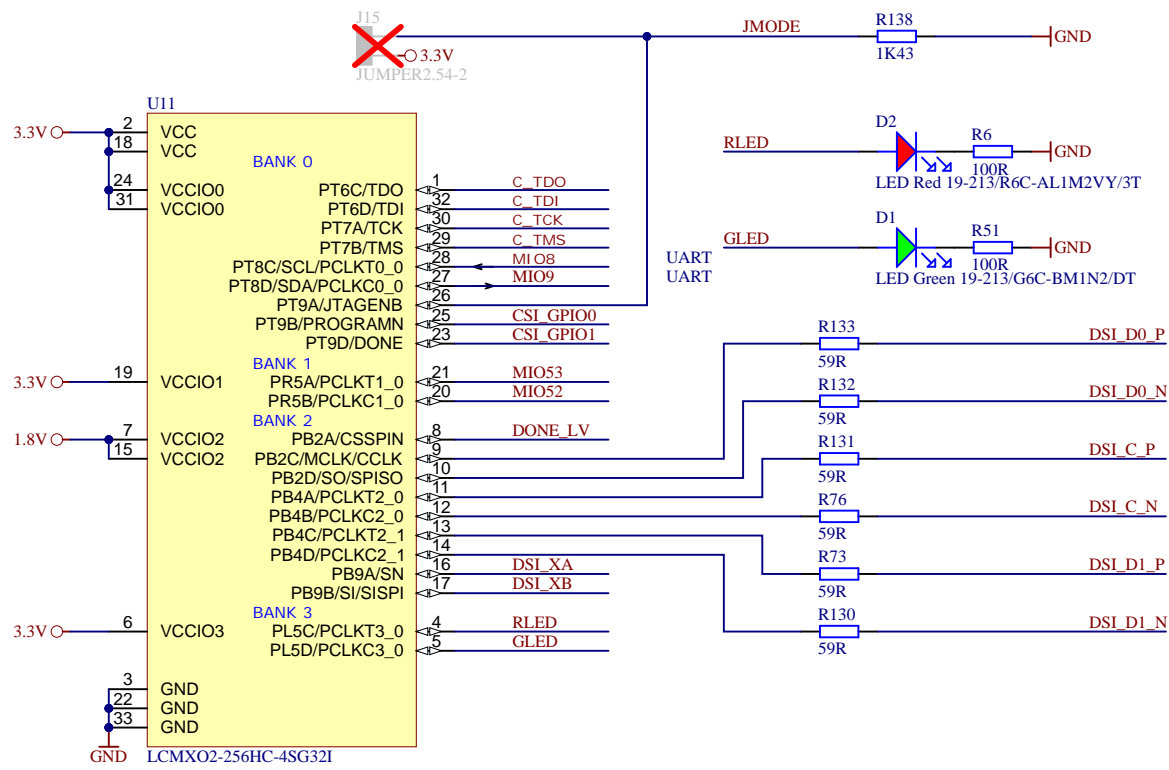
B

C

C

D

D



	Title: CPLD	
	A4	Number: TE0726 41194-A
	Date: 2023-03-20	Rev. 04
	Page 18 of 18	
Filename: SC.SchDoc		Copyright: Trenz Electronic GmbH

1

2

3

4