



TE0726 TRM

Revision v.56

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0726+TRM>

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4 Overview

The Trenz Electronic TE0726 is an industrial/extended grade module based on AMD Zynq 7 Series. It is Raspberry Pi form-factor compatible.

Refer to <http://trenz.org/te0726-info> for the latest online version of this manual and other available documentation.

4.1 Key Features

- **SoC/FPGA/Module**
 - Package: CLG225
 - Device: Z-7007S, Z-7010, ¹⁾
 - Temperature ranges: Commercial / Extended / Industrial ¹⁾
 - Speed grades: -3, -2, -1 ¹⁾
- **RAM/Storage**
 - 512 MByte DDR3L ECC RAM ¹⁾
 - 16 MByte QSPI Flash ¹⁾
 - 2 KBit EEPROM for FTDI
 - 2 KBit EEPROM for Ethernet & USB HUB
- **On Board**
 - System Controller CPLD
 - USB ULPI Transceiver
 - 10/100 Ethernet Transceiver with USB hub
 - USB to JTAG / UART FTDI
- **Interface**
 - 1x Micro USB (UART/JTAG)
 - 4x USB 2.0
 - 1x microSD Card socket
 - 1x Boot Select DIP switch
 - 1x Ethernet RJ45 socket
 - 1x TRRS Audio Jack 3.5mm with microphone (PWM audio only)
 - 1x HDMI Connector
 - 1x CSI-2 Connector (Camera Serial Interface)
 - 1x DSI Connector (Display Serial Interface)
 - 1x5 Pin Header for I²C
 - 2x20 Pin Header with 26 GPIO, 1x I²C, 5 and 3.3 V
 - 3 additional Pinheaders for CPLD access, Reset and PUDC (SoC Boot IO State) changes
- **Power**
 - via Micro USB
 - via 5V Pin header
- **Dimension**
 - 56 mm x 85 mm, like Raspberry Pi
- **Notes**
 - ¹⁾ Depends on assembly variant

4.2 Block Diagram

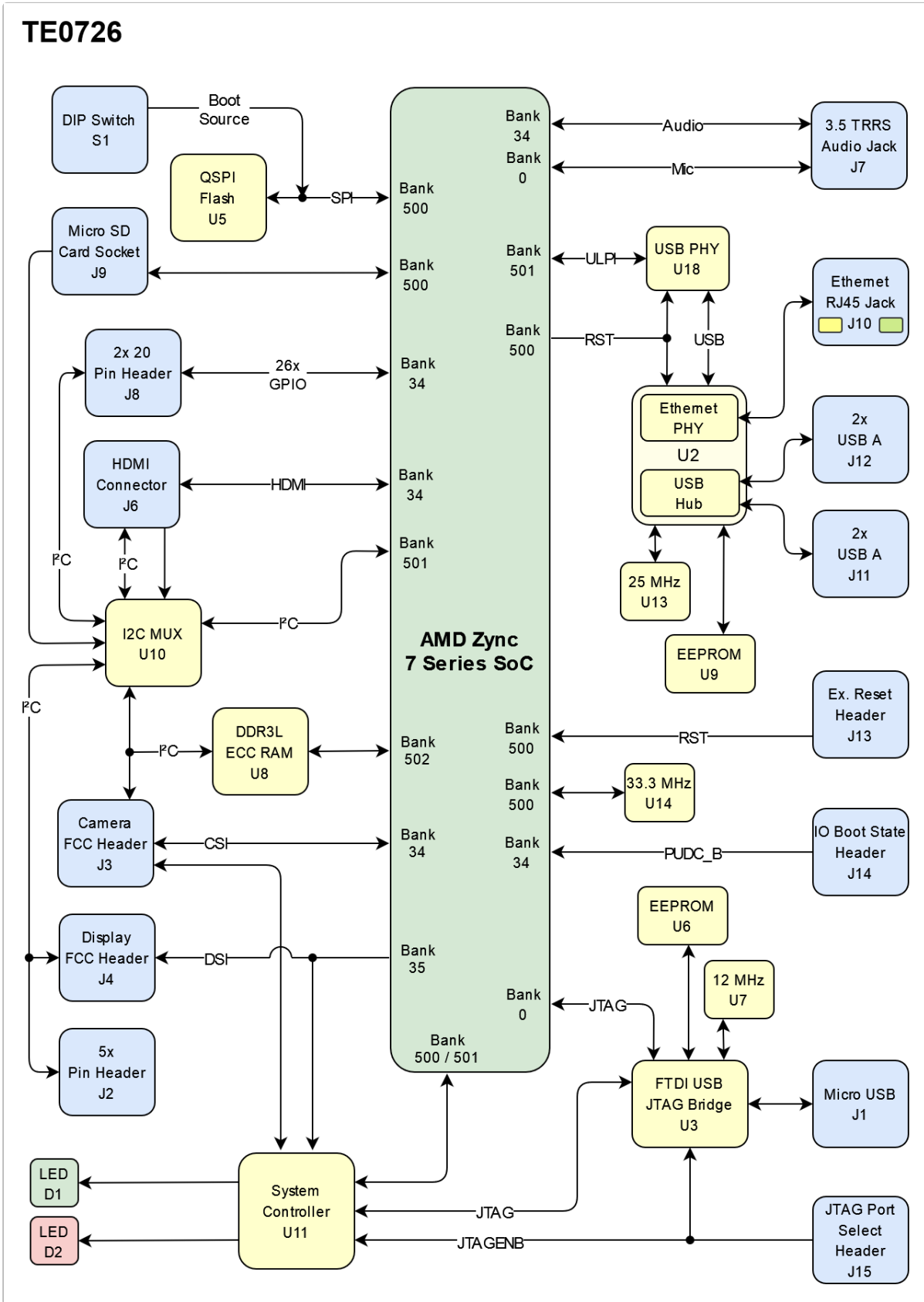


Figure 1: TE0726 block diagram

4.3 Main Components

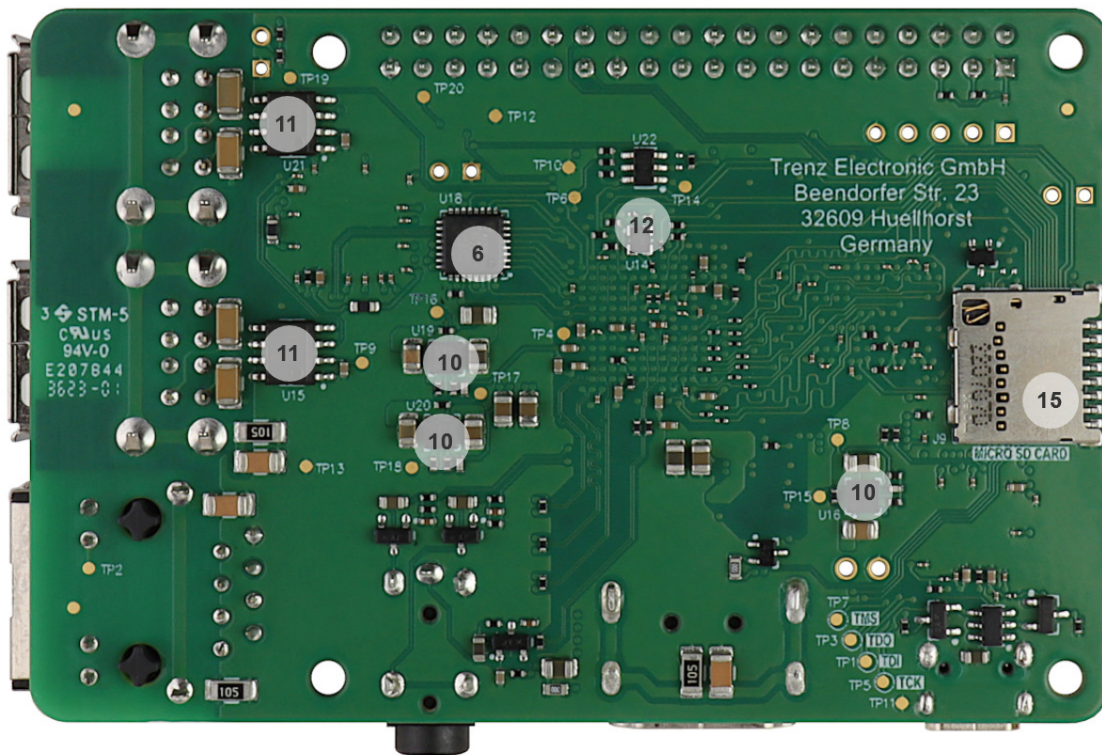
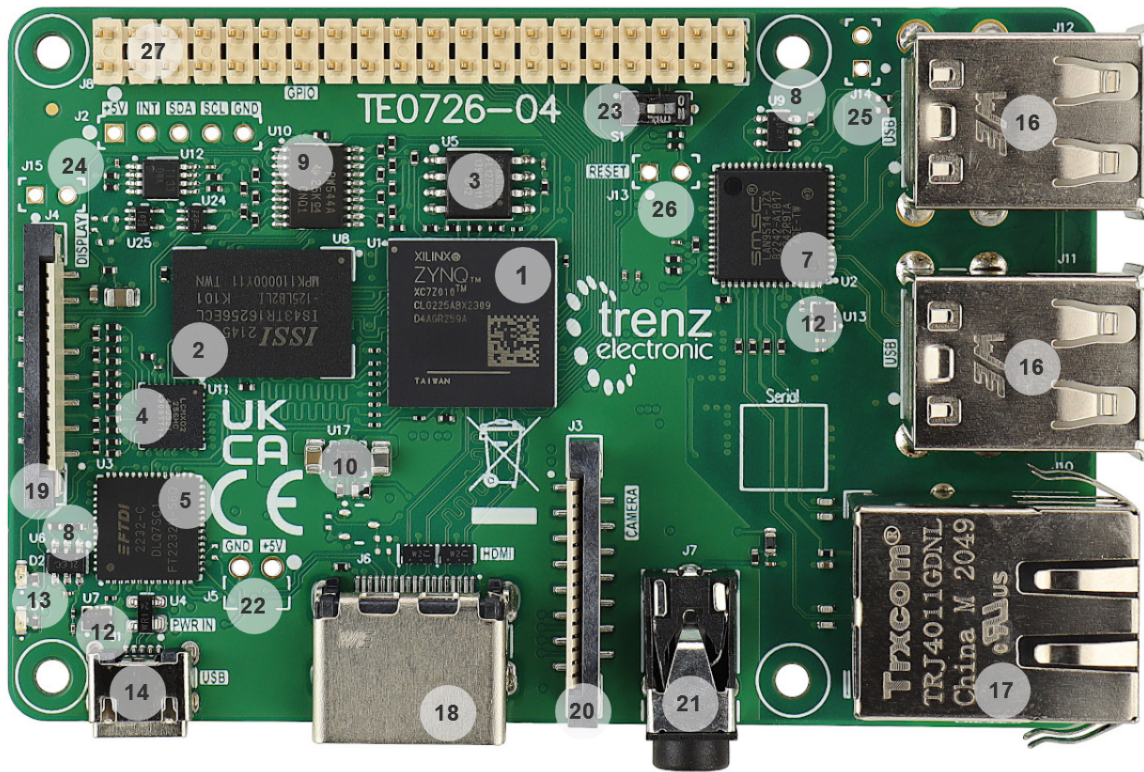


Figure 2: TE0726 main components

1. AMD 7 Series Zynq, U1
2. DDR3L ECC RAM, U8
3. SPI Flash, U5
4. System Controller CPLD, U11
5. FTDI USB to multipurpose JTAG/FIFO, U3
6. USB Transceiver, U18
7. Ethernet Transceiver LAN9514 with 4 port USB Hub , U2
8. EEPROM, U6 , U9
9. I²C Multiplexer, U10
10. Power Supply, U16, U17, U19, U20
11. USB power switch, U15 , U21
12. Oscillator, U14 , U13 , U7
13. LED, D1 , D2
14. Micro USB B receptacle, J1
15. microSD card, J9
16. 2x USB A, J11 , J12
17. RJ-45 Ethernet connector, J10
18. HDMI connector, J6
19. DSI LCD connector, J4
20. CSI camera connector, J3
21. 3.5mm RCA audio jack, J7
22. +5V Power Connector, J5
23. Boot DIP switch, S1
24. JTAG Port select header, J15
25. Boot IO State select header, J14
26. Externer reset header, J13
27. 2x20 pin header, J8

4.4 Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash	not programmed	
EEPROM FTDI	preprogrammed	
EEPROM ETH	not programmed	
System Controller CPLD	preprogrammed	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
2x 20 2.54 mm Pin Header	J8	GPIO (HR)	26	
2x 20 2.54 mm Pin Header	J8	I ² C	2	Multiplexer U10
2x 2.54 mm Pin Header	J15	JTAG select	1	SoC or SC select
2x 2.54 mm Pin Header	J14	Boot IO State select	1	
2x 2.54 mm Pin Header	J13	External reset	1	
2x USB A stacked	J11, J12	USB 2.0	12	To USB PHY (ULPI)
5x 2.54 mm Pin Header	J2	I ² C	2	Multiplexer U10, I ² C shared with J4
5x 2.54 mm Pin Header	J2	Interrupt	1	Multiplexer U10
DIP switch	S1	Boot select	1	Shared with SPI
FCC	J4	MIPI DSI	6 (3 pairs)	
FCC	J4	I ² C	2	Multiplexer U10
FCC	J3	I ² C	2	Multiplexer U10
FCC	J3	MIPI CSI-2	8 (4 pairs)	
HDMI	J6	HDMI	8 (4 pairs)	

Connector Type	Designator	Interface	IO CNT	Notes
HDMI	J6	I ² C	2	Multiplexer U10
HDMI	J6	Interrupt	1	Multiplexer U10
Micro-USB 2.0 B	J1	JTAG	2 (1 pair)	SoC or SC selectable
microSD Card	J9	Interrupt	1	Multiplexer U10
microSD Card	J9	SD	5	
RJ-45 Ethernet	J10	10/100 ETH	12	To USB PHY (ULPI)
TRRS 3.5 mm	J7	RCA Audio	2	
TRRS 3.5 mm	J7	RCA Mic	1	

Table 2: Board Connectors

5.2 Test Points

Test Point	Signal	Notes
TP1	TDI	
TP2	3.3V	
TP3	TDO	
TP4	1.8V	
TP5	TCK	
TP6	1.0V	
TP7	TMS	

Test Point	Signal	Notes
TP8	1.35V	
TP9	5V	
TP10	GND	
TP11	GND	
TP12	GND	
TP13	GND	
TP14	POR B	Zync SoC reset signal
TP15	PG_1.35V	Power good signal
TP16	PG_1.8V	Power good signal
TP17	PG_3.3V	Power good signal
TP18	PG_1.0V	Power good signal
TP19	PUDC	Zynq SoC IO State during boot process
TP20	SPI0_DQ3/M0	Boot source select signal

Table 3: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR3L RAM	U8	<ul style="list-style-type: none"> Zynq SoC DDR Interface PS Bank 502 	
System Controller CPLD	U11	<ul style="list-style-type: none"> Zynq SoC MIO Bank 35 MIDI DSI J4 MIDI CSI J3 FTDI U7 LEDs 	
USB-PHY	U18	<ul style="list-style-type: none"> Zynq SoC MIO and Zynq SoC USB ULPI 	
USB Ethernet Hub	J10	<ul style="list-style-type: none"> USB PHY USB A connectors J11 and J12 Power switch for USB A connectors U15, U21 ETH connector J10 EEPROM U9 	
FTDI	U3	<ul style="list-style-type: none"> JTAG to System Controller and Zynq SoC EEPROM U6 	
I ² C Expander	U10	<ul style="list-style-type: none"> Zynq MIO (Bus master) DDR3L via Voltage Bridge U12 shared with MIDI CSI J3 MIDI DSI J4 and Pin Header J2 HDMI socket J6 Pin header J8 	
I ² C Interrupts	U10	<ul style="list-style-type: none"> Zynq MIO (Bus master) microSD Card socket J9 insertion detection HDMI J6 insertion detection Pin header J2 	
Oscillator	U14	<ul style="list-style-type: none"> Zynq SoC - PS 	33.3 MHz

Chip/Interface	Designator	Connected To	Notes
Oscillator	U9	<ul style="list-style-type: none">• USB PHY	25 MHz
Oscillator	U7	<ul style="list-style-type: none">• FTDI	12 MHz

Table 4: On board peripherals

7 Configuration and System Control Signals

Connector	Signal Name	Direction ¹⁾	Description
S1	SPI0_DDQ3 / MO	IN	Boot source switch, SPI flash or SD Card
J13	EXTRST , POR_B , nRST	IN	Reset Zynq SoC
J14	PUDC	IN	State of Zynq SoC IO lines during boot
J15	JMODE , BDBUS7	IN	JTAG endpoint selction, System Controller or Zynq SoC

Table 5: Controller signal.

¹⁾ Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector + Pin	Direction ¹⁾	Notes
USB_B_Vbus	J1	IN	Default power supply 5V
5V	J5.1	IN/OUT	2x Pin Header, intended for alternative powering
5V	J2.1 J8.2 , J8.4	OUT	5x Pin Header 2x 20 Pin Header
5V_HDMI	J6.18	OUT	HDMI, reverse current protection diode D11
V_BUS_A , V_BUS_B , V_BUS_C , V_BUS_D	J11.A1 , J11.B1 , J12.A1 , J12.B1	OUT	2x USB A socket
3.3V	J8.1 , J8.17 J3.15 J4.15 J9.4	OUT	2x 20 Pin Header FCC CSI FCC DSI microSD Card socket

Table 6: Module power rails.

¹⁾ Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
1	USB_B_V bus	5V ($\pm 5\%$)	-	Main Power supply via Micro-USB J1.	Main module power supply. 0.5 A minimum. Power consumption depends mainly on design and cooling solution. If more current is needed use J5 for external power supply.
2	3.3V	-	-	Module generated output voltage.	
3	-	-	-	External components which are connected to J8 should be powered up with 3.3V from module.	See link: https://docs.amd.com/v/u/en-US/ds187-XC7Z010-XC7Z020-Data-Sheet , page 8 "PL Power-On/Off Power Supply Sequencing" for PL IO usage

Table 7: Baseboard Design Hints

9 Technical Specifications

9.1 Absolute Maximum Ratings ^{*)}

Power Rail / Schematic Name	Description	Min	Max	Unit
USB_B_Vbus	Determined through "USB 2.0 VBUS Max Limits"	4.75	5.5	V
5V	Determined through "USB 2.0 VBUS Max Limits"	4.75	5.5	V

Table 8: Absolute maximum ratings

^{*)} Stresses beyond those listed under [Absolute Maximum Ratings \(see page 0\)](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Condition \(see page 0\)](#). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

9.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: [Article Number Information](#)¹
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

¹ <https://wiki.trenz-electronic.de/display/PD/Article+Number+Information>

Parameter	Min	Max	Units	Reference Document
USB_B_V bus	4.75	5.25	V	Schematic of this board. SCH-TE0726-04-41C94-A.PDF page 3, table "Supported Voltage Ranges"
5V	4.75	5.25	V	Schematic of this board. SCH-TE0726-04-41C94-A.PDF page 3, table "Supported Voltage Ranges"

Table 9: Recommended operating conditions.

9.3 Physical Dimensions

- Module size: 85 mm × 56 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.57 mm ± 10 %.

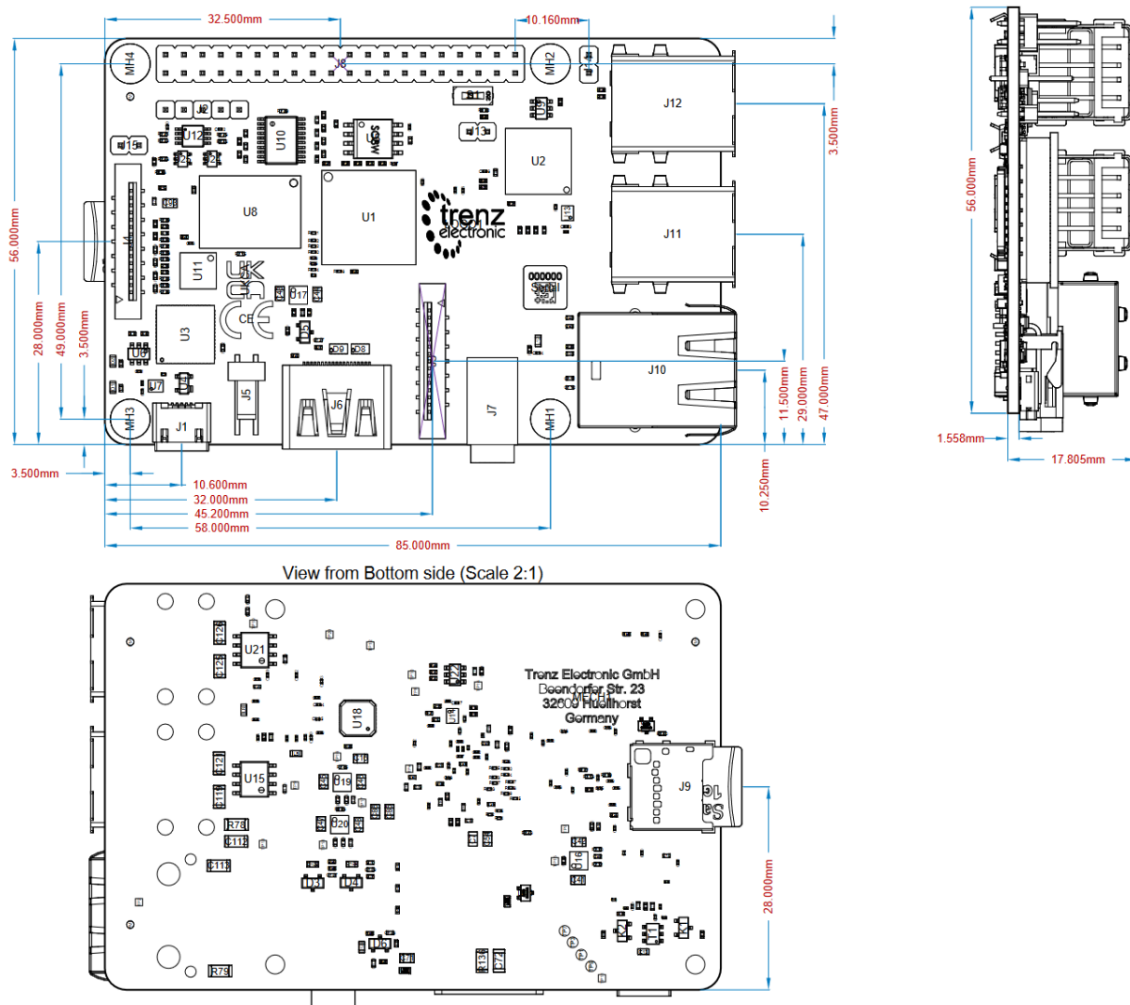


Figure 3: Physical Dimension

10 Currently Offered Variants

Trenz shop TE0726 overview page	
English page²	German page³

Table 10: Trenz Electronic Shop Overview

² <https://shop.trenz-electronic.de/en/search?sSearch=TE0726>

³ <https://shop.trenz-electronic.de/de/search?sSearch=TE0726>

11 Revision History

11.1 Hardware Revision History



Figure 4: Board hardware revision number.

Date	Revision	Changes	PCN Link	Documentation Link
2023-06-10	04	<p>Page Numbers refer to the schematic for this revision</p> <ul style="list-style-type: none"> EOL components U16, U17, U19, U20 (EN5311QI) were replaced by MPM3834CGPA Added MIC bias power L12, C114, R151 (Page 16) Added Legal notices (Page 1) Added power diagram (Page 4) Added S1 switch and R152 for "JTAG only mode" enable (Page 8) The signals were renamed: <ul style="list-style-type: none"> SPI-DQ0/M0 ----> SPI-DQ0/M3 SPI-DQ3/M3 ----> SPI-DQ3/M0 ECC function has been added for U8 (Page 11) Added I2C level shifter U12 for DDR3 ECC function (Page 11) Added Buffers U24, U25 to match the level of signals (Page 6) Added Diode D7, resistors R155, R160 EOL components L1, L2, L3, L4, L6, L7, L9, L10 BKP0603HS121-T replaced by MPZ0603S121HT000 EOL components D8, D9 SP5001-04TTG replaced by EMI8042MUTAG Resistors R80-R82 replaced by 10 kOhm (was 1k43) Added Testpoints TP15 - TP20 The type of testpoints TP1 - TP14 was updated. Diameter changed from 0.8 mm to 1 mm CEC function is not supported. L11 was removed. C127, D5, R140, R42 are DNP Power-up sequencing was updated for new DC-DC supplies Capacitors C29, C32, C33 replaced by 470 nF (was 100 nF) 	<p>PCN-20230619 TE0726-03 to TE0726-04 Hardware Revision Change⁴</p>	<p>TE0726-04⁵</p>
2021-01-21	03	<ul style="list-style-type: none"> Change DDR3 RAM (U8) from IM4G16D3FABG-125I to IS43TR16256BL-125KBLL Clock Revision Change (U7, U14) from SiT8008AI-... to SiT8008BI-... Clock Revision Change (U13) from SiT8008AI-... to SiT8008BI-... LEDs D1 and D2 changed to 19-213/G6C-BM1N2/DT and 19-213/R6C-AL1M2VY/3T Set S/N to not fitted 	<p>PCN-20210121 TE0726-03 DDR3 Change and Product Update⁶</p>	<p>TE0726-03⁷</p>

4 <https://wiki.trenz-electronic.de/display/PD/PCN-20230619+TE0726-03+to+TE0726-04+Hardware+Revision+Change>

5 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/REV04

6 <https://wiki.trenz-electronic.de/display/PD/PCN-20210121+TE0726-03+DDR3+Change+and+Product+Update>

7 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/REV03

Date	Revision	Changes	PCN Link	Documentation Link
2019-04-08	03	<ul style="list-style-type: none"> VBUS Resistor R94 replaced by 10 kOhm (was 12k1) 	-	TE0726-03⁸
2016-05-06	03	<ul style="list-style-type: none"> Introduced new variants: <ul style="list-style-type: none"> Default with DDR3L 128 Mb TE0726-03M with DDR3L 512 Mb TE0726-03L with DDR3L 128 Mb, without usb's, eth_phy, RJ-45, CSI, DSI, HDMI and 3.5mm jack connectors Changed FTDI to 56 pins package Moved LED's into Raspberry Pi 3 layout Replaced POWER connector on right angle connector Corected conection PUDC pin Replace HDMI, DSI/CSI connector, USB stacked connectors, RJ-45, power connector) 	-	TE0726-03⁹
2016-01-26	02	<ul style="list-style-type: none"> CSI CLK line moved to MRCC pin, CSI lanes swap CSI camera GPIO moved to MIO GPIO RPi GPIO 14,15 moved from MIO to PL Added 47 µF capacitor for SD Card VCC (required by SD spec) Added 47 µF capacitor for RPi camera - prevent voltage drop at camera init Fixed MODE pin strapping LED change 0603 Added POWER connector 2 pin Change HDMI ESD to ESD+EMI Fixed HDMI HPD and backpower DSI find solution for LS mode Fixed XADC power caps Changed LPDDR2 to DDR3L 	-	TE0726-02¹⁰
-	01	<ul style="list-style-type: none"> Initial board release 	-	-

Table 11: Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

11.2 Document Change History

8 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/REV03

9 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/REV03

10 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726/REV02


Date	Revision	Contributor	Description
 2024-07-30	v.56 (see page 5)	Kilian Jahn¹¹	<ul style="list-style-type: none"> Removed editing bar from 2 pictures
2024-04-16	v.54	John Hartfiel	<ul style="list-style-type: none"> Updated to new TRM style. Updated to board REV04.
2017-11-10	v.52	John Hartfiel	<ul style="list-style-type: none"> rework J8 header
2017-11-10	v.51	Ali Naseri	<ul style="list-style-type: none"> Updated Power section added Power-Distribution diagram
2017-05-30	v.40	Jan Kumann	<ul style="list-style-type: none"> Absolute maximum ratings Layout redesign Wiki link fixed SoC model removed from BD
2017-05-24	v.1	Jan Kumann	<ul style="list-style-type: none"> Initial version
--	all	Ali Naseri¹² , John Hartfiel¹³ , Jan Kumann¹⁴ , Kilian Jahn¹⁵ , Thorsten Trenz¹⁶	<ul style="list-style-type: none"> --

Table 12: Document change history.

11 <https://wiki.trenz-electronic.de/display/~k.jahn>
 12 <https://wiki.trenz-electronic.de/display/~a.naseri>
 13 <https://wiki.trenz-electronic.de/display/~j.hartfiel>
 14 <https://wiki.trenz-electronic.de/display/~j.kumann>
 15 <https://wiki.trenz-electronic.de/display/~k.jahn>
 16 <https://wiki.trenz-electronic.de/display/~tht>

12 Disclaimer

12.1 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

12.2 Document Warranty

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12.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

12.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH¹⁷. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List¹⁸ are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)¹⁹.

RoHS


Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07

¹⁷ <http://guidance.echa.europa.eu/>

¹⁸ <https://echa.europa.eu/candidate-list-table>

¹⁹ <http://www.echa.europa.eu/>