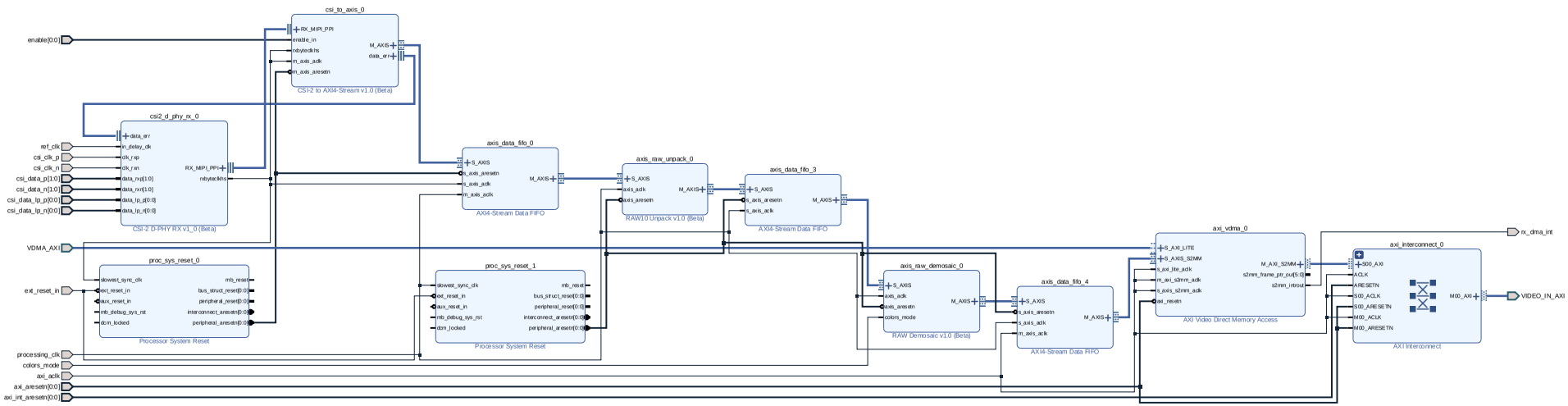
csi_to_axis_0
RX_MIPI_PPI
enable_in
rxbyteclkhs
m_axis_aclk
m_axis_aresetn
M_AXIS
data_err
CSI-2 to AXI4-Stream v1.0 (Beta)
enable[0:0]
csi2_d_phy_rx_0
data_err
ref_clk
in_delay_clk
csi_clk_p
dk_rxp
csi_clk_n
dk_rxn
csi_data_p[1:0]
data_rxp[1:0]
csi_data_n[1:0]
data_rxn[1:0]
csi_data_lp_p[0:0]
data_lp_p[0:0]
csi_data_lp_n[0:0]
data_lp_n[0:0]
RX_MIPI_PPI
rxbyteclkhs
CSI-2 D-PHY RX v1_0 (Beta)
axis_data_fifo_0
S_AXIS
s_axis_aresetn
s_axis_aclk
m_axis_aclk
M_AXIS
AXI4-Stream Data FIFO
axis_raw_unpack_0
S_AXIS
axis_aclk
axis_aresetn
M_AXIS
RAW10 Unpack v1.0 (Beta)
axis_data_fifo_3
S_AXIS
s_axis_aresetn
s_axis_aclk
M_AXIS
AXI4-Stream Data FIFO
VDMA_AXI
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
ext_reset_in
proc_sys_reset_1
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axis_raw_demosaic_0
S_AXIS
axis_aclk
axis_aresetn
colors_mode
M_AXIS
RAW Demosaic v1.0 (Beta)
axis_data_fifo_4
S_AXIS
s_axis_aresetn
s_axis_aclk
m_axis_aclk
M_AXIS
AXI4-Stream Data FIFO
axi_vdma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_s2mm_aclk
s_axis_s2mm_aclk
axi_resetn
M_AXI_S2MM
s2mm_frame_ptr_out[5:0]
s2mm_introut
AXI Video Direct Memory Access
axi_vdma_int
axi_interconnect_0
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
VIDEO_IN_AXI
processing_clk
colors_mode
axi_aclk
axi_aresetn[0:0]
axi_int_aresetn[0:0]