



## TE0726 Zynqberry Demo2

Revision v.2

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0726+Zynqberry+Demo2>

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## 4 Overview

Zynq PS Design with Debian Desktop.

Refer to <http://trenz.org/te0726-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Vivado 2018.3
- Win32DiskImager
- SD Card Formatter
- Linux Debian 9 (Stretch)
- HDMI
- PetaLinux
- SD
- ETH
- USB
- I2C
- Special FSBL for QSPI programming

### 4.2 Revision History

Date	Viva do	Project Built	Authors	Description
2019-1 2-19	2018. 3	te0726-zynqberrydemo2_noprebuilt- vivado_2018.3- build_10_20200113155225.zip te0726-zynqberrydemo2-vivado_2018.3- build_10_20200113155211.zip te0726-demo_2_debian_stretch.zip	Mohsen Chamanbaz	<ul style="list-style-type: none"><li>• update with Vivado 2018.3</li></ul>
2018-1 1-19	2018. 2	te0726-zynqberrydemo1_noprebuilt- vivado_2018.2- build_03_20181119110154.zip  te0726-zynqberrydemo1-vivado_2018.2- build_03_20181119110059.zip	Oleksandr Kiyenko	<ul style="list-style-type: none"><li>• initial release (not published)</li></ul>

**Table 1: Design Revision History**

## 4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

**Table 2: Known Issues**

## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vivado	2018.3	needed
SDK	2018.3	needed
PetaLinux	2018.3	needed

**Table 3: Software**

### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>1</sup>

Complete List is available on <design name>/board\_files/\*\_board\_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
te0726-0±	01	REV01	64MB LPDDR2	16MB		not included, user modifications are needed
te0726-03r	r	REV02, REV03	128MB DDR3L	16MB		not included, user modifications are needed
te0726-03m	m	REV02, REV03	512MB DDR3L	16MB		

<sup>1</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
te0726-0 3-07s-1c	7s	REV03	512MB DDR3L	16MB		

**Table 4: Hardware Modules**

Design supports following carriers:

Carrier Model	Notes
---	

**Table 5: Hardware Carrier**

Additional HW Requirements:

Additional Hardware	Notes
USB Power	Use USB2.0 or higher for power supply via USB
USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
Monitor	DELL Model Number: U2412Mc
HDMI Cable	--

**Table 6: Additional Hardware**

## 4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices<sup>2</sup>](#)

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/ block_design <design name>/ constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

Type	Location	Notes
SDK/ HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLin ux	<design name>/os/ petalinux	PetaLinux template with current configuration

**Table 7: Design sources**

#### 4.5.2 Additional Sources

Type	Location	Notes
--	--	--

**Table 8: Additional design sources**

#### 4.5.3 Prebuilt

File	File- Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Debian SD-Image	*.img	Debian Image for SD-Card
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)

<b>File</b>	<b>File-Extension</b>	<b>Description</b>
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 9: Prebuilt files (only on ZIP with prebuilt content)**

#### 4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0726 "Zynqberry Demo2" Reference Design<sup>3</sup>

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<sup>3</sup>[https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/special/TE0726\\_Reference\\_Design/2018.3/zynqberrydemo2](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/special/TE0726_Reference_Design/2018.3/zynqberrydemo2)

## 5 Design Flow

- ⚠** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

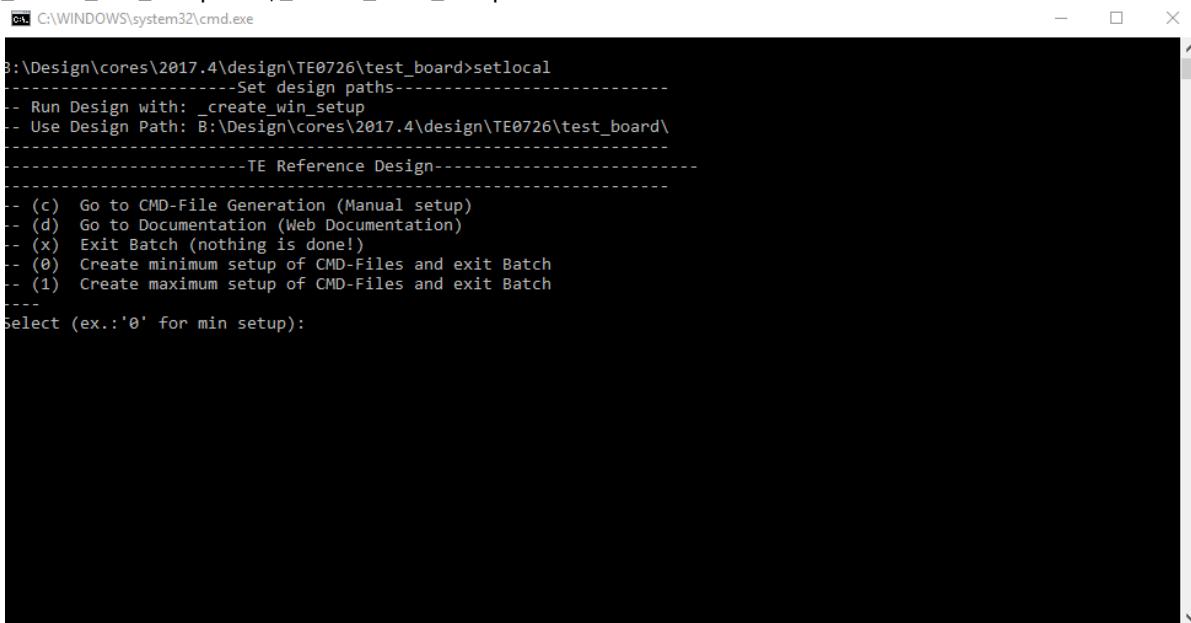
See also:

- [Xilinx Development Tools](#)<sup>4</sup>
- [Vivado Projects - TE Reference Design](#)<sup>5</sup>
- [Project Delivery](#)<sup>6</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>7</sup>

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:



```
C:\WINDOWS\system32\cmd.exe
B:\Design\cores\2017.4\design\TE0726\test_board>setlocal
--Set design paths--
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.4\design\TE0726\test_board\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for min setup):
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
  - a. (optional for manual changes) Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guimode.cmd" Note: Select correct one, see [TE Board Part Files](#)<sup>8</sup>

<sup>4</sup> <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery++Xilinx+devices>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery++Xilinx+devices#ProjectDelivery-Xilinxdevices-Currentlylimitationsoffunctionality>

<sup>8</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

5. Create HDF and export to prebuilt folder
  - a. Run on Vivado TCL: TE::hw\_build\_design -export\_prebuilt  
Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported HDF
  - a. HDF is exported to "prebuilt\hardware\<short name>"  
Note: HW Export from Vivado GUI create another path as default workspace.  
Create Linux images on VM, see [PetaLinux KICKstart](#)<sup>9</sup>
    - i. Use TE Template from /os/petalinux
    - ii. For 128MB and 64MB only: Netboot Offset must be reduced manually, see [Config](#)(see page 21)
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
  - a. "prebuilt\os\petalinux\<DDR size>" or "prebuilt\os\petalinux\<short name>"  
Notes: Scripts select "prebuilt\os\petalinux\<DDR size>", if exist, otherwise "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with HSI/SDK
  - a. Run on Vivado TCL: TE::sw\_run\_hsi  
Note: Scripts generate applications and bootable files, which are defined in "sw\_lib\apps\_list.csv"
  - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw\_run\_sdk  
Note: See [SDK Projects](#)<sup>10</sup>

<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>

## 6 Launch

### 6.1 Programming

**⚠** Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging<sup>11</sup>](#)

#### 6.1.1 QSPI

1. Connect JTAG and power module (TE0726 can be powered via JTAG USB or external)
2. Open Vivado Project with "vivado\_open\_existing\_project\_guimode.cmd" or if not created, create with "vivado\_create\_project\_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr\_program\_flash\_binfile -swapp u-boot  
Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp\_fsbl\_flash) on setup  
optional "TE::pr\_program\_flash\_binfile -swapp hello\_te0726" possible
4. Build Image.ub in Petalinux
5. Build the Debian image file with executing the "mkdebian\_stretch.sh" file in Linux Terminal
6. Format the SD Card with SD Card Formatter
7. Write the Debian image file on SD Card with Win32DiskImager
8. Copy the Petalinux image.ub on SD-Card
  - For correct prebuilt file location, see <design\_name>/prebuilt/readme\_file\_location.txt
9. Insert SD-Card

#### 6.1.2 SD

Xilinx Zynq devices in CLG225 package do not support SD Card boot directly from ROM bootloader. Use QSPI for primary boot and SD for secondary boot (u-boot)

#### 6.1.3 JTAG

Not used on this Example.

### 6.2 Usage

1. Prepare HW like described in section [Programming](#)(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Insert SD Card with image.ub
4. Power On PCB  
Note: 1. Zynq Boot ROM loads FSBL from QSPI into OCM, 2. FSBL loads U-boot from QSPI into DDR, 3. U-boot load Linux from SD into DDR

<sup>11</sup><https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

## 6.2.1 Linux

---

1. Open Serial Console (e.g. putty)
  - a. Speed: 115200
  - b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is \*USB1)
2. Linux Console:  
Note: Wait until Linux boot finished For Linux Login use:
  - a. User Name: root
  - b. Password: root  
Note: Wait until Linux boot finished For Linux Login use:
  - i. User Name: root
  - ii. Password: root
3. You can use a Linux shell to start GUI.
  - a. Run "startx&" to open Desktop
4. Debian Desktop
  - a. open console and run dhclient to request IP
  - b. Web Browser Dillo open console and type dillo or use browser
  - c. open console and start video or audio with "mplayer <video or audio file>"

## 7 System Design - Vivado

### 7.1 Block Design

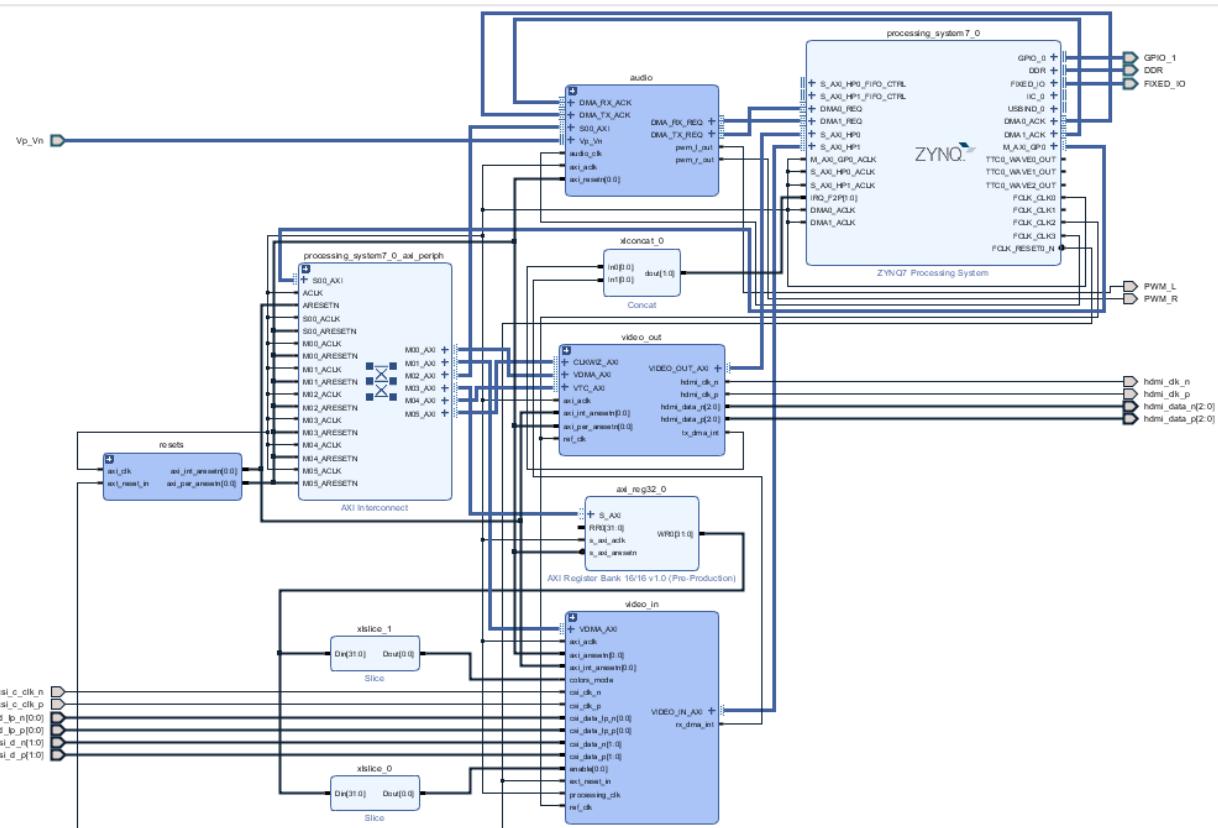


Figure 1: Block Design

#### 7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
USB0	MIO, ETH over USB
SD1	MIO
UART1	MIO
I2C0	EMIO

Type	Note
I2C1	MIO
GPIO	MIO / EMIO
USB RST	MIO
TTC0..1	MIO
WDT	MIO
AXI HP0..1	
DMA0..1	

**Table 10: PS Interfaces**

## 7.2 Constraints

---

### 7.2.1 Basic module constraints

---

```
_i_bitgen_common.xdc

#
# Common BITGEN related settings for TE0726
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

### 7.2.2 Design specific constraint

---

```
_i_common.xdc

#
#
#
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

### \_i\_te0726.xdc

```
#set_property IOSTANDARD LVCMOS33 [get_ports spdif_tx_o]
#set_property PACKAGE_PIN K15 [get_ports spdif_tx_o]

set_property IOSTANDARD LVCMOS33 [get_ports {GPIO_1_tri_io[*]}]
# GPIO Pins
# GPIO2
set_property PACKAGE_PIN K15 [get_ports {GPIO_1_tri_io[0]}]
# GPIO3
set_property PACKAGE_PIN J14 [get_ports {GPIO_1_tri_io[1]}]
# GPIO4
set_property PACKAGE_PIN H12 [get_ports {GPIO_1_tri_io[2]}]
# GPIO5
set_property PACKAGE_PIN N14 [get_ports {GPIO_1_tri_io[3]}]
# GPIO6
set_property PACKAGE_PIN R15 [get_ports {GPIO_1_tri_io[4]}]
# GPIO7
set_property PACKAGE_PIN L14 [get_ports {GPIO_1_tri_io[5]}]
# GPIO8
set_property PACKAGE_PIN L15 [get_ports {GPIO_1_tri_io[6]}]
# GPIO9
set_property PACKAGE_PIN J13 [get_ports {GPIO_1_tri_io[7]}]
# GPIO10
set_property PACKAGE_PIN H14 [get_ports {GPIO_1_tri_io[8]}]
# GPIO11
set_property PACKAGE_PIN J15 [get_ports {GPIO_1_tri_io[9]}]
# GPIO12
set_property PACKAGE_PIN M15 [get_ports {GPIO_1_tri_io[10]}]
# GPIO13
set_property PACKAGE_PIN R13 [get_ports {GPIO_1_tri_io[11]}]
# GPIO16
set_property PACKAGE_PIN L13 [get_ports {GPIO_1_tri_io[12]}]
# GPIO17
set_property PACKAGE_PIN G11 [get_ports {GPIO_1_tri_io[13]}]
# GPIO18
set_property PACKAGE_PIN H11 [get_ports {GPIO_1_tri_io[14]}]
# GPIO19
set_property PACKAGE_PIN R12 [get_ports {GPIO_1_tri_io[15]}]
# GPIO20
set_property PACKAGE_PIN M14 [get_ports {GPIO_1_tri_io[16]}]
# GPIO21
set_property PACKAGE_PIN P15 [get_ports {GPIO_1_tri_io[17]}]
# GPIO22
set_property PACKAGE_PIN H13 [get_ports {GPIO_1_tri_io[18]}]
# GPIO23
set_property PACKAGE_PIN J11 [get_ports {GPIO_1_tri_io[19]}]
# GPIO24
set_property PACKAGE_PIN K11 [get_ports {GPIO_1_tri_io[20]}]
# GPIO25
set_property PACKAGE_PIN K13 [get_ports {GPIO_1_tri_io[21]}]
# GPIO26
set_property PACKAGE_PIN L12 [get_ports {GPIO_1_tri_io[22]}]
# GPIO27
```

```
set_property PACKAGE_PIN G12 [get_ports {GPIO_1_tri_io[23]}]

## DSI_D0_N
#set_property PACKAGE_PIN F13 [get_ports {GPIO_1_tri_io[24]}]
## DSI_D0_P
#set_property PACKAGE_PIN F14 [get_ports {GPIO_1_tri_io[25]}]
## DSI_D1_N
#set_property PACKAGE_PIN F12 [get_ports {GPIO_1_tri_io[26]}]
## DSI_D1_P
#set_property PACKAGE_PIN E13 [get_ports {GPIO_1_tri_io[27]}]
## DSI_C_N
#set_property PACKAGE_PIN E11 [get_ports {GPIO_1_tri_io[28]}]
## DSI_C_P
#set_property PACKAGE_PIN E12 [get_ports {GPIO_1_tri_io[29]}]

## CSI_D0_N
#set_property PACKAGE_PIN M11 [get_ports {GPIO_1_tri_io[30]}]
## CSI_D0_P
#set_property PACKAGE_PIN M10 [get_ports {GPIO_1_tri_io[31]}]
## CSI_D1_N
#set_property PACKAGE_PIN P14 [get_ports {GPIO_1_tri_io[32]}]
## CSI_D2_P
#set_property PACKAGE_PIN P13 [get_ports {GPIO_1_tri_io[33]}]
## CSI_C_N
#set_property PACKAGE_PIN N12 [get_ports {GPIO_1_tri_io[34]}]
## CSI_C_P
#set_property PACKAGE_PIN N11 [get_ports {GPIO_1_tri_io[35]}]
## PWM_R
##set_property PACKAGE_PIN N8 [get_ports {GPIO_1_tri_io[36]}]
## PWM_L
##set_property PACKAGE_PIN N7 [get_ports {GPIO_1_tri_io[37]}]

# PWM_R
set_property PACKAGE_PIN N8 [get_ports PWM_R]
# PWM_L
set_property PACKAGE_PIN N7 [get_ports PWM_L]
set_property IOSTANDARD LVCMOS33 [get_ports PWM_*]
```

### \_i\_hdmi.xdc

```
set_property IOSTANDARD TMDS_33 [get_ports hdmi_clk_p]
set_property PACKAGE_PIN R7 [get_ports hdmi_clk_p]

set_property IOSTANDARD TMDS_33 [get_ports {hdmi_data_p[*]}]
set_property PACKAGE_PIN P8 [get_ports {hdmi_data_p[0]}]
set_property PACKAGE_PIN P10 [get_ports {hdmi_data_p[1]}]
set_property PACKAGE_PIN P11 [get_ports {hdmi_data_p[2]}]
```

### \_i\_csi.xdc

```
set_property PACKAGE_PIN N11 [get_ports csi_c_clk_p]
set_property IOSTANDARD LVDS_25 [get_ports csi_c_clk_p]
set_property PACKAGE_PIN M9 [get_ports {csi_d_lp_n[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_n[0]}]
set_property PACKAGE_PIN N9 [get_ports {csi_d_lp_p[0]}]
set_property IOSTANDARD HSUL_12 [get_ports {csi_d_lp_p[0]}]
set_property PACKAGE_PIN M10 [get_ports {csi_d_p[0]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[0]}]
set_property PACKAGE_PIN P13 [get_ports {csi_d_p[1]}]
set_property IOSTANDARD LVDS_25 [get_ports {csi_d_p[1]}]
set_property INTERNAL_VREF 0.6 [get_iobanks 34]
set_property PULLDOWN true [get_ports {csi_d_lp_p[0]}]
set_property PULLDOWN true [get_ports {csi_d_lp_n[0]}]
# RPI Camera 1
create_clock -period 6.250 -name csi_clk -add [get_ports csi_c_clk_p]
# RPI Camera 2.1
#create_clock -period 1.875 -name csi_clk -add [get_ports csi_c_clk_p]
```

### \_i\_timing.xdc

```
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl/tx_sync/
out_data_reg[4]}]
set_property ASYNC_REG true [get_cells {zsys_i/audio/axi_i2s_adi_0/U0/ctrl/
SDATA_0_reg[0]}]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks clk_fpga_3]
set_false_path -from [get_clocks clk_fpga_3] -to [get_clocks clk_fpga_0]

set_false_path -from [get_pins {zsys_i/axi_reg32_0/U0/axi_reg32_v1_0_S_AXI_inst/
slv_reg16_reg[1]/C}] -to [get_pins zsys_i/video_in/axis_raw_demosaic_0/U0/
colors_mode_i_reg/D]
set_false_path -from [get_pins zsys_i/video_in/csi_to_axis_0/U0/lane_align_inst/
err_req_reg/C] -to [get_pins zsys_i/video_in/csi2_d_phy_rx_0/U0/clock_upd_req_reg/D]

set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/
GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/
GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_max_first_increment_reg[2]/C}] -to [get_pins
zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/
GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/
sig_btt_eq_0_reg/D]
set_false_path -from [get_pins {zsys_i/video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/
GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/
GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/sig_btt_cntr_dup_reg[1]/C}] -to [get_pins zsys_i/
video_in/axi_vdma_0/U0/I_PRMRY_DATAMOVER/GEN_S2MM_FULL.I_S2MM_FULL_WRAPPER/
GEN_INCLUDE_REALIGNER.I_S2MM_REALIGNER/GEN_INCLUDE_SCATTER.I_S2MM_SCATTER/
sig_btt_eq_0_reg/D]
```

## 8 Software Design - SDK/HSI

---

For SDK project creation, follow instructions from:

[SDK Projects<sup>12</sup>](#)

### 8.1 Application

---

SDK template in ./sw\_lib/sw\_apps/ available.

#### 8.1.1 zynq\_fsbl

---

TE modified 2018.3 FSBL

General:

- Modified Files: main.c, fsbl\_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_fsbl\_hooks.h/.c(for hooks and board)\n\
- General Changes:
  - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te\_\*
  - enable VTC and VDMA cores for debian desktop

#### 8.1.2 zynq\_fsbl\_flash

---

TE modified 2018.3 FSBL

General:

- Modified Files: main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

#### 8.1.3 hello\_te0726

---

Hello TE0726 is a Xilinx Hello World example as endless loop instead of one console output.

---

<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>

## 9 Software Design - PetaLinux

---

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart<sup>13</sup>](#)

### 9.1 Config

---

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Select Image Packaging Configuration ==> Root filesystem type ==> Select SD Card

Changes:

- # CONFIG\_SUBSYSTEM\_ROOTFS\_INITRAMFS is not set
- # CONFIG\_SUBSYSTEM\_ROOTFS\_INITRD is not set
- # CONFIG\_SUBSYSTEM\_ROOTFS\_JFFS2 is not set
- # CONFIG\_SUBSYSTEM\_ROOTFS\_NFS is not set
- CONFIG\_SUBSYSTEM\_ROOTFS\_SD=y
- # CONFIG\_SUBSYSTEM\_ROOTFS\_OTHER is not set

For 64MB variant only:

- CONFIG\_SUBSYSTEM\_NETBOOT\_OFFSET = 0x2000000

For 128MB variant only:

- CONFIG\_SUBSYSTEM\_NETBOOT\_OFFSET = 0x4000000

### 9.2 U-Boot

---

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG\_ENV\_IS\_NOWHERE=y
- # CONFIG\_ENV\_IS\_IN\_SPI\_FLASH is not set

---

<sup>13</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

## 9.3 Device Tree

```
/include/ "system-conf.dtsi"
{
};

/ {
    #address-cells = <1>;
    #size-cells = <1>;

    reserved-memory {
        #address-cells = <1>;
        #size-cells = <1>;
        ranges;
        hdmi_fb_reserved_region@1FC00000 {
            compatible = "removed-dma-pool";
            no-map;
            // 512M (M modules)
            reg = <0x1FC00000 0x4000000>;
            // 128M (R modules)
            //reg = <0x7C00000 0x4000000>;
        };
        camera_fb_reserved_region@1F800000 {
            compatible = "removed-dma-pool";
            no-map;
            // 512M (M modules)
            reg = <0x1F800000 0x4000000>;
            // 128M (R modules)
            //reg = <0x7800000 0x4000000>;
        };
    };

    hdmi_fb: framebuffer@0x1FC00000 {           // HDMI out
        compatible = "simple-framebuffer";
        // 512M (M modules)
        reg = <0x1FC00000 (1280 * 720 * 4)>;   // 720p
        // 128M (R modules)
        //reg = <0x7C00000 (1280 * 720 * 4)>;   // 720p
        width = <1280>;                         // 720p
        height = <720>;                          // 720p
        stride = <(1280 * 4)>;                  // 720p
        format = "a8b8g8r8";
        status = "okay";
    };

    camera_fb: framebuffer@0x1F800000 {          // CAMERA in
        compatible = "simple-framebuffer";
        // 512M (M modules)
        reg = <0x1F800000 (1280 * 720 * 4)>;   // 720p
        // 128M (R modules)
        //reg = <0x7800000 (1280 * 720 * 4)>;   // 720p
    };
}
```

```
width = <1280>;                                // 720p
height = <720>;                               // 720p
stride = <(1280 * 4)>;                         // 720p
format = "a8b8g8r8";
};

vcc_3V3: fixedregulator@0 {
    compatible = "regulator-fixed";
    regulator-name = "vccaux-supply";
    regulator-min-microvolt = <3300000>;
    regulator-max-microvolt = <3300000>;
    regulator-always-on;
};

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
        spi-max-frequency = <50000000>;
        partition@0x00000000 {
            label = "boot";
            reg = <0x00000000 0x00500000>;
        };
        partition@0x00500000 {
            label = "bootenv";
            reg = <0x00500000 0x00020000>;
        };
        partition@0x00520000 {
            label = "kernel";
            reg = <0x00520000 0x00a80000>;
        };
        partition@0x00fa0000 {
            label = "spare";
            reg = <0x00fa0000 0x00000000>;
        };
    };
};

/*
 * We need to disable Linux VDMA driver as VDMA
 * already configured in FSBL
 */
&video_in_axi_vdma_0 {
    status = "disabled";
};

&video_out_axi_vdma_0 {
    status = "disabled";
};
```

```
&video_out_v_tc_0 {
    //xilinx-vtc: probe of 43c20000.v_tc failed with error -2
    status = "disabled";
};

&gpio0 {
    interrupt-controller;
    #interrupt-cells = <2>;
};

&i2c1 {
    #address-cells = <1>;
    #size-cells = <0>;

    i2cmux0: i2cmux@70 {
        compatible = "nxp,pca9544";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x70>;

        i2c1@0 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;

            id_eeprom@50 {
                compatible = "atmel,24c32";
                reg = <0x50>;
            };
        };
        i2c1@1 {      // Display Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        i2c1@2 {      // HDMI Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c1@3 {      // Camera Interface Connector
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
    };
};

/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
}
```

```
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    usb-phy = <&usb_phy0>;
} ;

/*
 * Sound configuration
 */

{

    // Custom driver based on spdif-transmitter
    te_audio: dummy_codec_te {
        compatible = "te,te-audio";
        #sound-dai-cells = <0>;
    };

    // Simple Audio Card from AXI_I2S and custom XADC audio input and
    // PWM audio output cores
    sound {
        compatible = "simple-audio-card";
        simple-audio-card,name = "TE0726-PWM-Audio";
        simple-audio-card,format = "i2s";
        simple-audio-card,widgets =
            "Microphone", "In Jack",
            "Line", "Line In Jack",
            "Line", "Line Out Jack",
            "Headphone", "Out Jack";

        simple-audio-card,routing =
            "Out Jack", "te-out",
            "te-in", "In Jack";

        simple-audio-card,cpu {
            sound-dai = <&audio_axi_i2s_adi_0>;
        };
        simple-audio-card,codec {
            sound-dai = <&te_audio>;
        };
    };
};

&audio_axi_i2s_adi_0 {
    compatible = "adi,axi-i2s-1.00.a";
    reg = <0x43c00000 0x1000>;
    clocks = <&clkc 15>, <&clkc 18>; // FCLK_CLK0, FCLK_CLK3
    clock-names = "axi", "ref";
    dmas = <&dmac_s 0 &dmac_s 1>;
    dma-names = "tx", "rx";
    #sound-dai-cells = <0>;
};

/*

```

```
* We need to disable Linux XADC driver to use XADC for audio recording
*/
&adc {
    status = "disabled";
};
```

## 9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG\_XILINX\_GMII2RGMII=y
- CONFIG\_USB\_USBNET=y
- CONFIG\_USB\_NET\_AX8817X=y
- CONFIG\_USB\_NET\_AX88179\_178A=y
- CONFIG\_USB\_NET\_CDCETHER=y
- # CONFIG\_USB\_NET\_CDC\_EEM is not set
- CONFIG\_USB\_NET\_CDC\_NCM=y
- # CONFIG\_USB\_NET\_HUAWEI\_CDC\_NCM is not set
- # CONFIG\_USB\_NET\_CDC\_MBIM is not set
- # CONFIG\_USB\_NET\_DM9601 is not set
- # CONFIG\_USB\_NET\_SR9700 is not set
- # CONFIG\_USB\_NET\_SR9800 is not set
- # CONFIG\_USB\_NET\_SMSC75XX is not set
- CONFIG\_USB\_NET\_SMSC95XX=y
- # CONFIG\_USB\_NET\_GL620A is not set
- CONFIG\_USB\_NET\_NET1080=y
- # CONFIG\_USB\_NET\_PLUSUSB is not set
- # CONFIG\_USB\_NET\_MCS7830 is not set
- # CONFIG\_USB\_NET\_RNDIS\_HOST is not set
- CONFIG\_USB\_NET\_CDC\_SUBSET\_ENABLE=y
- CONFIG\_USB\_NET\_CDC\_SUBSET=y
- # CONFIG\_USB\_ALI\_M5632 is not set
- # CONFIG\_USB\_AN2720 is not set
- CONFIG\_USB\_BELKIN=y
- CONFIG\_USB\_ARMLINUX=y
- # CONFIG\_USB\_EPSON2888 is not set
- # CONFIG\_USB\_KC2190 is not set
- CONFIG\_USB\_NET\_ZAURUS=y
- # CONFIG\_USB\_NET\_CX82310\_ETH is not set
- # CONFIG\_USB\_NET\_KALMIA is not set
- # CONFIG\_USB\_NET\_QMI\_WWAN is not set
- # CONFIG\_USB\_NET\_INT51X1 is not set
- # CONFIG\_USB\_SIERRA\_NET is not set
- # CONFIG\_USB\_VL600 is not set
- # CONFIG\_USB\_NET\_CH9200 is not set
- CONFIG\_USBIP\_CORE=y
- # CONFIG\_USBIP\_VHCI\_HCD is not set
- # CONFIG\_USBIP\_HOST is not set
- # CONFIG\_USBIP\_VUDC is not set
- # CONFIG\_USBIP\_DEBUG is not set
- # CONFIG\_FRAMEBUFFER\_CONSOLE is not set
- CONFIG\_FB\_SIMPLE=y
- CONFIG SND\_SIMPLE\_CARD\_UTILS=y

- CONFIG SND SIMPLE CARD=y

## 9.5 Rootfs

---

File system will be generated with Debian script (mkdebian\_stretch.sh)

## 9.6 Applications

---

Applications will be generated with Debian script (mkdebian\_stretch.sh)

## 9.7 Kernel Modules

---

### 9.7.1 te-audio-codec

---

Simple module stab to use audio interface. Will be installed with debian script

See: \os\petalinux\project-spec\meta-user\recipes-modules\te-audio-codec\files

## 10 Additional Software

---

No additional software is needed.

## 11 Appx. A: Change History and Legal Notices

### 11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2020-01-13	v.2(see page 6)	Mohsen Chamanbaz	<ul style="list-style-type: none"><li>• Vivado 2018.3 release</li></ul>
2018-12-19	v.1	John Hartfiel	<ul style="list-style-type: none"><li>• Vivado 2018.2 release</li></ul>
--	all	Mohsen Chamanbaz <sup>14</sup> , John Hartfiel <sup>15</sup>	<ul style="list-style-type: none"><li>• update documentation</li></ul>

**Table 11: Document change history.**

### 11.2 Legal Notices

### 11.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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<sup>14</sup> <https://wiki.trenz-electronic.de/display/~M.Chamanbaz>

<sup>15</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

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## 11.9 REACH, RoHS and WEEE

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<sup>16</sup> <http://guidance.echa.europa.eu/>

<sup>17</sup> <https://echa.europa.eu/candidate-list-table>

<sup>18</sup> <http://www.echa.europa.eu/>

precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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