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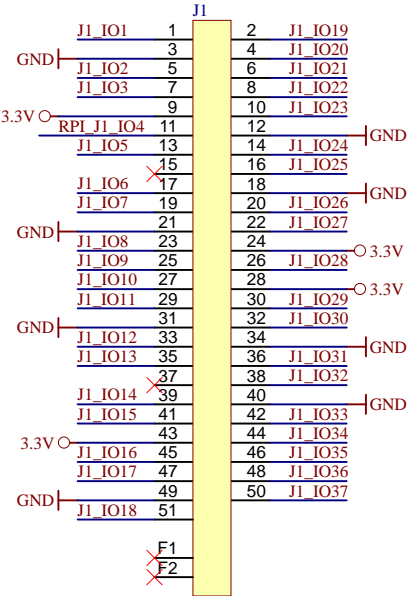
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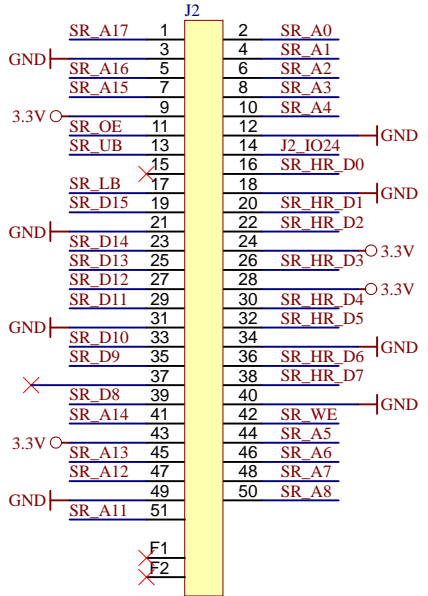
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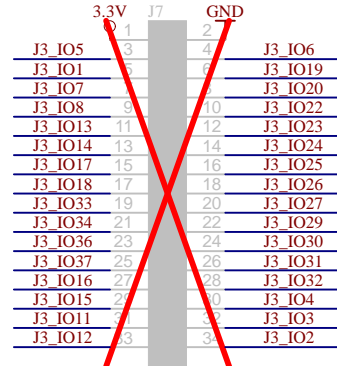
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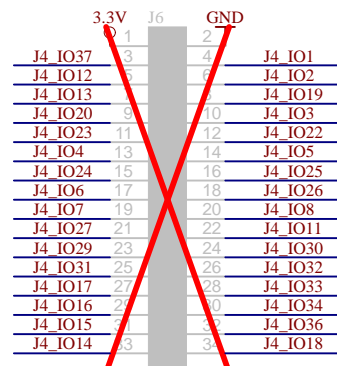
FFC 51pol. 0,3mm 90°



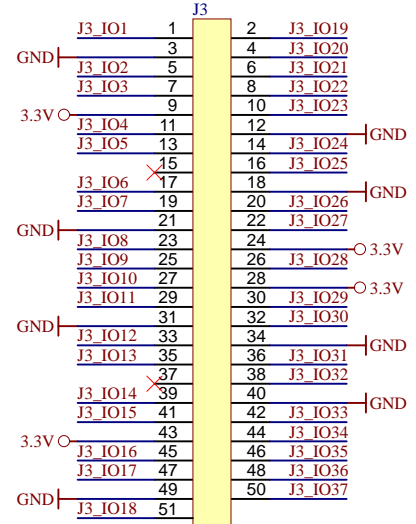
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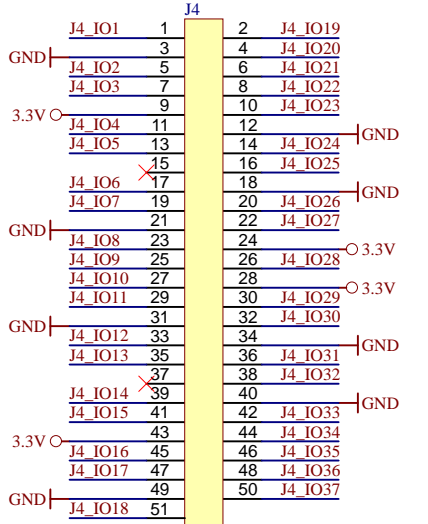
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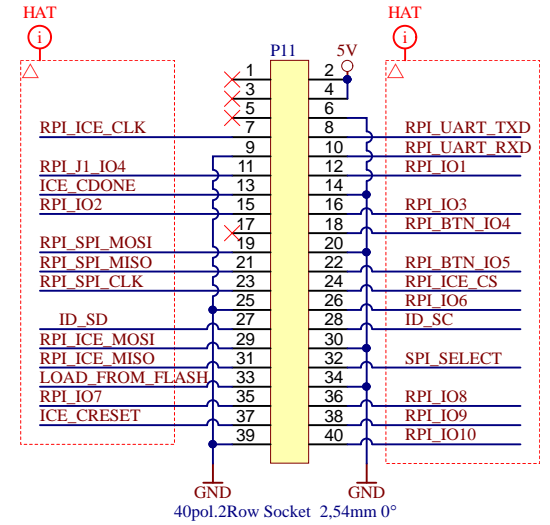
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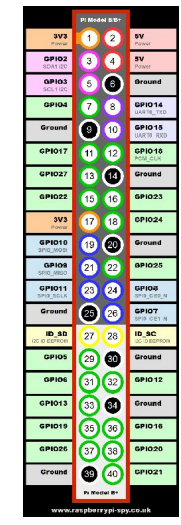
FFC 51pol. 0,3mm 90°



FFC 51pol. 0,3mm 90°



40pol.2Row Socket 2,54mm 0°



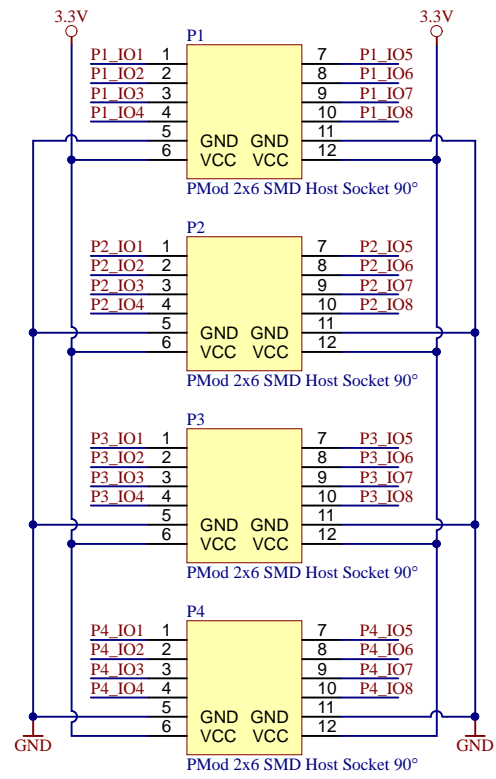
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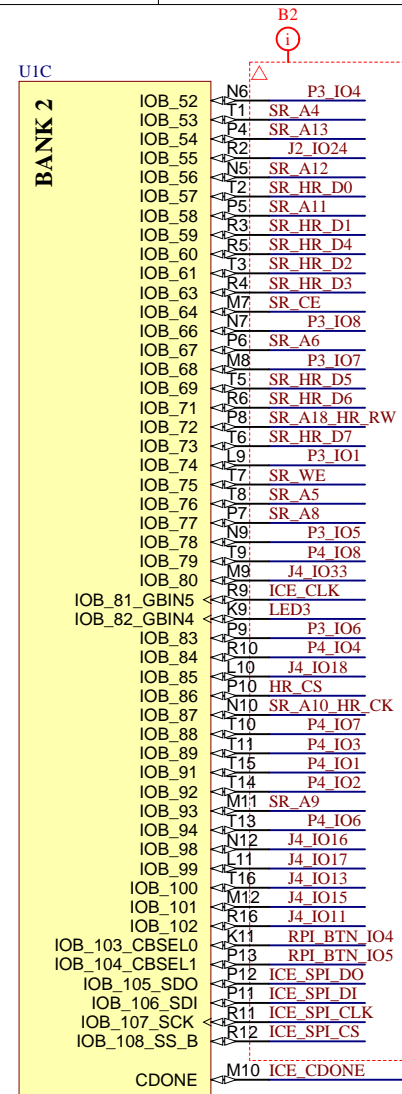
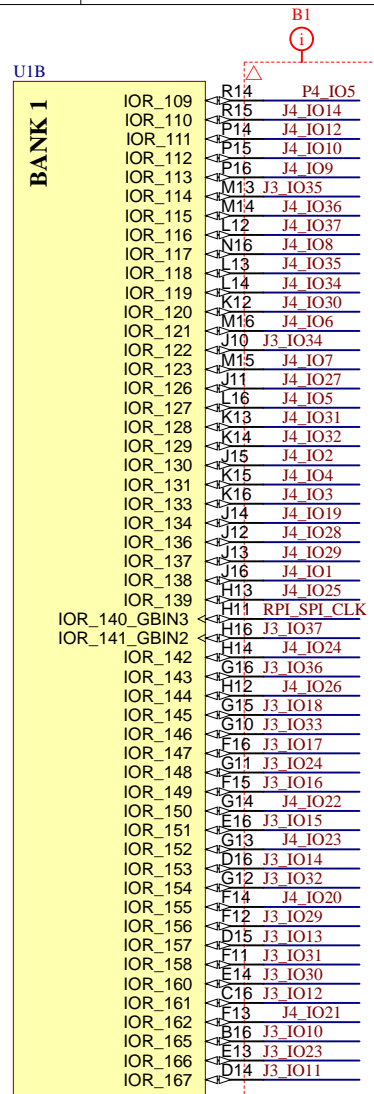
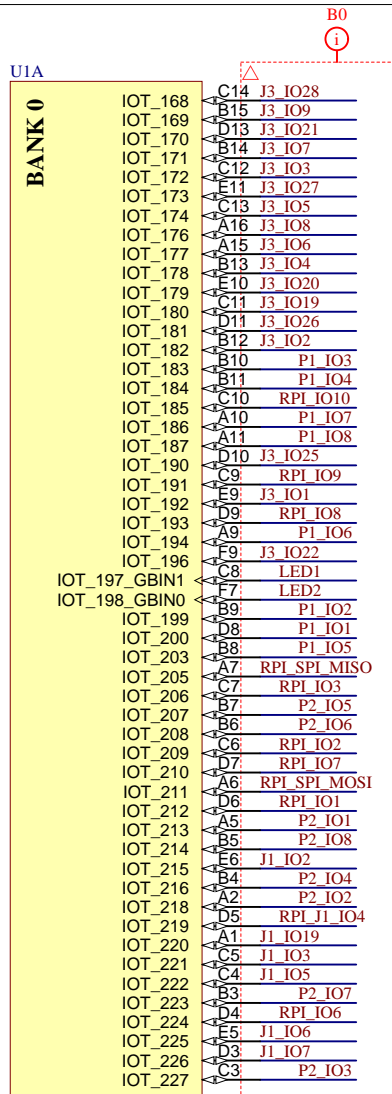
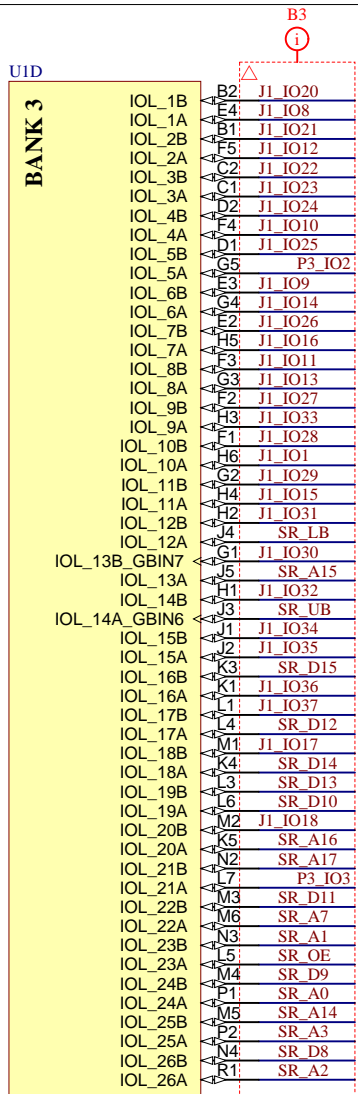
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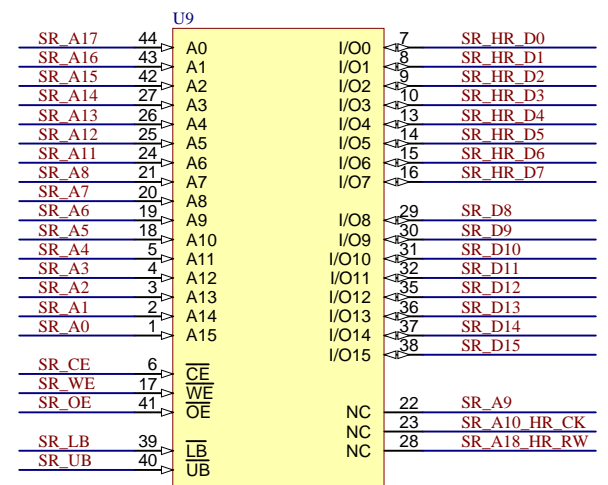
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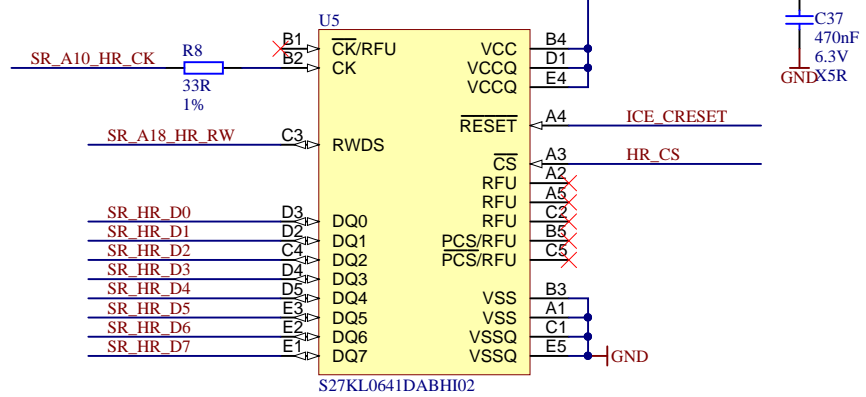
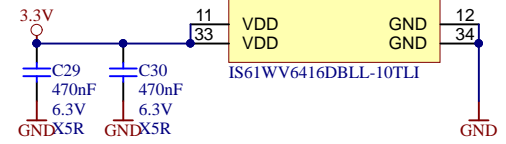
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SRAM on the WEB

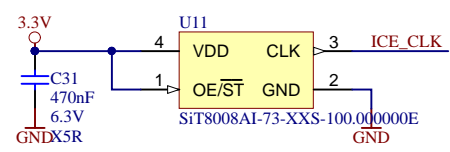
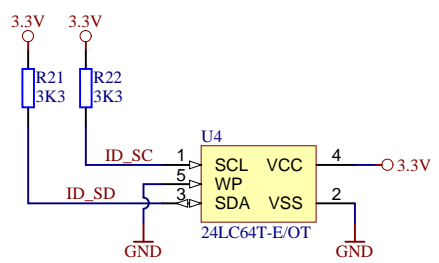
1MBit [IS61WV6416DBLL-10TLI](#)

8MBit [IS61WV51216BLL-10TLI](#)

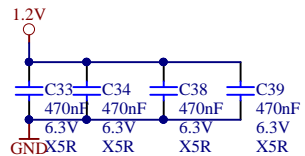
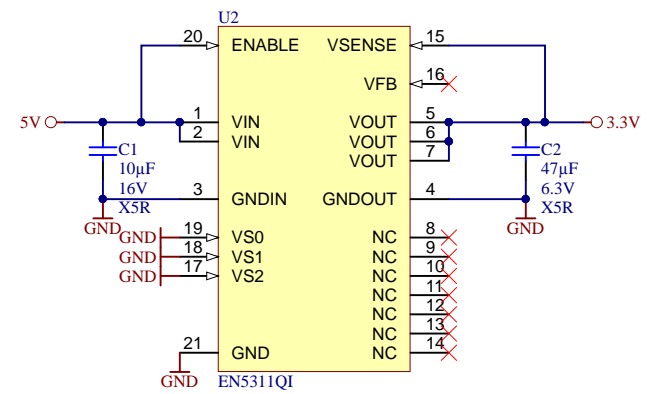
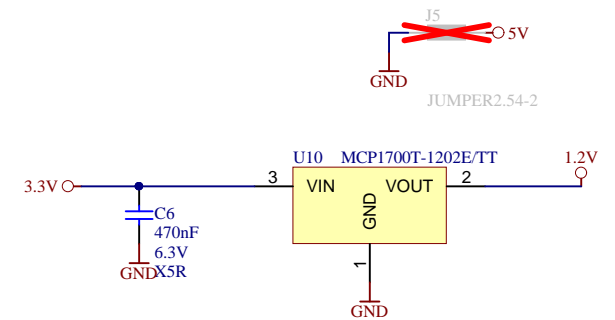
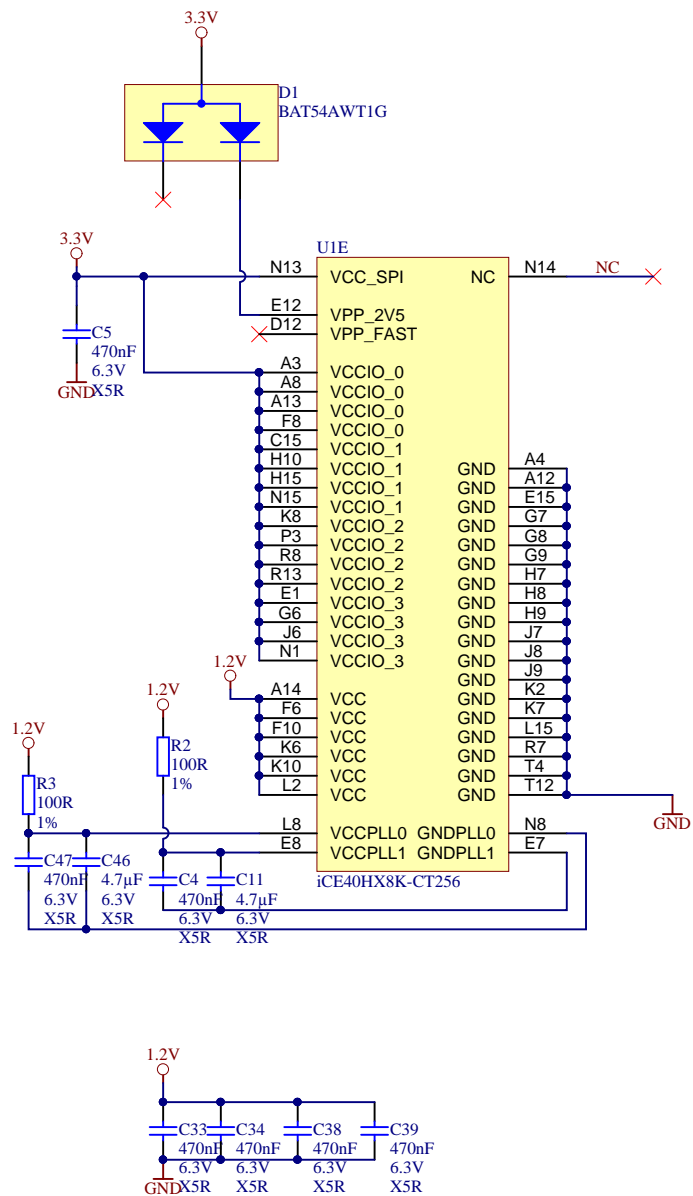



HyperRAM on the WEB

[S27KL0641DABHI02](#)



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Rev. 03:

- 1. PCB: changed position of connectors J1-J4. J1, J3: ΔY -0.8mm; J2, J4: ΔY -0.9mm
- 2. U12 HOLD and WP inputs connected to 3.3V via 10 kOm pull-up resistor.
- 3. PCB: jumper J8 (CPLD JTAG_EN) moved between P3 - P4
- 4. Added series R8 to IO87 (Hyper RAM CK input)
- 5. Added pull-up resistor R9 (Hyper RAM CS input)
- 6. P1 and P2 are interchanged
- 7. Added PMOD and pin headers labels
- 8. Renamed nets
- 9. U5 HyperFlash replaced by HyperRAM

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