TEB0912 Test Board

Revision v.3

Exported on 2021-06-28

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TEB0912+Test+Board

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4 Overview

Design example with Linux and PLL frequency monitoring over VIO.

Refer to http://trenz.org/teb0912-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- SD
- 2x ETH
- CAN
- I2C
- PCIe
- FMeter
- LED
- Modified FSBL SI5395 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-06-10	2019.2	TEB0912-test_board_noprebuilt-vivado_2019.2-build_12_20200610085718.zip TEB0912-test_board-vivado_2019.2-build_12_20200610085620.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TEB0912-02-ABI21-A	11eg_1e_4gb	REV02	4GB	128MB	NA	4GB PL DDR	

Table 4: Hardware Modules

Additional HW Requirements:

Additional Hardware	Notes

Table 5: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[2]

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files
2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 6: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5395	<design name>/misc/Si5395	SI5395 Project with current PLL Configuration
init.sh	<design name>/misc/init_script	Additional Initialization Script for Linux

Table 7: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats

File	File-Extension	Description
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 8: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TEB0912 "Test Board" Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Motherboards_and_Carriers/TEB0912/Reference_Design/2019.2/test_board

5 Design Flow

> Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

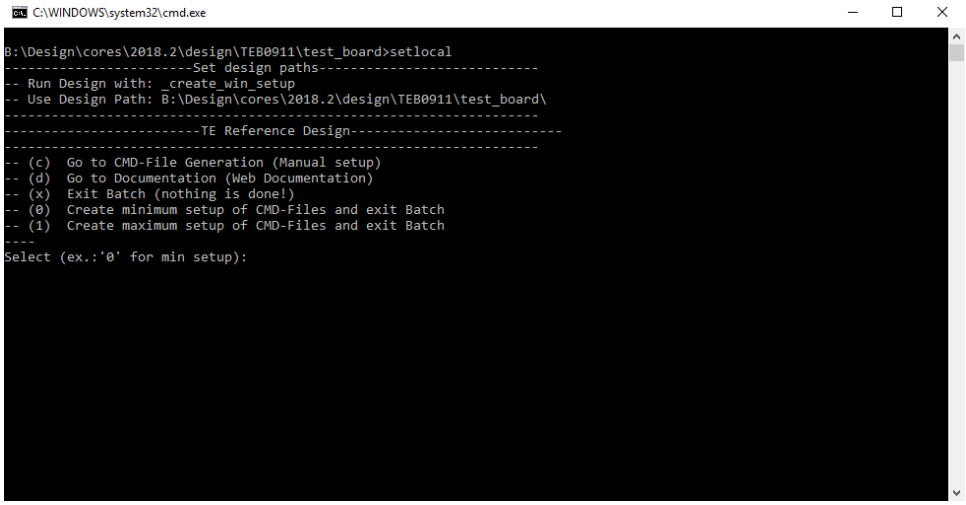
See also:

- Xilinx Development Tools[4]
- Vivado Projects - TE Reference Design[5]
- Project Delivery.[6]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[7]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see alsoTE Board Part Files[8]
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported XSA
   a. XSAis exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.

4 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Create Linux images on VM, see PetaLinux KICKstart[9]

i. Use TE Template from /os/petalinux

7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
   a. Run on Vivado TCL: TE::sw_run_vitis -all
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
      Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[10]

9 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
10 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[11]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
   Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   Optional "TE::pr_program_flash_binfile -swapp hello_teb0912" possible
4. Copy image.ub and optional misc/sd/init.sh on SD-Card
   - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries(see page 12)
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

6.1.3 SD

1. Copy image.ub, Boot.bin and misc/sd/init.sh on SD-Card.
   - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries(see page 12)
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   - Depends on CPLD Firmware, see <todo>
3. Insert SD-Card in SD-Slot.

11 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 12)
2. Connect UART USB (same as FPGA JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect DisplayPort Monitor (List of usable Monitors: https://www.xilinx.com/support/answers/68671.html)
6. (Optional) Connect Network Cable
7. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. ETH0/1 works with udhcpc
   c. PCIe type "lspci"

6.2.2 Vivado HW Manager

Control:

- User LED Control (D16, D15)

Monitoring:

- MGT CLK Measurement:
  - Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).Set radix from VIO signals to unsigned integer.Note: Frequency Counter is inaccurate and displayed unit is Hz
  - Default B229_CLK1: 78,8MHz, B128_CLK1: 150MHz, B129_CLK1: 175MHz, B130_CLK1: 200MHz, B228_CLK1: 125MHz, B23ß_CLK1: 100MHz

<todo>

7 System Design - Vivado

7.1 Block Design

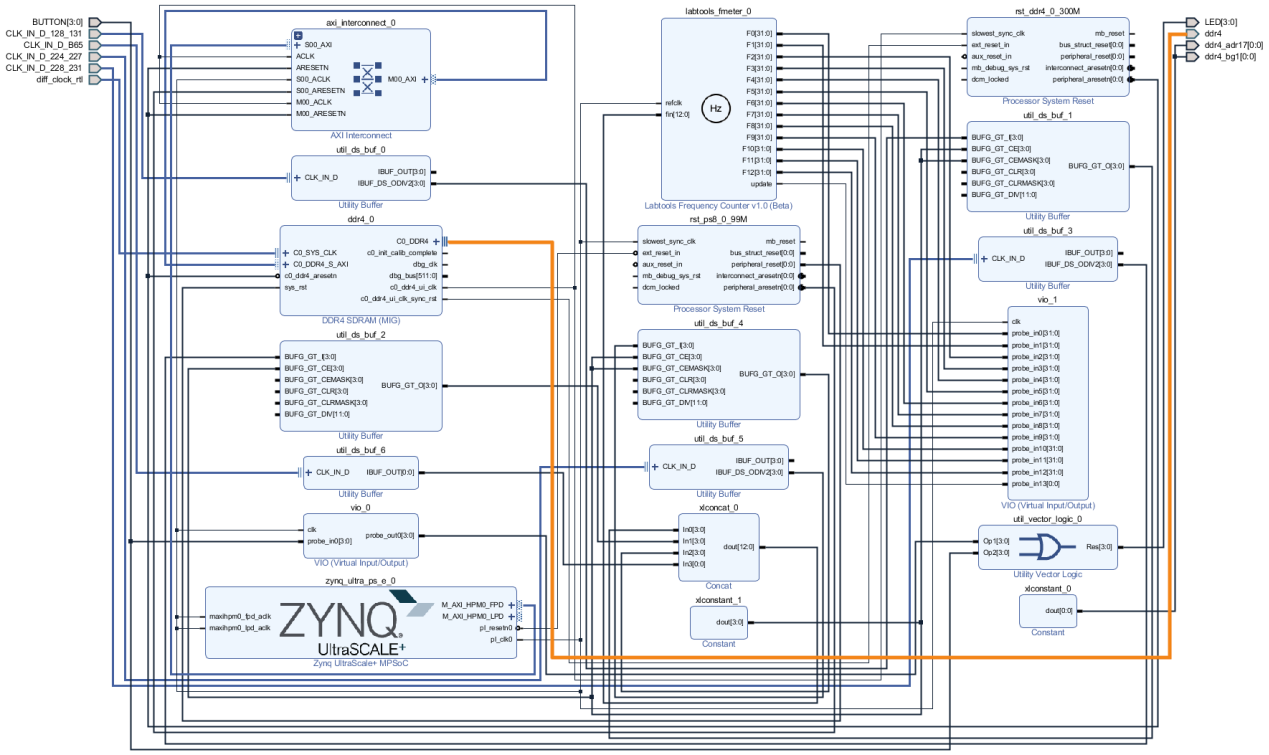


Figure 1: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD1	MIO
CAN0	MIO
I2C0	MIO
I2C1	MIO
UART0	MIO

Type	Note
GPIO0---2	MIO
SWDT0..1	
TTC0..3	
GEM2	MIO
GEM3	MIO
PCIe	MIO/GTP

Table 9: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```
#   AB34     MGT_128_CLK_P
#   AB35     MGT_128_CLK_N
#    W32     MGT_129_CLK_P
#    W33     MGT_129_CLK_N
#    R32     MGT_130_CLK_P
#    R33     MGT_130_CLK_N
#    L32     MGT_131_CLK_P
#    L33     MGT_131_CLK_N
set_property PACKAGE_PIN AB34 [get_ports {CLK_IN_D_128_131_clk_p[0]}]
set_property PACKAGE_PIN W32 [get_ports {CLK_IN_D_128_131_clk_p[1]}]
set_property PACKAGE_PIN R32 [get_ports {CLK_IN_D_128_131_clk_p[2]}]
set_property PACKAGE_PIN L32 [get_ports {CLK_IN_D_128_131_clk_p[3]}]

#   AB11     MGT_228_CLK_N
#   AB12     MGT_228_CLK_P
#    Y11     MGT_229_CLK_N
#    Y12     MGT_229_CLK_P
#    V11     MGT_230_CLK_N
#    V12     MGT_230_CLK_P
#    T11     MGT_231_CLK_N
#    T12     MGT_231_CLK_P
set_property PACKAGE_PIN AB12 [get_ports {CLK_IN_D_228_231_clk_p[0]}]
set_property PACKAGE_PIN Y12 [get_ports {CLK_IN_D_228_231_clk_p[1]}]
set_property PACKAGE_PIN V12 [get_ports {CLK_IN_D_228_231_clk_p[2]}]
set_property PACKAGE_PIN T12 [get_ports {CLK_IN_D_228_231_clk_p[3]}]

#   AK11     MGT_224_CLK_N
#   AK12     MGT_224_CLK_P
#   AH11     MGT_225_CLK_N
#   AH12     MGT_225_CLK_P
#   AF11     MGT_226_CLK_N
#   AF12     MGT_226_CLK_P
#   AD11     MGT_227_CLK_N
#   AD12     MGT_227_CLK_P
set_property PACKAGE_PIN AK12 [get_ports {CLK_IN_D_224_227_clk_p[0]}]
set_property PACKAGE_PIN AH12 [get_ports {CLK_IN_D_224_227_clk_p[1]}]
set_property PACKAGE_PIN AF12 [get_ports {CLK_IN_D_224_227_clk_p[2]}]
set_property PACKAGE_PIN AD12 [get_ports {CLK_IN_D_224_227_clk_p[3]}]

#   B65 CLK
set_property PACKAGE_PIN AR24 [get_ports {CLK_IN_D_B65_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {CLK_IN_D_B65_clk_p[0]}]


#get_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN D3                  }
[get_ports {+3.3V_ETH_PHY_EN}]   #removed on REV02 --> use unused pullup for rev01
#set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN C1                  }
[get_ports {+3.3V_M2_KeyE_EN}]  #removed on REV02 --> use unused pullup for rev01
```

```
#set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN G10                 }
[get_ports {ssd1_perstn[0]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN B6                  } [get_ports
{LED[0]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN B5                  } [get_ports
{LED[1]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN A5                  } [get_ports
{LED[2]}]
set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN A4                  } [get_ports
{LED[3]}]
#set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN G13                 }
[get_ports {M2M_SLEEP[0]}]
#set_property -dict { IOSTANDARD LVCMOS33 PACKAGE_PIN F13 PULLUP TRUE     }
[get_ports {ssd1_wake[0]}]  #removed on REV02 --> use unused pullup for rev01
#
#    B10     FF10_MPRS
#    C10     FF01_MPRS
#    C11     FF00_MPRS
#    D11     FF31_MPRS
#    D12     FF30_MPRS
#    E10     FF20_MPRS
#    E11     FF11_MPRS
#    E12     FF21_MPRS
#    J12     FFA_SDA
#    J14     FFA_SCL
#    K10     FFD_MPRS
#    K11     FFD_MSEL
#    K12     FFC_MPRS
#    K14     FFA_INTL
#    L10     FFD_INTL
#    L12     FFC_MSEL
#    L13     FFA_MPRS
#    L14     FFA_MSEL
#    M10     FFD_SDA
#    M11     FFB_SDA
#    M13     FFB_SCL
#    N10     FFD_SCL
#    N11     FF_AB_RSTL
#    N12     FF_CD_RSTL
#    N13     FFB_MSEL
#    N14     FFB_INTL
#    P12     FFC_INTL
#    P13     FFC_SCL
#    P14     FFB_MPRS
#    R14     FFC_SDA
#
#     E3     PEX_FATAL_ERRORn      REV02 only
#     E4     PEX_GPIO3             REV02 only
#     E5     PEX_LANE_GOOD2n       REV02 only
#     F4     PEX_LANE_GOOD1n       REV02 only
#     F5     PEX_LANE_GOOD0n       REV02 only
#
#     F6     DSPLL1_RST_N
#     F7     DSPLL0_RST_N
#
#    G11     W_DISABLE1n         REV01 other name
```

```
#    G12     W_DISABLE2n         REV01 other name
#    G13  M2M_SLEEP           REV02 only
#
#    F10     SSD1_CLKRQ          REV01 only
#    F13     SSD1_WAKE           REV01 only
#    G10     SSD1_PERSTn         REV01 only
#    G13     M2M_SLEEP           REV01 other nameSSD1_SLEEP
#


set_property -dict { IOSTANDARD LVCMOS18 PACKAGE_PIN AK23                } [get_ports
{BUTTON[0]}]
set_property -dict { IOSTANDARD LVCMOS18 PACKAGE_PIN AL23                } [get_ports
{BUTTON[1]}]
set_property -dict { IOSTANDARD LVCMOS18 PACKAGE_PIN AJ24                } [get_ports
{BUTTON[2]}]
set_property -dict { IOSTANDARD LVCMOS18 PACKAGE_PIN AK24                } [get_ports
{BUTTON[3]}]

set_property -dict { IOSTANDARD DIFF_SSTL12_DCI  PACKAGE_PIN G26          }
[get_ports {diff_clock_rtl_clk_p}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN N24                }
[get_ports {ddr4_act_n}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN J27                }
[get_ports {ddr4_adr[0]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN J24                }
[get_ports {ddr4_adr[1]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN F27                }
[get_ports {ddr4_adr[2]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN E26                }
[get_ports {ddr4_adr[3]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN M25                }
[get_ports {ddr4_adr[4]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN D26                }
[get_ports {ddr4_adr[5]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN K27                }
[get_ports {ddr4_adr[6]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN E27                }
[get_ports {ddr4_adr[7]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN K26                }
[get_ports {ddr4_adr[8]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN H26                }
[get_ports {ddr4_adr[9]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN L24                }
[get_ports {ddr4_adr[10]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN F28                }
[get_ports {ddr4_adr[11]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN J23                }
[get_ports {ddr4_adr[12]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN J26                }
[get_ports {ddr4_adr[13]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN L23                }
[get_ports {ddr4_adr[14]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN K24                }
[get_ports {ddr4_adr[15]}]
```

```
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN H23                }
[get_ports {ddr4_adr[16]}]
## /* dummy for ddr4-ram */
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN G25                }
[get_ports {ddr4_adr17[0]}]


set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN N26                }
[get_ports {ddr4_ba[0]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN G23                }
[get_ports {ddr4_ba[1]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN M23                }
[get_ports {ddr4_bg[0]}]
#set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN P23                }
[get_ports {ddr4_bg[1]}]
## /* dummy for ddr4-ram */
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN P23                }
[get_ports {ddr4_bg1[0]}]

set_property -dict { IOSTANDARD DIFF_SSTL12_DCI PACKAGE_PIN F25                }
[get_ports {ddr4_ck_t[0]}]
set_property -dict { IOSTANDARD DIFF_SSTL12_DCI PACKAGE_PIN E25                }
[get_ports {ddr4_ck_c[0]}]

set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN L25                }
[get_ports {ddr4_cke[0]}]
set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN N23                }
[get_ports {ddr4_cs_n[0]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN P18                } [get_ports
{ddr4_dm_n[0]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN K19                } [get_ports
{ddr4_dm_n[1]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN D19                } [get_ports
{ddr4_dm_n[2]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN G22                } [get_ports
{ddr4_dm_n[3]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN K29                } [get_ports
{ddr4_dm_n[4]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E29                } [get_ports
{ddr4_dm_n[5]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C36                } [get_ports
{ddr4_dm_n[6]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E32                } [get_ports
{ddr4_dm_n[7]}]

set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN N19                }
[get_ports {ddr4_dqs_c[0]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN J22                }
[get_ports {ddr4_dqs_c[1]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN B21                }
[get_ports {ddr4_dqs_c[2]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN E20                }
[get_ports {ddr4_dqs_c[3]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN F30                }
[get_ports {ddr4_dqs_c[4]}]
```

```
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN A32                }
[get_ports {ddr4_dqs_c[5]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN A40                }
[get_ports {ddr4_dqs_c[6]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN C34                }
[get_ports {ddr4_dqs_c[7]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN N20                }
[get_ports {ddr4_dqs_t[0]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN K22                }
[get_ports {ddr4_dqs_t[1]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN C21                }
[get_ports {ddr4_dqs_t[2]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN F20                }
[get_ports {ddr4_dqs_t[3]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN G30                }
[get_ports {ddr4_dqs_t[4]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN B31                }
[get_ports {ddr4_dqs_t[5]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN A39                }
[get_ports {ddr4_dqs_t[6]}]
set_property -dict { IOSTANDARD DIFF_POD12_DCI PACKAGE_PIN D34                }
[get_ports {ddr4_dqs_t[7]}]

set_property -dict { IOSTANDARD SSTL12_DCI PACKAGE_PIN H24                 }
[get_ports {ddr4_odt[0]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN N25                } [get_ports
{ddr4_reset_n}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN N21                } [get_ports
{ddr4_dq[0]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN M18                } [get_ports
{ddr4_dq[1]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN M21                } [get_ports
{ddr4_dq[2]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN M20                } [get_ports
{ddr4_dq[3]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN P21                } [get_ports
{ddr4_dq[4]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN L18                } [get_ports
{ddr4_dq[5]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN M22                } [get_ports
{ddr4_dq[6]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN L19                } [get_ports
{ddr4_dq[7]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN H19                } [get_ports
{ddr4_dq[8]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN L20                } [get_ports
{ddr4_dq[9]}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN H20                } [get_ports
{ddr4_dq[10]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN K21                } [get_ports
{ddr4_dq[11]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN G20                } [get_ports
{ddr4_dq[12]}]
```

```
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN K20                } [get_ports
{ddr4_dq[13]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN H21                } [get_ports
{ddr4_dq[14]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN J21                } [get_ports
{ddr4_dq[15]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B22                } [get_ports
{ddr4_dq[16]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C20                } [get_ports
{ddr4_dq[17]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A22                } [get_ports
{ddr4_dq[18]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A19                } [get_ports
{ddr4_dq[19]}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B23                } [get_ports
{ddr4_dq[20]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B20                } [get_ports
{ddr4_dq[21]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A23                } [get_ports
{ddr4_dq[22]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A20                } [get_ports
{ddr4_dq[23]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F22                } [get_ports
{ddr4_dq[24]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E19                } [get_ports
{ddr4_dq[25]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E22                } [get_ports
{ddr4_dq[26]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN D21                } [get_ports
{ddr4_dq[27]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F23                } [get_ports
{ddr4_dq[28]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F19                } [get_ports
{ddr4_dq[29]}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN D22                } [get_ports
{ddr4_dq[30]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E21                } [get_ports
{ddr4_dq[31]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F31                } [get_ports
{ddr4_dq[32]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN J28                } [get_ports
{ddr4_dq[33]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN J30                } [get_ports
{ddr4_dq[34]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN H28                } [get_ports
{ddr4_dq[35]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F32                } [get_ports
{ddr4_dq[36]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN G28                } [get_ports
{ddr4_dq[37]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN H30                } [get_ports
{ddr4_dq[38]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN F29                } [get_ports
{ddr4_dq[39]}]
```

```
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN E31                } [get_ports
{ddr4_dq[40]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C30                } [get_ports
{ddr4_dq[41]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C31                } [get_ports
{ddr4_dq[42]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B30                } [get_ports
{ddr4_dq[43]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN D31                } [get_ports
{ddr4_dq[44]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C29                } [get_ports
{ddr4_dq[45]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A30                } [get_ports
{ddr4_dq[46]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A29                } [get_ports
{ddr4_dq[47]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C42                } [get_ports
{ddr4_dq[48]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B36                } [get_ports
{ddr4_dq[49]}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B40                } [get_ports
{ddr4_dq[50]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B37                } [get_ports
{ddr4_dq[51]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B42                } [get_ports
{ddr4_dq[52]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A37                } [get_ports
{ddr4_dq[53]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B41                } [get_ports
{ddr4_dq[54]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A38                } [get_ports
{ddr4_dq[55]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B35                } [get_ports
{ddr4_dq[56]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B32                } [get_ports
{ddr4_dq[57]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A33                } [get_ports
{ddr4_dq[58]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN D33                } [get_ports
{ddr4_dq[59]}]

set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A35                } [get_ports
{ddr4_dq[60]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN A34                } [get_ports
{ddr4_dq[61]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN C33                } [get_ports
{ddr4_dq[62]}]
set_property -dict { IOSTANDARD POD12_DCI PACKAGE_PIN B33                } [get_ports
{ddr4_dq[63]}]


#create_clock -name c0_sys_clk -period 4.998 [get_ports diff_clock_rtl_clk_p]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[12]

8.1 Application

SDK template in ./sw_lib/sw_apps/ available.

8.1.1 zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5396 Configuration
    - PCIe and eth reset

8.1.2 zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_teb0912

Hello TEB0912 is a Xilinx Hello World example as endless loop instead of one console output.

12 https://wiki.trenz-electronic.de/display/PD/Vitis

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[13]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set

Change platform-top.h

13 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {




};

&i2c1 {

    i2cswitch@75 { /* u35 */
        compatible = "nxp,pca9544";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x70>;

        i2c@0 { /* DSPLL0*/
                    #address-cells = <1>;
                    #size-cells = <0>;
                    reg = <0>;
        };
        i2c@1 { /* DSPLL1*/
                    #address-cells = <1>;
                    #size-cells = <0>;
                    reg = <1>;
        };
        i2c@2 { /* J34*/
                    #address-cells = <1>;
                    #size-cells = <0>;
                    reg = <2>;
        };
        i2c@3 { /* J34*/
                    #address-cells = <1>;
                    #size-cells = <0>;
                    reg = <3>;
        };
    };
};


/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
```

```
        #size-cells = <1>;
    };
};


/* SD1 with level shifter */
&sdhci1 {
    pinctrl-names = "default";
    pinctrl-0 = <&pinctrl_sdhci1_default>;
};

&pinctrl0 {
    status = "okay";
    pinctrl_sdhci1_default: sdhci1-default {
        mux {
            groups = "sdio1_0_grp";
            function = "sdio1";
        };

        conf {
            groups = "sdio1_0_grp";
            slew-rate = <1>;
            io-standard = <1>;
            bias-disable;
        };
/*
        mux-cd {
            groups = "sdio1_cd_0_grp";
            function = "sdio1_cd";
        };

        conf-cd {
            groups = "sdio1_cd_0_grp";
            bias-high-impedance;
            bias-pull-up;
            slew-rate = <1>;
            io-standard = <1>;
        };

        mux-wp {
            groups = "sdio1_wp_0_grp";
            function = "sdio1_wp";
        };

        conf-wp {
            groups = "sdio1_wp_0_grp";
            bias-high-impedance;
            bias-pull-up;
            slew-rate = <1>;
            io-standard = <1>;
        };
*/

    };
};
```

```
/* ETH PHY */

/*
    mdio {
            #address-cells = <0x1>;
            #size-cells = <0x0>;
            compatible = "cdns,macb-mdio";
            reg = <0x0 0xff0e0000 0x0 0x1000>;
            ethernet_phy0: ethernet-phy@0 {
                    reg = <0>;
                    #address-cells = <0x1>;
                    #size-cells = <0x1>;
            };
            ethernet_phy1: ethernet-phy@1 {
                   reg = <1>;
                   #address-cells = <0x1>;
                   #size-cells = <0x1>;
            };
    };
*/



/* gem1 on REV01 */

&gem2 {
    status = "okay";
    phy-mode = "rgmii-id";
    phy-handle = <ðernet_phy1>;
    ethernet_phy0: ethernet-phy@0 {
            compatible = "marvell,88e1510";
            reg = <0>;
            #address-cells = <0x1>;
            #size-cells = <0x1>;
    };
    ethernet_phy1: ethernet-phy@1 {
           compatible = "marvell,88e1510";
           reg = <1>;
           #address-cells = <0x1>;
           #size-cells = <0x1>;
    };
};


&gem3 {
    status = "okay";
    phy-mode = "rgmii-id";
    phy-handle = <ðernet_phy0>;
};



/* USB  REV01 only */
```

```
/*
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
     snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};
 */
```

9.4 Kernel

Start with **petalinux-config -c kernel**

- Changes:
- # CONFIG_CPU_IDLE is not set
- # CONFIG_CPU_FREQ is not set
- CONFIG_EDAC_CORTEX_ARM64=y
- CONFIG_NVME_CORE=y
- CONFIG_BLK_DEV_NVME=y
- # CONFIG_NVME_MULTIPATH is not set
- CONFIG_NVME_TARGET=y
- # CONFIG_NVME_TARGET_LOOP is not set
- # CONFIG_NVME_TARGET_FC is not set
- CONFIG_NVM=y
- CONFIG_NVM_PBLK=y
- CONFIG_NVM_PBLK_DEBUG=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)

- CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

See: \os\petalinux\project-spec\meta-user\recipes-apps\

9.6.1 startup

Script App to load init.sh from SD Card if available.

9.6.2 webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

10 Additional Software

No additional software is needed.

10.1 SI5395

File location <design name>/misc/Si5395/Si5395*.slabtimeproj

General documentation how you work with these project will be available on Si5395[14]

14 https://wiki.trenz-electronic.de/display/PD/Si5395

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-06-10	v.3(see page 6)	John Hartfiel[15]	• 2019.2 release
--	all	John Hartfiel[16]	--

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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15 https://wiki.trenz-electronic.de/display/~j.hartfiel
16 https://wiki.trenz-electronic.de/display/~j.hartfiel

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union.

17 http://guidance.echa.europa.eu/
18 https://echa.europa.eu/candidate-list-table
19 http://www.echa.europa.eu/

Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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