U_FPGA
FPGA.SchDoc

U_SODIMM
SODIMM.SchDoc

U_CLOCK
CLOCK.SchDoc

U_POWER
POWER.SchDoc

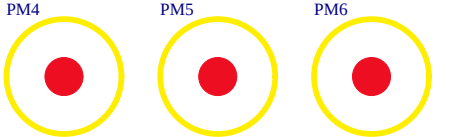
U_CONN
CONN.SchDoc

U_CPLD
CPLD.SchDoc

PM1 PM2 PM3

FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

PM4 PM5 PM6



FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

Serial
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

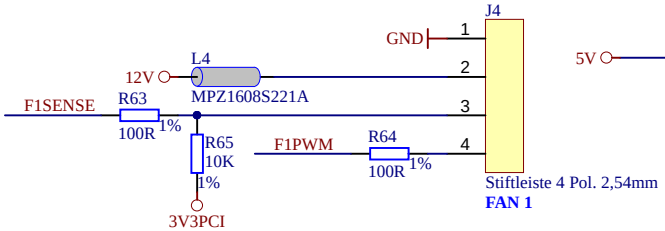
trenz electronic

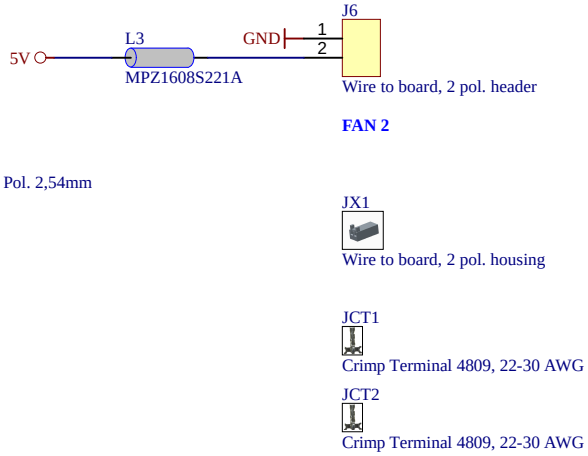
Title: TEC0330 - Overview			
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page1 of 38
Filename: TEC0330.SchDoc			

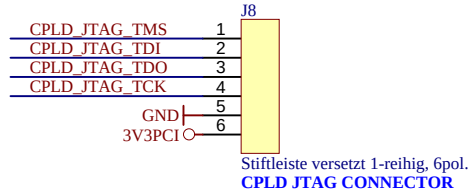
U_FMC
FMC.SchDoc

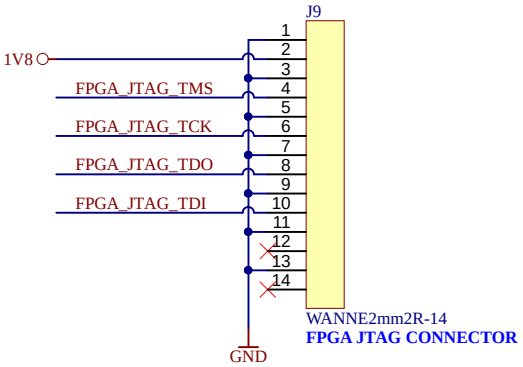
U_PCIE_CONN
PCIE_CONN.SchDoc

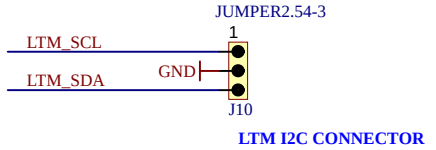
U_MLVDS_CONN
MLVDS_CONN.SchDoc





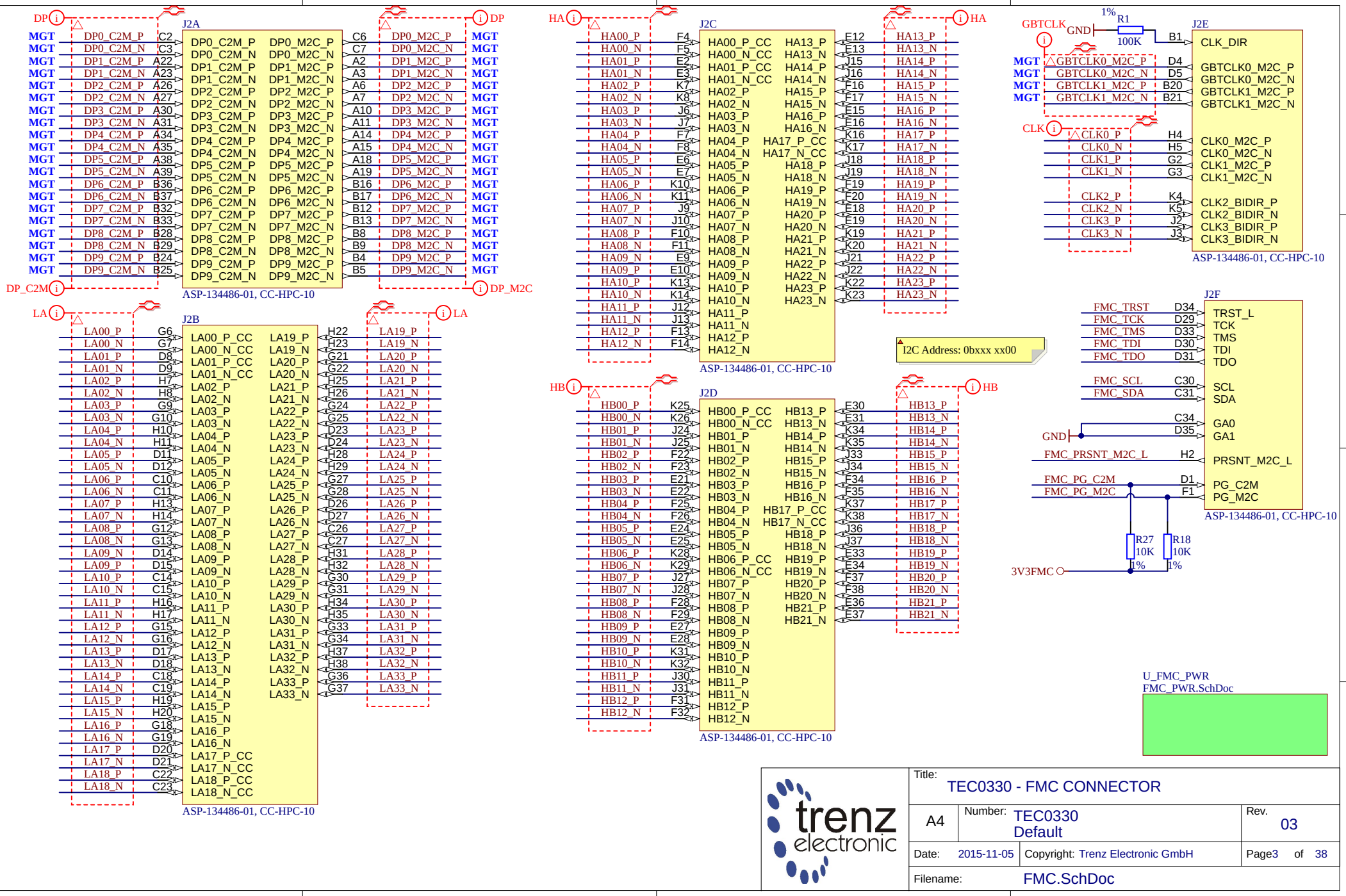






trenz electronic

Title: TEC0330 - CONNECTORS			
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page2 of 38
Filename: CONN.SchDoc			


DP
J2A
DP0_C2M_P C2
DP0_C2M_N C3
DP1_C2M_P A22
DP1_C2M_N A23
DP2_C2M_P A26
DP2_C2M_N A27
DP3_C2M_P A30
DP3_C2M_N A31
DP4_C2M_P A34
DP4_C2M_N A35
DP5_C2M_P A38
DP5_C2M_N A39
DP6_C2M_P B36
DP6_C2M_N B37
DP7_C2M_P B32
DP7_C2M_N B33
DP8_C2M_P B28
DP8_C2M_N B29
DP9_C2M_P B24
DP9_C2M_N B25
DP_C2M
DP0_M2C_P C6
DP0_M2C_N C7
DP1_M2C_P A2
DP1_M2C_N A3
DP2_M2C_P A6
DP2_M2C_N A7
DP3_M2C_P A10
DP3_M2C_N A11
DP4_M2C_P A14
DP4_M2C_N A15
DP5_M2C_P A18
DP5_M2C_N A19
DP6_M2C_P B16
DP6_M2C_N B17
DP7_M2C_P B12
DP7_M2C_N B13
DP8_M2C_P B8
DP8_M2C_N B9
DP9_M2C_P B4
DP9_M2C_N B5
DP_M2C
ASP-134486-01, CC-HPC-10
LA
J2B
LA00_P G6
LA00_N G7
LA01_P D8
LA01_N D9
LA02_P H7
LA02_N H8
LA03_P G9
LA03_N G10
LA04_P H10
LA04_N H11
LA05_P D11
LA05_N D12
LA06_P C10
LA06_N C11
LA07_P H13
LA07_N H14
LA08_P G12
LA08_N G13
LA09_P D14
LA09_N D15
LA10_P C14
LA10_N C15
LA11_P H16
LA11_N H17
LA12_P G15
LA12_N G16
LA13_P D17
LA13_N D18
LA14_P C18
LA14_N C19
LA15_P H19
LA15_N H20
LA16_P G18
LA16_N G19
LA17_P D20
LA17_N D21
LA18_P C22
LA18_N C23
LA00_P_CC
LA00_N_CC
LA01_P_CC
LA01_N_CC
LA02_P
LA02_N
LA03_P
LA03_N
LA04_P
LA04_N
LA05_P
LA05_N
LA06_P
LA06_N
LA07_P
LA07_N
LA08_P
LA08_N
LA09_P
LA09_N
LA10_P
LA10_N
LA11_P
LA11_N
LA12_P
LA12_N
LA13_P
LA13_N
LA14_P
LA14_N
LA15_P
LA15_N
LA16_P
LA16_N
LA17_P_CC
LA17_N_CC
LA18_P_CC
LA18_N_CC
LA19_P H22
LA19_N H23
LA20_P G21
LA20_N G22
LA21_P H25
LA21_N H26
LA22_P G24
LA22_N G25
LA23_P D23
LA23_N D24
LA24_P H28
LA24_N H29
LA25_P G27
LA25_N G28
LA26_P D26
LA26_N D27
LA27_P C26
LA27_N C27
LA28_P H31
LA28_N H32
LA29_P G30
LA29_N G31
LA30_P H34
LA30_N H35
LA31_P G33
LA31_N G34
LA32_P H37
LA32_N H38
LA33_P G36
LA33_N G37
ASP-134486-01, CC-HPC-10
HA
J2C
HA00_P F4
HA00_N F5
HA01_P E2
HA01_N E3
HA02_P K7
HA02_N K8
HA03_P J6
HA03_N J7
HA04_P F7
HA04_N F8
HA05_P E6
HA05_N E7
HA06_P K10
HA06_N K11
HA07_P J9
HA07_N J10
HA08_P F10
HA08_N F11
HA09_N E9
HA09_P E10
HA10_P K13
HA10_N K14
HA11_P J12
HA11_N J13
HA12_P F13
HA12_N F14
HA00_P_CC
HA00_N_CC
HA01_P_CC
HA01_N_CC
HA02_P
HA02_N
HA03_P
HA03_N
HA04_P
HA04_N
HA05_P
HA05_N
HA06_P
HA06_N
HA07_P
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HA08_P
HA08_N
HA09_P
HA09_N
HA10_P
HA10_N
HA11_P
HA11_N
HA12_P
HA12_N
HA13_P E12
HA13_N E13
HA14_P J15
HA14_N J16
HA15_P F16
HA15_N F17
HA16_P E15
HA16_N E16
HA17_P K16
HA17_N K17
HA18_P J18
HA18_N J19
HA19_P F19
HA19_N F20
HA20_P E18
HA20_N E19
HA21_P K19
HA21_N K20
HA22_P J21
HA22_N J22
HA23_P K22
HA23_N K23
ASP-134486-01, CC-HPC-10
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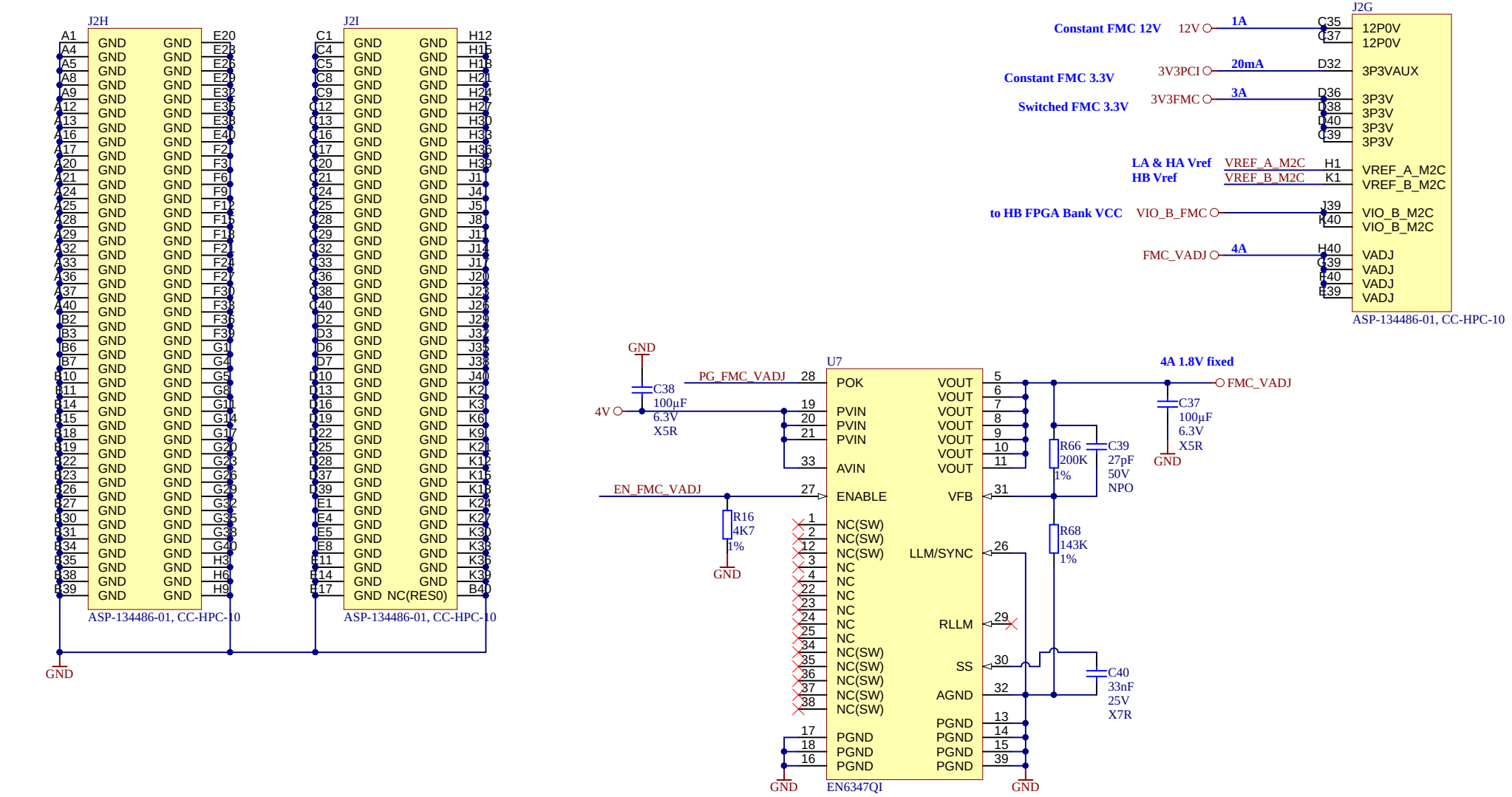
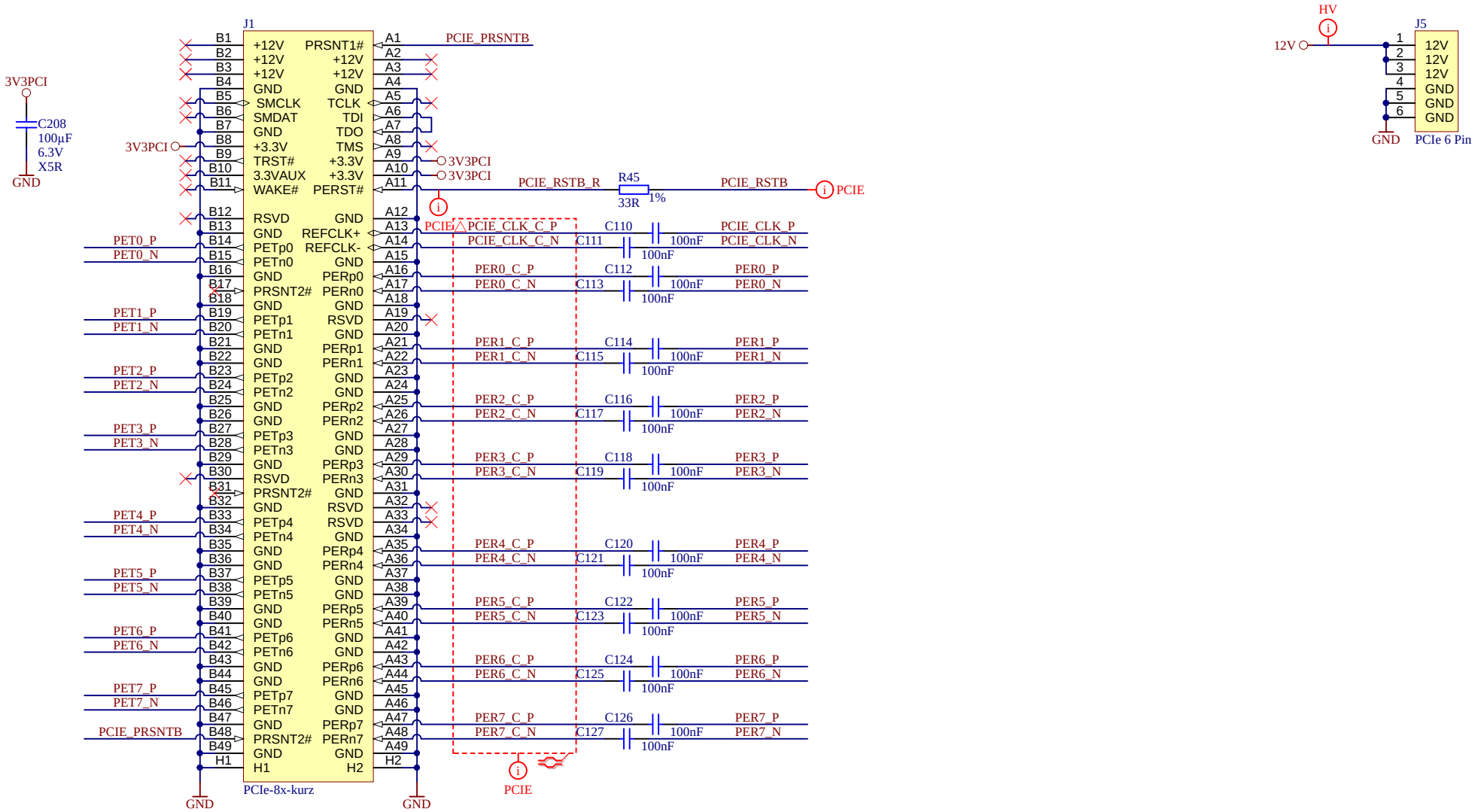
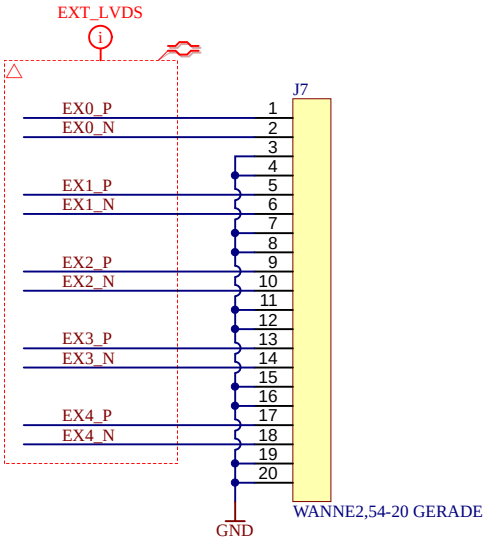
J2D
HB00_P K25
HB00_N K26
HB01_P J24
HB01_N J25
HB02_P F22
HB02_N F23
HB03_P E21
HB03_N E22
HB04_P F25
HB04_N F26
HB05_P E24
HB05_N E25
HB06_P K28
HB06_N K29
HB07_P J27
HB07_N J28
HB08_P F28
HB08_N F29
HB09_P E27
HB09_N E28
HB10_P K31
HB10_N K32
HB11_P J30
HB11_N J31
HB12_P F31
HB12_N F32
HB00_P_CC
HB00_N_CC
HB01_P
HB01_N
HB02_P
HB02_N
HB03_P
HB03_N
HB04_P
HB04_N
HB05_P
HB05_N
HB06_P
HB06_N
HB07_P
HB07_N
HB08_P
HB08_N
HB09_P
HB09_N
HB10_P
HB10_N
HB11_P
HB11_N
HB12_P
HB12_N
HB13_P E30
HB13_N E31
HB14_P K34
HB14_N K35
HB15_P J33
HB15_N J34
HB16_P F34
HB16_N F35
HB17_P K37
HB17_N K38
HB18_P J36
HB18_N J37
HB19_P E33
HB19_N E34
HB20_P F37
HB20_N F38
HB21_P E36
HB21_N E37
ASP-134486-01, CC-HPC-10
I2C Address: 0bxxx xx00
GBTCLK
GND
1%
R1
100K
J2E
CLK_DIR B1
GBTCLK0_M2C_P D4
GBTCLK0_M2C_N D5
GBTCLK1_M2C_P B20
GBTCLK1_M2C_N B21
CLK0_M2C_P H4
CLK0_M2C_N H5
CLK1_M2C_P G2
CLK1_M2C_N G3
CLK2_BIDIR_P K4
CLK2_BIDIR_N K5
CLK3_BIDIR_P J2
CLK3_BIDIR_N J3
ASP-134486-01, CC-HPC-10
J2F
TRST_L FMC_TRST D34
TCK FMC_TCK D29
TMS FMC_TMS D33
TDI FMC_TDI D30
TDO FMC_TDO D31
SCL FMC_SCL C30
SDA FMC_SDA C31
GA0 C34
GA1 D35
PRSNT_M2C_L H2
PG_C2M FMC_PG_C2M D1
PG_M2C FMC_PG_M2C F1
ASP-134486-01, CC-HPC-10
R27 10K 1%
R18 10K 1%
3V3FMC
U_FMC_PWR
FMC_PWR.SchDoc
trenz electronic
Title: TEC0330 - FMC CONNECTOR
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
Page3 of 38
Filename: FMC.SchDoc



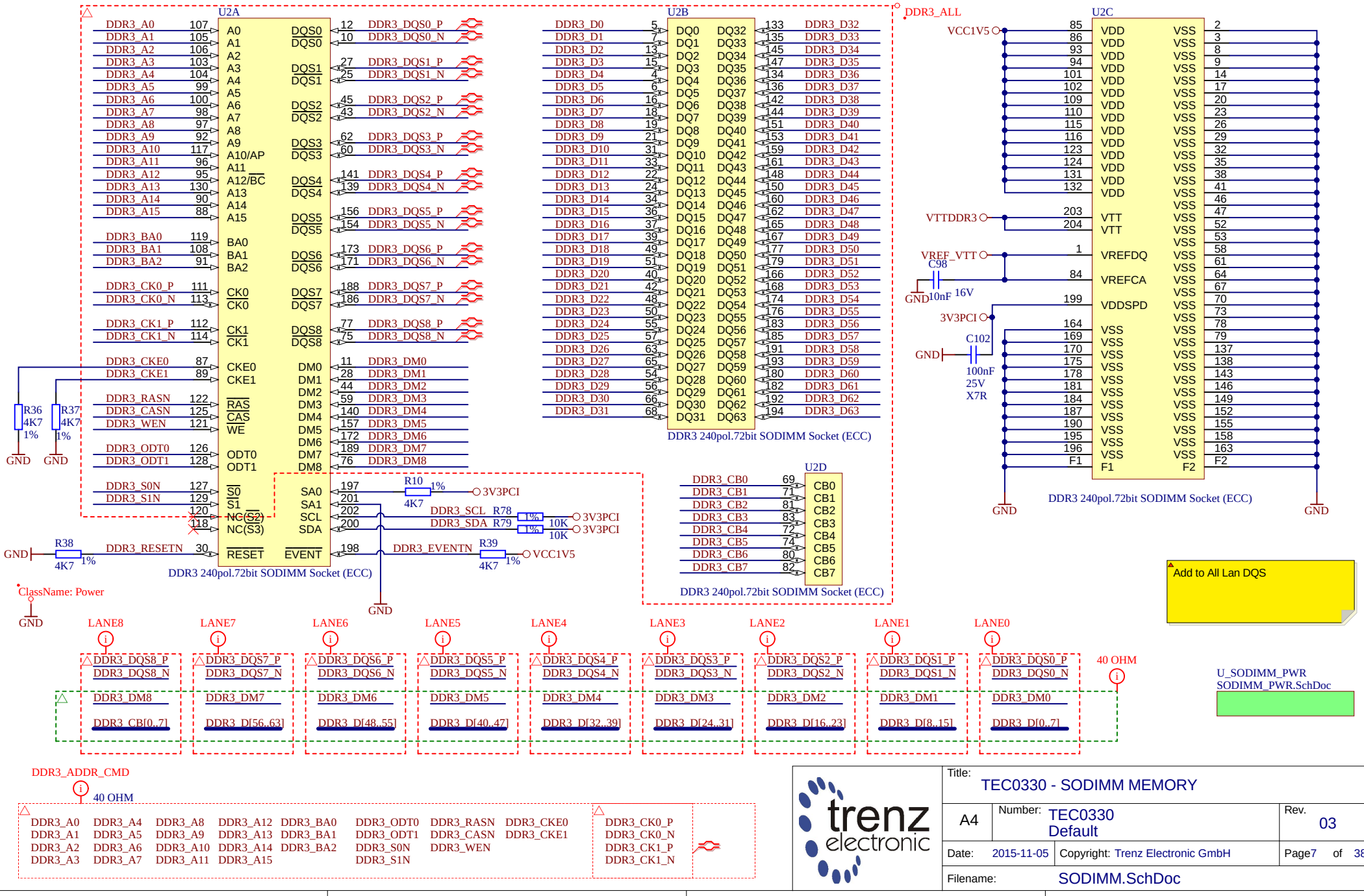
Title:	TEC0330 - FMC CONNECTOR POWER		
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page4 of 38
Filename:	FMC_PWR.SchDoc		



trenz electronic	Title: TEC0330 - PCIE CONNECTOR		
	A4	Number: TEC0330 Default	Rev. 03
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page5 of 38
	Filename: PCIE_CONN.SchDoc		



trenz electronic	Title: TEC0330 - MLVDS CONNECTOR		
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page6 of 38
Filename: MLVDS_CONN.SchDoc			


U2A
DDR3 240pol.72bit SODIMM Socket (ECC)
U2B
DDR3 240pol.72bit SODIMM Socket (ECC)
U2C
DDR3 240pol.72bit SODIMM Socket (ECC)
U2D
DDR3 240pol.72bit SODIMM Socket (ECC)
DDR3_ALL
VCC1V5
VTTDDR3
VREF_VTT
C98
10nF 16V
3V3PCI
C102
100nF
25V
X7R
GND
R36
4K7
1%
R37
4K7
1%
R10
4K7
1%
3V3PCI
DDR3_SCL R78
DDR3_SDA R79
10K
10K
R38
4K7
1%
DDR3_RESETN
R39
4K7
1%
VCC1V5
DDR3_EVENTN
ClassName: Power
Add to All Lan DQS
LANE8
LANE7
LANE6
LANE5
LANE4
LANE3
LANE2
LANE1
LANE0
40 OHM
U_SODIMM_PWR
SODIMM_PWR.SchDoc
DDR3_ADDR_CMD
40 OHM
DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14 DDR3_A15 DDR3_BA0 DDR3_BA1 DDR3_BA2 DDR3_ODT0 DDR3_ODT1 DDR3_S0N DDR3_S1N DDR3_RASN DDR3_CASN DDR3_WEN DDR3_CKE0 DDR3_CKE1
DDR3_CK0_P DDR3_CK0_N DDR3_CK1_P DDR3_CK1_N
trenz electronic
Title: TEC0330 - SODIMM MEMORY
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
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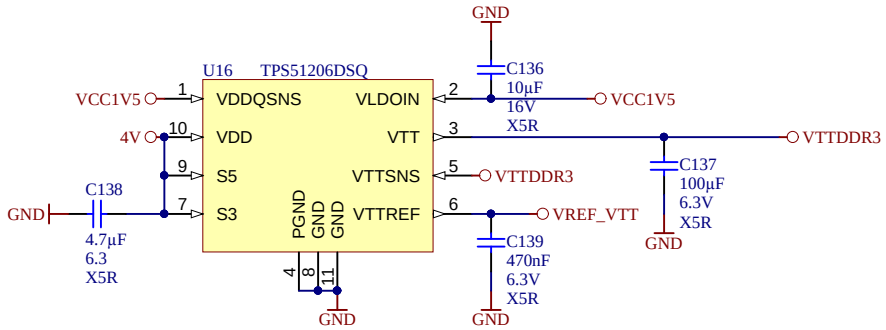
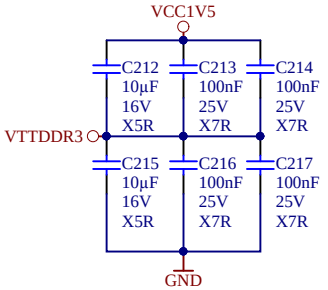
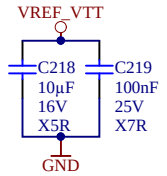
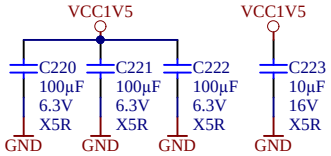
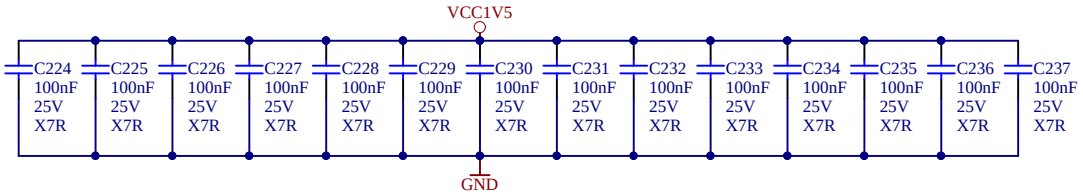
Filename: SODIMM.SchDoc



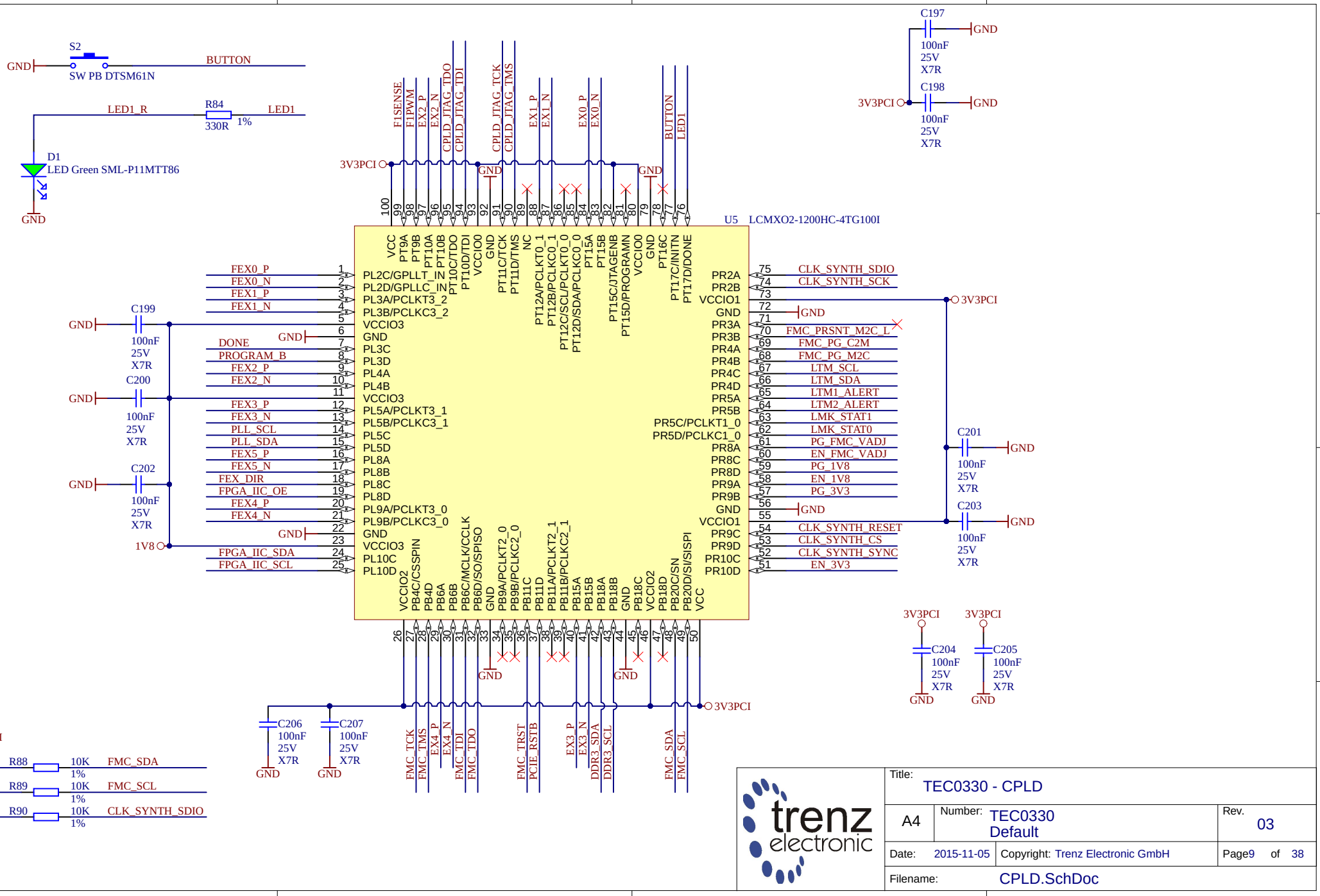






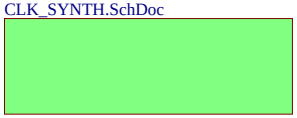


trenz electronic	Title: TEC0330 - SODIMM MEMORY		
	A4	Number: TEC0330 Default	Rev. 03
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page 8 of 38
	Filename: SODIMM_PWR.SchDoc		

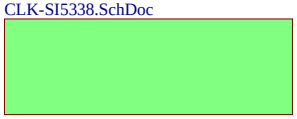


Title:	TEC0330 - CPLD		
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page9 of 38
Filename:	CPLD.SchDoc		

U_CLK_SYNTH
CLK_SYNTH.SchDoc



U_CLK-SI5338
CLK-SI5338.SchDoc



	Title: TEC0330 - CLOCKS		
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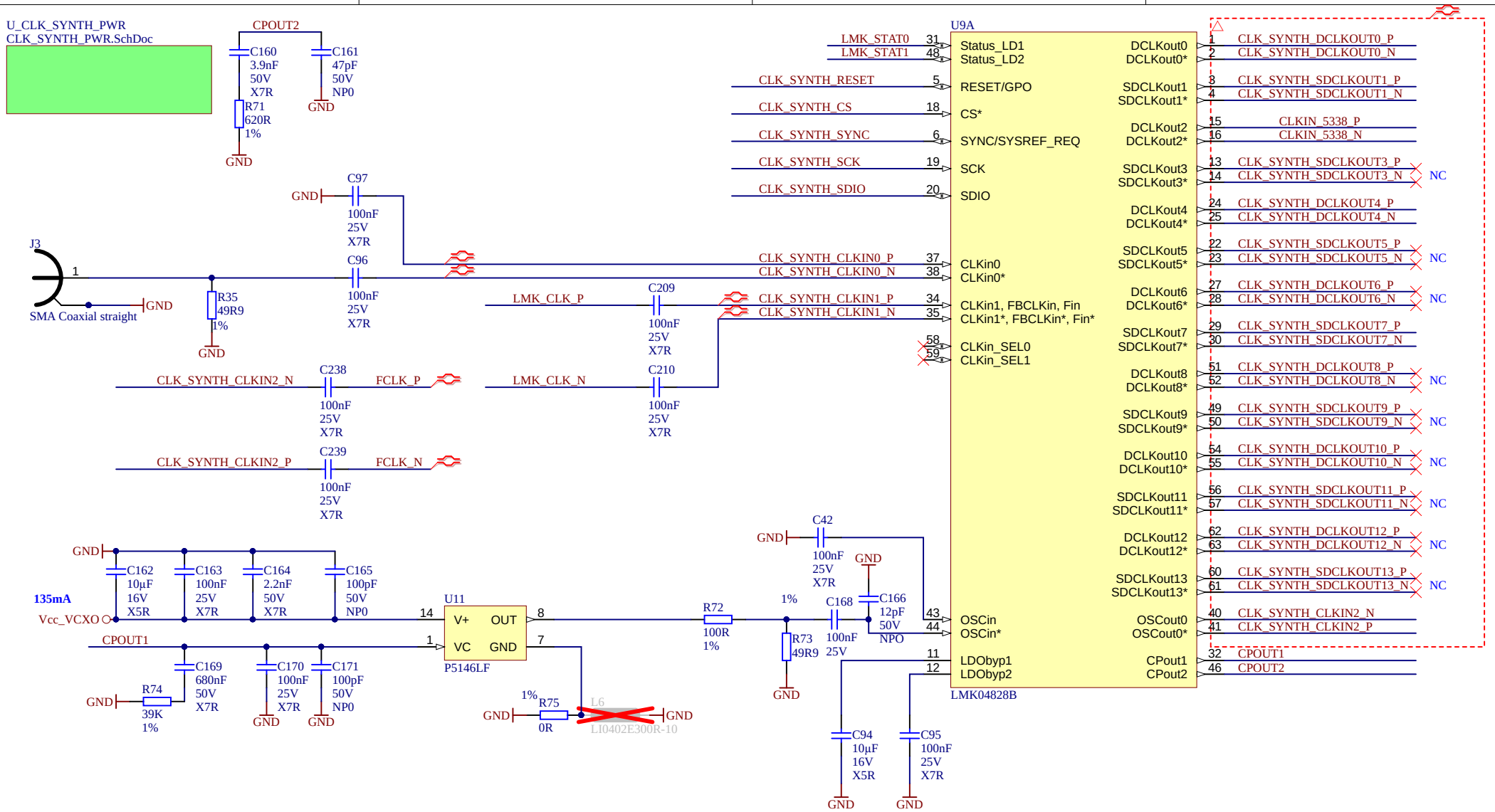
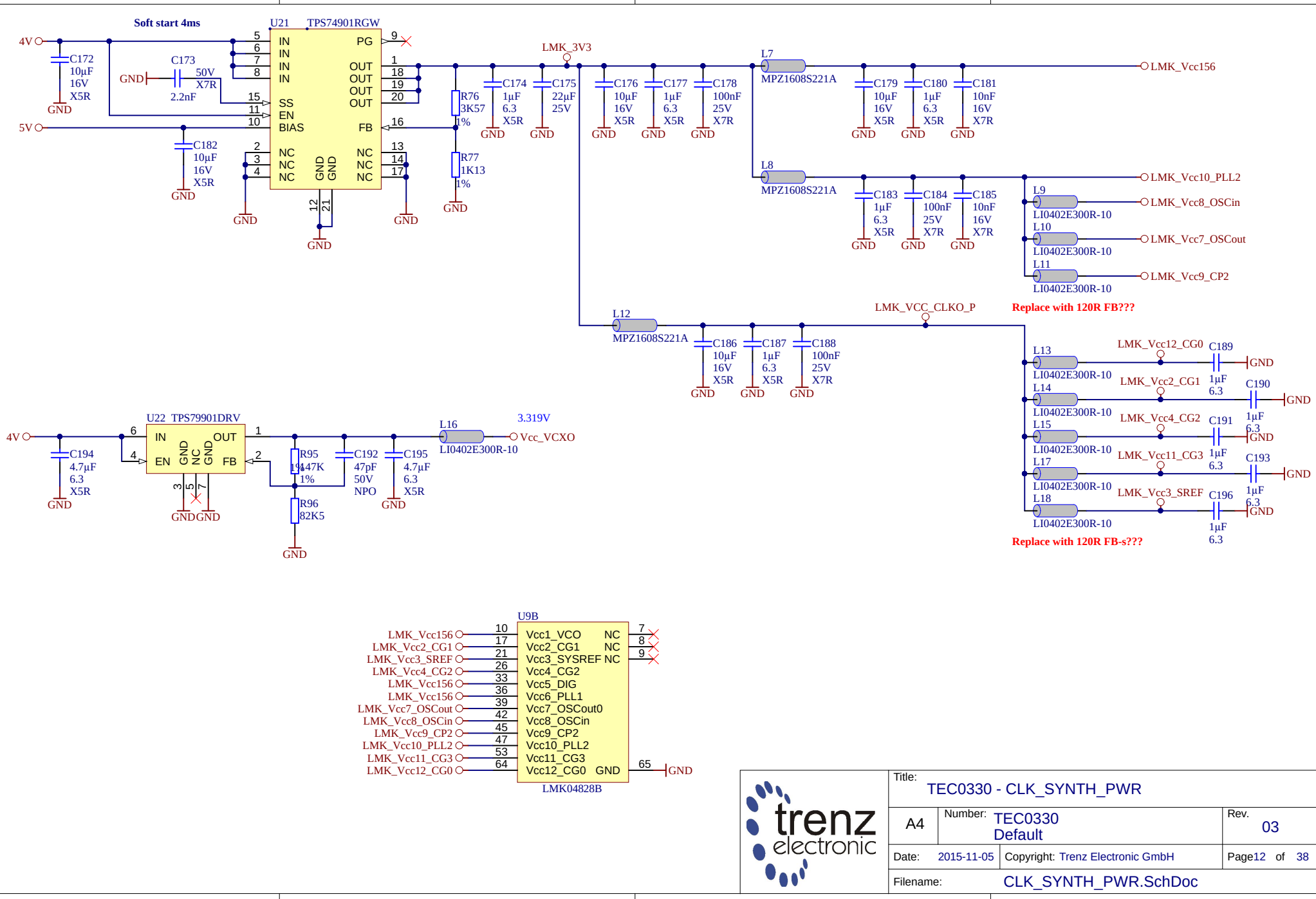
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page10 of 38
Filename: CLOCK.SchDoc			


U_CLK_SYNTH_PWR
CLK_SYNTH_PWR.SchDoc
CPOUT2
C160 3.9nF 50V X7R
C161 47pF 50V NP0
R71 620R 1%
GND
C97 100nF 25V X7R
J3
SMA Coaxial straight
R35 49R9 1%
C96 100nF 25V X7R
C209 100nF 25V X7R
C238 100nF 25V X7R
C239 100nF 25V X7R
C210 100nF 25V X7R
CLK_SYNTH_CLKIN2_N
CLK_SYNTH_CLKIN2_P
FCLK_P
FCLK_N
LMK_CLK_P
LMK_CLK_N
135mA
Vcc_VCXO
C162 10µF 16V X5R
C163 100nF 25V X7R
C164 2.2nF 50V X7R
C165 100pF 50V NP0
U11
P5146LF
V+ OUT VC GND
CPOUT1
C169 680nF 50V X7R
C170 100nF 25V X7R
C171 100pF 50V NP0
R74 39K 1%
R75 0R
L6
LI0402E300R-10
R72 100R 1%
C42 100nF 25V X7R
C166 12pF 50V NPO
R73 49R9 1%
C168 100nF 25V
C94 10µF 16V X5R
C95 100nF 25V X7R
U9A
LMK04828B
LMK_STAT0
LMK_STAT1
CLK_SYNTH_RESET
CLK_SYNTH_CS
CLK_SYNTH_SYNC
CLK_SYNTH_SCK
CLK_SYNTH_SDIO
Status_LD1
Status_LD2
RESET/GPO
CS*
SYNC/SYSREF_REQ
SCK
SDIO
CLKin0
CLKin0*
CLKin1, FBCLKin, Fin
CLKin1*, FBCLKin*, Fin*
CLKin_SEL0
CLKin_SEL1
OSCin
OSCin*
LDObyp1
LDObyp2
DCLKout0
DCLKout0*
SDCLKout1
SDCLKout1*
DCLKout2
DCLKout2*
SDCLKout3
SDCLKout3*
DCLKout4
DCLKout4*
SDCLKout5
SDCLKout5*
DCLKout6
DCLKout6*
SDCLKout7
SDCLKout7*
DCLKout8
DCLKout8*
SDCLKout9
SDCLKout9*
DCLKout10
DCLKout10*
SDCLKout11
SDCLKout11*
DCLKout12
DCLKout12*
SDCLKout13
SDCLKout13*
OSCout0
OSCout0*
CPout1
CPout2
CLK_SYNTH_DCLKOUT0_P
CLK_SYNTH_DCLKOUT0_N
CLK_SYNTH_SDCLKOUT1_P
CLK_SYNTH_SDCLKOUT1_N
CLKIN_5338_P
CLKIN_5338_N
CLK_SYNTH_SDCLKOUT3_P
CLK_SYNTH_SDCLKOUT3_N
CLK_SYNTH_DCLKOUT4_P
CLK_SYNTH_DCLKOUT4_N
CLK_SYNTH_SDCLKOUT5_P
CLK_SYNTH_SDCLKOUT5_N
CLK_SYNTH_DCLKOUT6_P
CLK_SYNTH_DCLKOUT6_N
CLK_SYNTH_SDCLKOUT7_P
CLK_SYNTH_SDCLKOUT7_N
CLK_SYNTH_DCLKOUT8_P
CLK_SYNTH_DCLKOUT8_N
CLK_SYNTH_SDCLKOUT9_P
CLK_SYNTH_SDCLKOUT9_N
CLK_SYNTH_DCLKOUT10_P
CLK_SYNTH_DCLKOUT10_N
CLK_SYNTH_SDCLKOUT11_P
CLK_SYNTH_SDCLKOUT11_N
CLK_SYNTH_DCLKOUT12_P
CLK_SYNTH_DCLKOUT12_N
CLK_SYNTH_SDCLKOUT13_P
CLK_SYNTH_SDCLKOUT13_N
CLK_SYNTH_CLKIN2_N
CLK_SYNTH_CLKIN2_P
CPOUT1
CPOUT2
NC
CLK2_P
CLK2_N
CLK3_P
CLK3_N
trenz electronic
Title: TEC0330 - CLK_SYNTH
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
Page11 of 38
Filename: CLK_SYNTH.SchDoc



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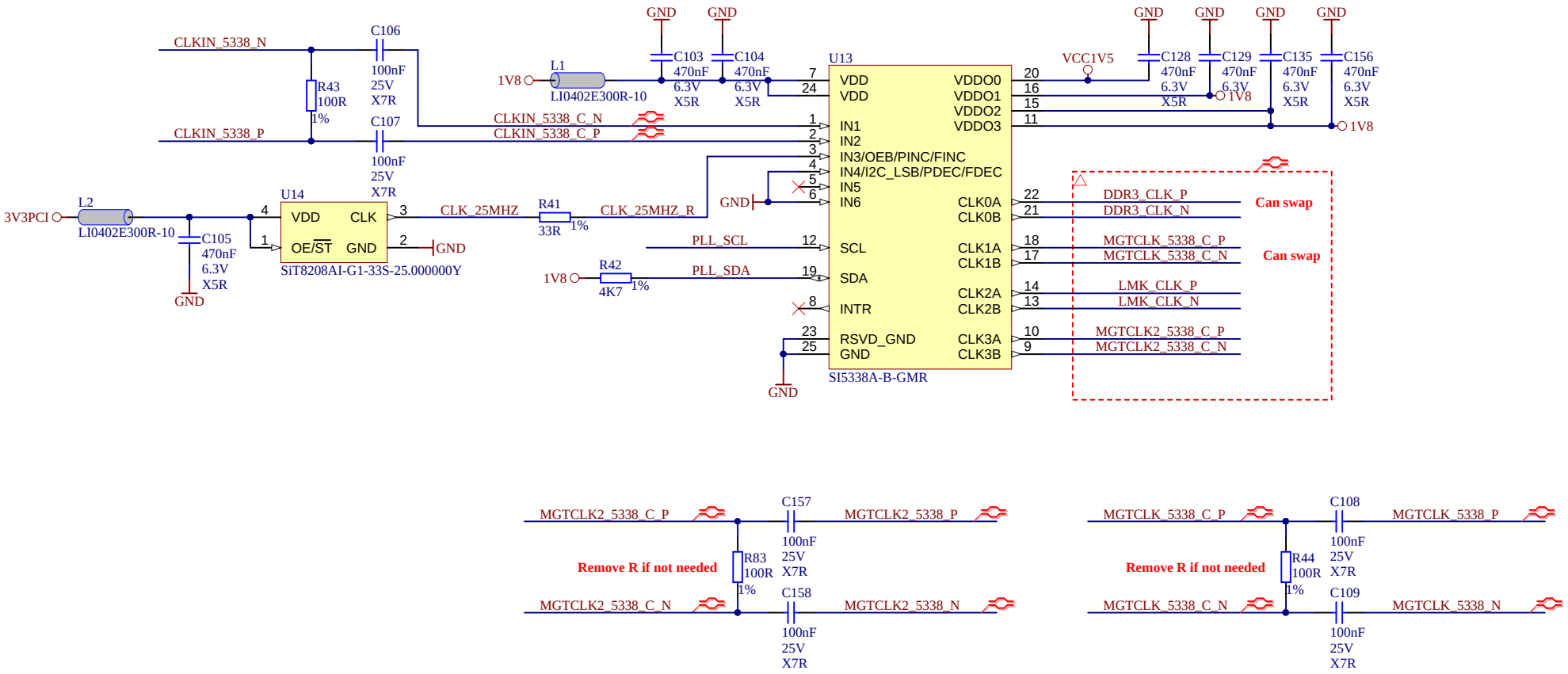
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page12 of 38
Filename: CLK_SYNTH_PWR.SchDoc			



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Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page13 of 38
Filename: CLK-SI5338.SchDoc			

U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

U_FPGA_BANK_16
FPGA_BANK_16.SchDoc

U_FPGA_BANK_17
FPGA_BANK_17.SchDoc

U_FPGA_BANK_18
FPGA_BANK_18.SchDoc

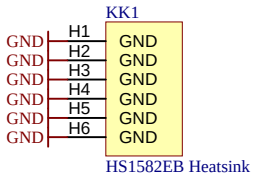
U_DDR_Banks
DDR_Banks.SchDoc

U_FMC_Banks
FMC_Banks.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

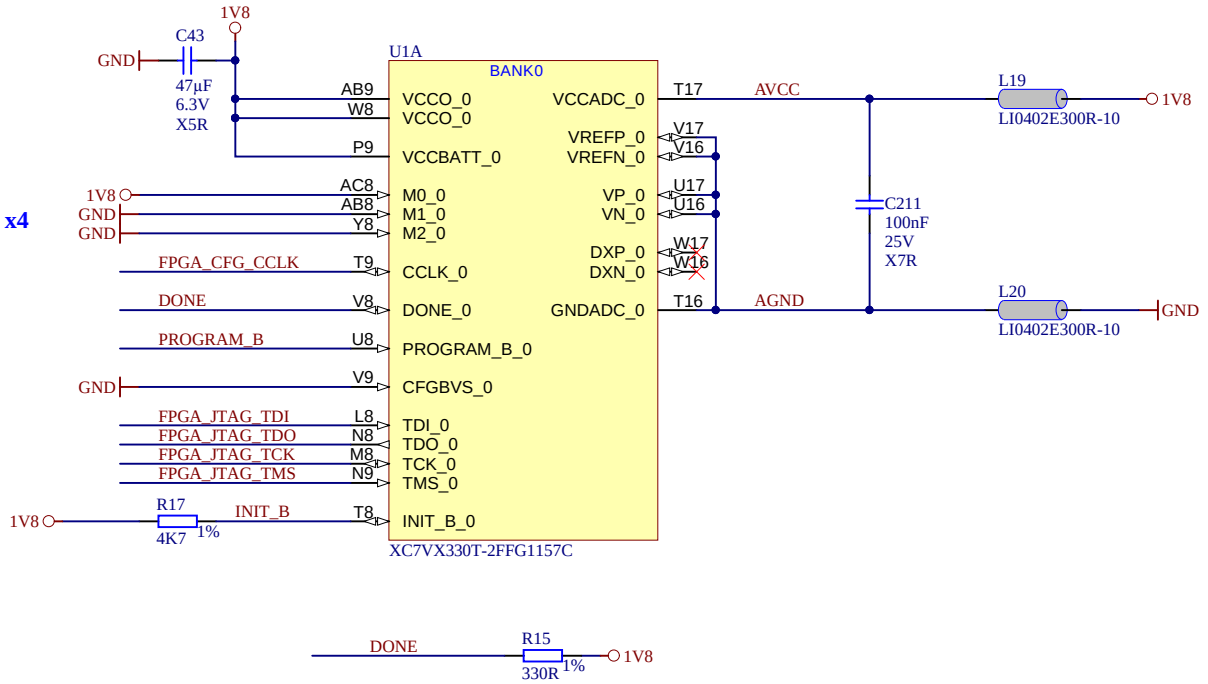
U_FPGA_POWER
FPGA_POWER.SchDoc



trenz electronic

Title: TEC0330 - FPGA			
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page14 of 38
Filename: FPGA.SchDoc			

MASTER SPI x4



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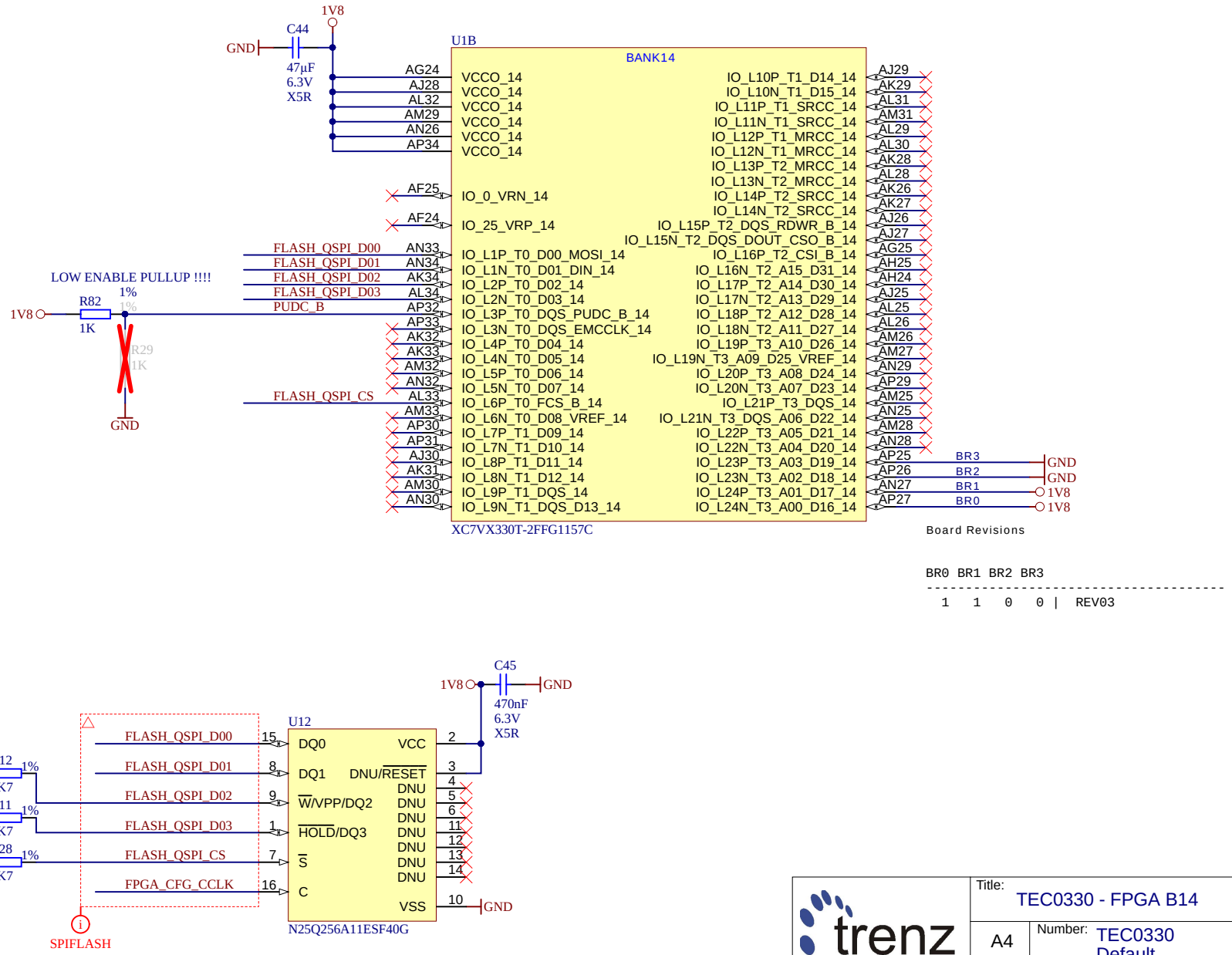
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page15 of 38
Filename: FPGA_CFG.SchDoc			



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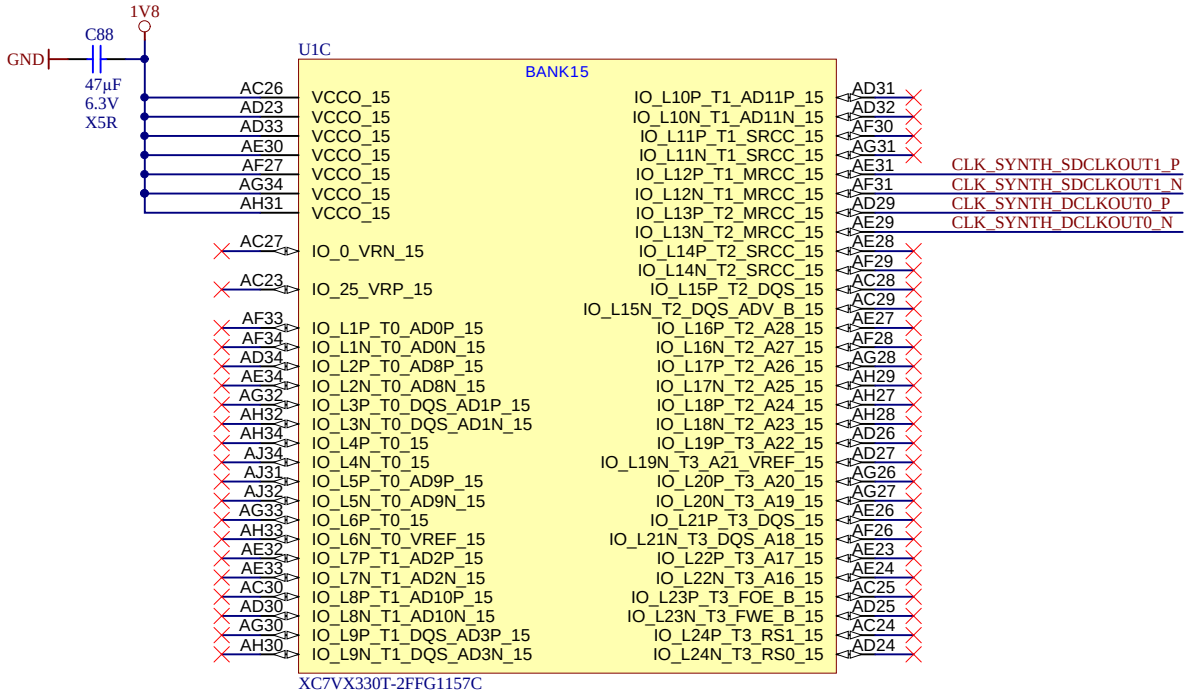
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page16 of 38
	Filename: FPGA_BANK_14.SchDoc		



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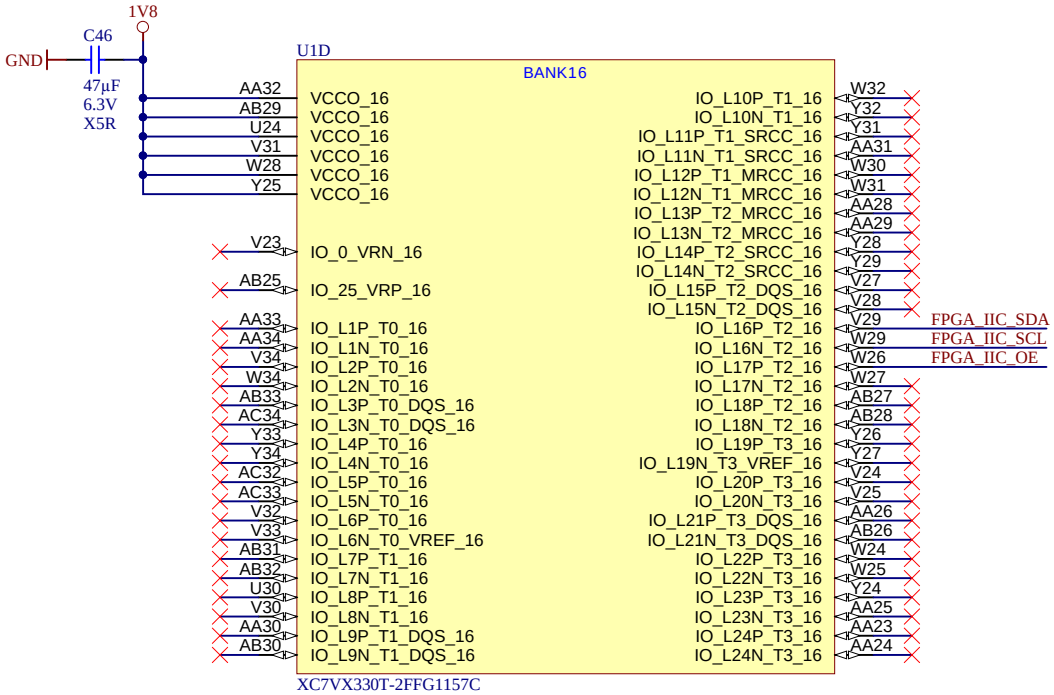
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page17 of 38
	Filename: FPGA_BANK_15.SchDoc		



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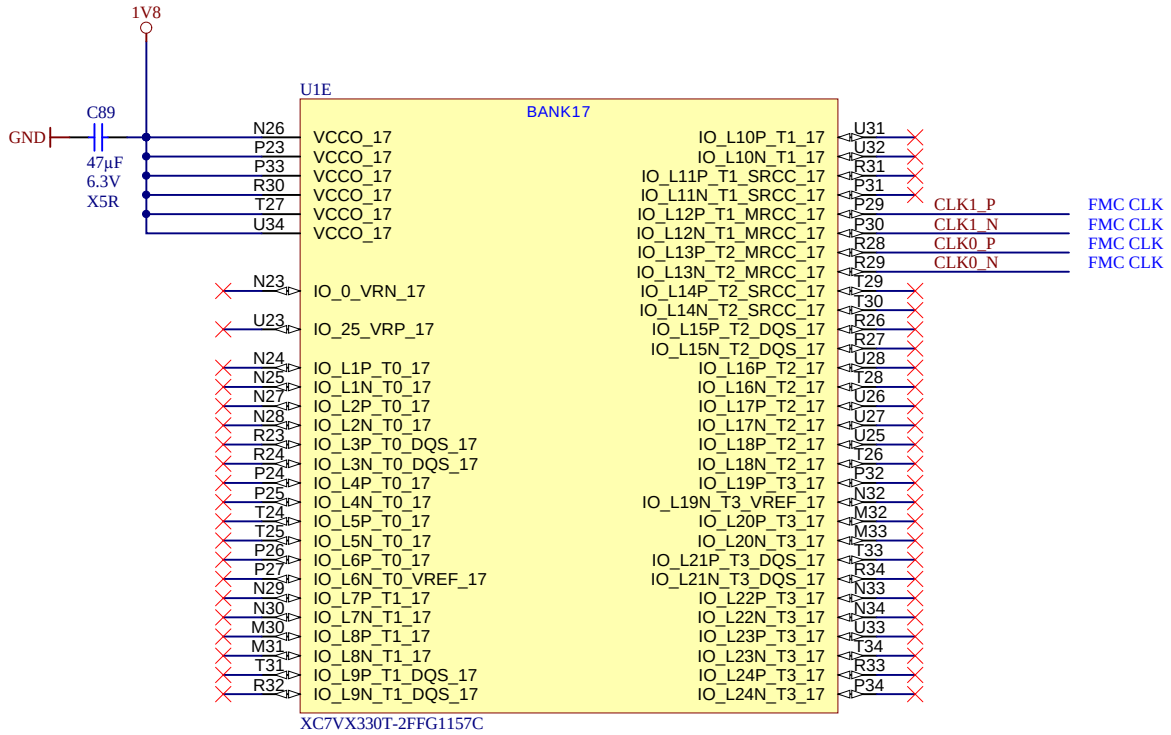
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page18 of 38
	Filename: FPGA_BANK_16.SchDoc		



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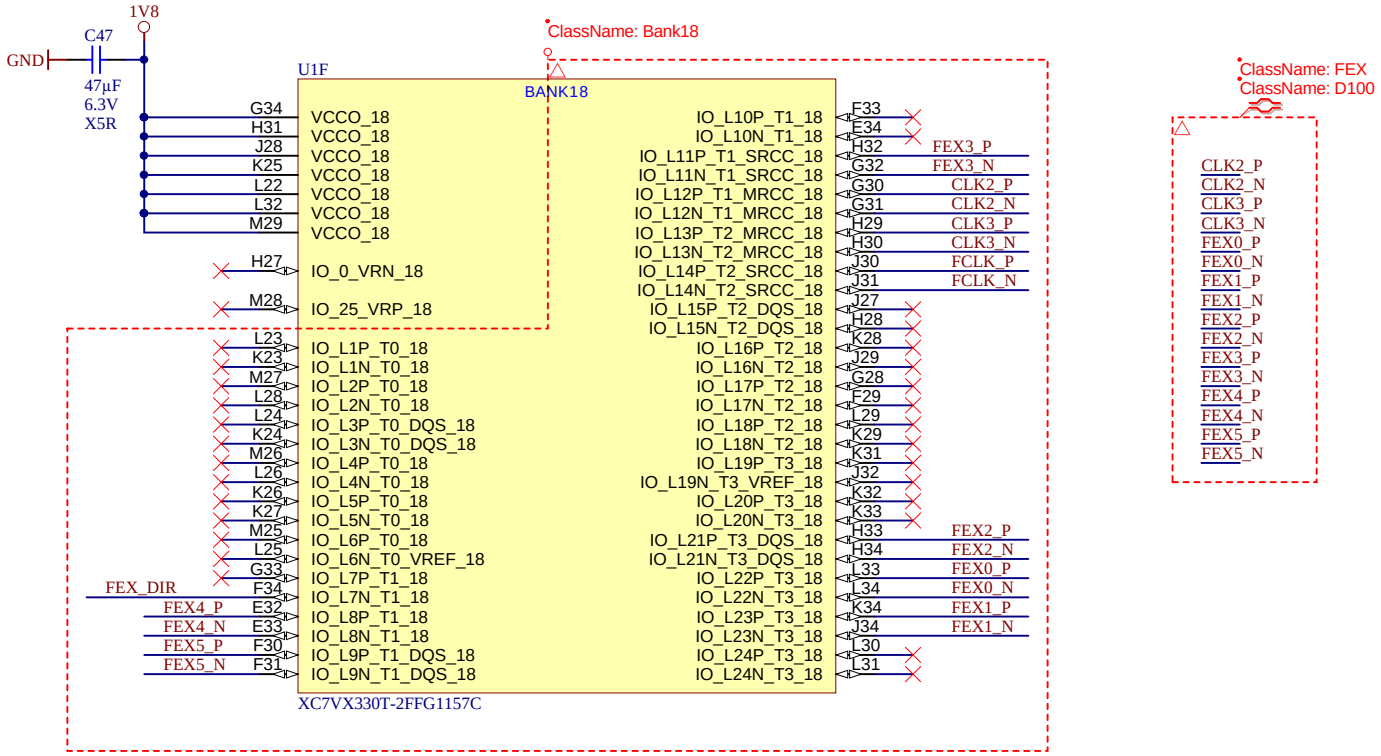
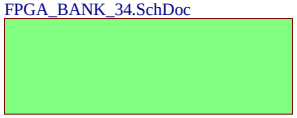
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page19 of 38
	Filename: FPGA_BANK_17.SchDoc		



trenz electronic

Title: TEC0330 - FPGA B18			
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page20 of 38
Filename: FPGA_BANK_18.SchDoc			

U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



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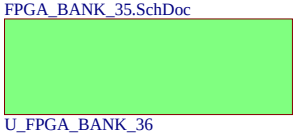
FPGA_BANK_35.SchDoc



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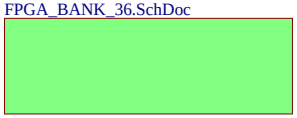
FPGA_BANK_36.SchDoc



trenz electronic	Title: TEC0330 - FPGA_DDR_BANKS		
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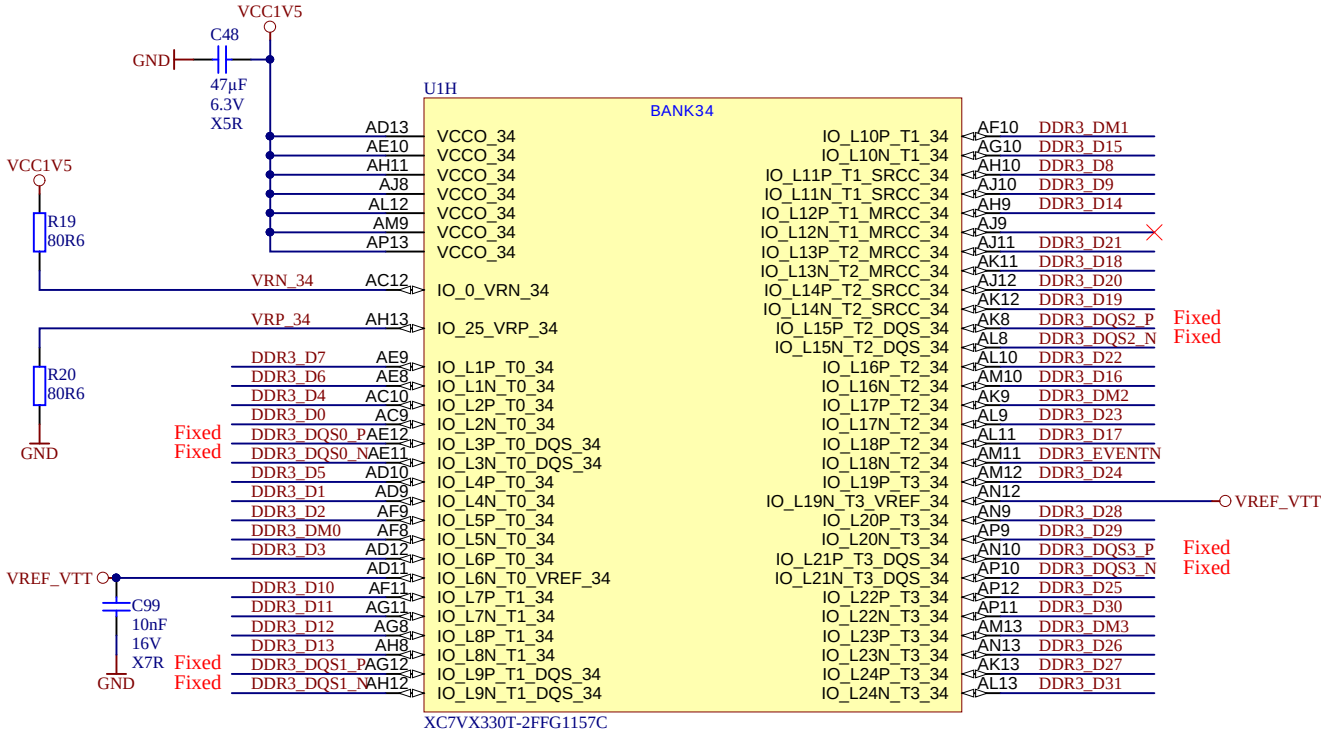
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page 21 of 38
Filename: DDR_Banks.SchDoc			



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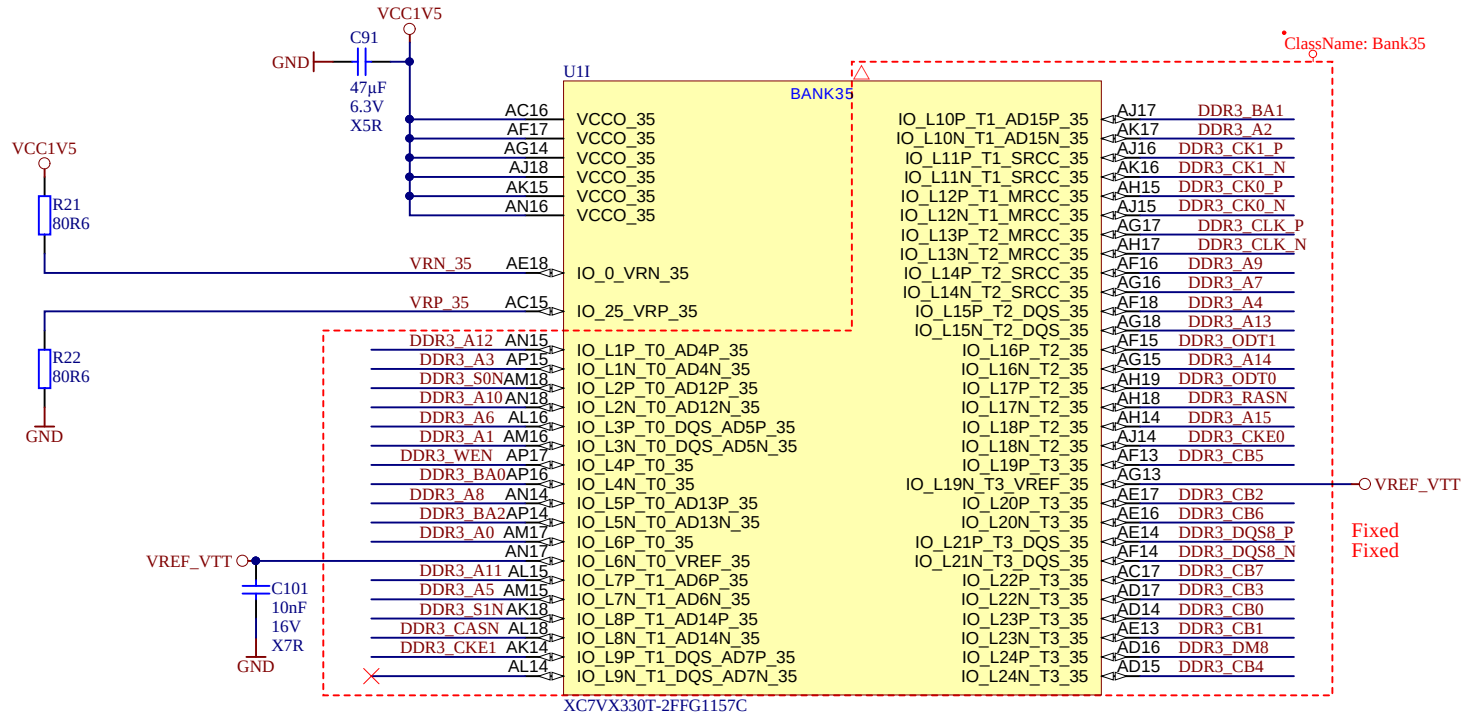
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page22 of 38
Filename: FPGA_BANK_34.SchDoc			



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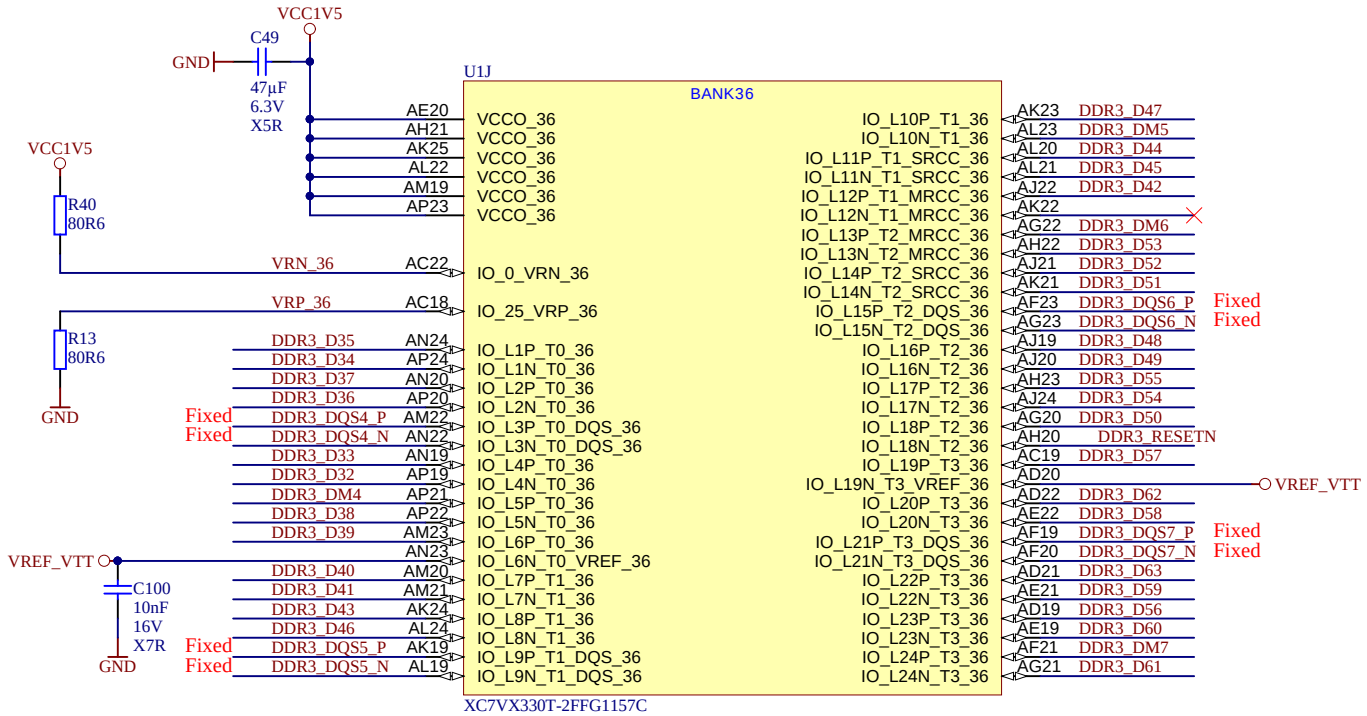
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page23 of 38
	Filename: FPGA_BANK_35.SchDoc		



trenz electronic	Title: TEC0330 - FPGA B36		
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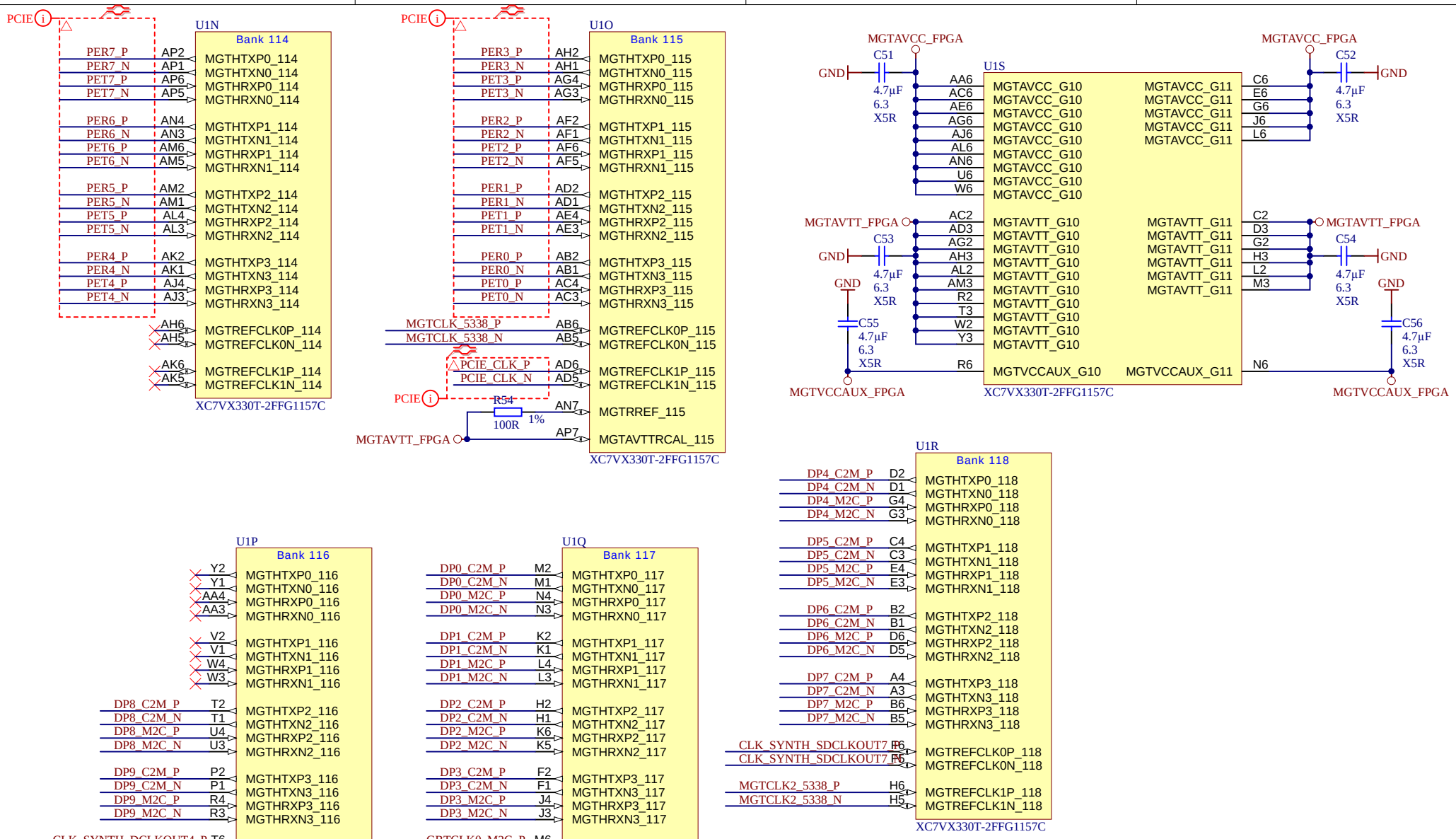
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page24 of 38
	Filename: FPGA_BANK_36.SchDoc		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Bank 114
PER7_P AP2 MGTHTXP0_114
PER7_N AP1 MGTHTXN0_114
PET7_P AP6 MGTHRXP0_114
PET7_N AP5 MGTHRXN0_114
PER6_P AN4 MGTHTXP1_114
PER6_N AN3 MGTHTXN1_114
PET6_P AM6 MGTHRXP1_114
PET6_N AM5 MGTHRXN1_114
PER5_P AM2 MGTHTXP2_114
PER5_N AM1 MGTHTXN2_114
PET5_P AL4 MGTHRXP2_114
PET5_N AL3 MGTHRXN2_114
PER4_P AK2 MGTHTXP3_114
PER4_N AK1 MGTHTXN3_114
PET4_P AJ4 MGTHRXP3_114
PET4_N AJ3 MGTHRXN3_114
AH6 MGTREFCLK0P_114
AH5 MGTREFCLK0N_114
AK6 MGTREFCLK1P_114
AK5 MGTREFCLK1N_114
XC7VX330T-2FFG1157C
U1O
Bank 115
PER3_P AH2 MGTHTXP0_115
PER3_N AH1 MGTHTXN0_115
PET3_P AG4 MGTHRXP0_115
PET3_N AG3 MGTHRXN0_115
PER2_P AF2 MGTHTXP1_115
PER2_N AF1 MGTHTXN1_115
PET2_P AF6 MGTHRXP1_115
PET2_N AF5 MGTHRXN1_115
PER1_P AD2 MGTHTXP2_115
PER1_N AD1 MGTHTXN2_115
PET1_P AE4 MGTHRXP2_115
PET1_N AE3 MGTHRXN2_115
PER0_P AB2 MGTHTXP3_115
PER0_N AB1 MGTHTXN3_115
PET0_P AC4 MGTHRXP3_115
PET0_N AC3 MGTHRXN3_115
MGTCLK_5338_P AB6 MGTREFCLK0P_115
MGTCLK_5338_N AB5 MGTREFCLK0N_115
PCIE_CLK_P AD6 MGTREFCLK1P_115
PCIE_CLK_N AD5 MGTREFCLK1N_115
R54 100R 1%
AN7 MGTRREF_115
MGTAVTT_FPGA AP7 MGTAVTTRCAL_115
XC7VX330T-2FFG1157C
U1S
MGTAVCC_FPGA
C51 4.7µF 6.3 X5R
GND
AA6 AC6 AE6 AG6 AJ6 AL6 AN6 U6 W6
MGTAVCC_G10
MGTAVCC_G11
C6 E6 G6 J6 L6
C52 4.7µF 6.3 X5R
MGTAVTT_FPGA
C53 4.7µF 6.3 X5R
AC2 AD3 AG2 AH3 AL2 AM3 R2 T3 W2 Y3
MGTAVTT_G10
MGTAVTT_G11
C2 D3 G2 H3 L2 M3
C54 4.7µF 6.3 X5R
C55 4.7µF 6.3 X5R
R6
MGTVCCAUX_G10
MGTVCCAUX_G11
N6
C56 4.7µF 6.3 X5R
MGTVCCAUX_FPGA
XC7VX330T-2FFG1157C
U1R
Bank 118
DP4_C2M_P D2 DP4_C2M_N D1 DP4_M2C_P G4 DP4_M2C_N G3
DP5_C2M_P C4 DP5_C2M_N C3 DP5_M2C_P E4 DP5_M2C_N E3
DP6_C2M_P B2 DP6_C2M_N B1 DP6_M2C_P D6 DP6_M2C_N D5
DP7_C2M_P A4 DP7_C2M_N A3 DP7_M2C_P B6 DP7_M2C_N B5
MGTHTXP0_118 MGTHTXN0_118 MGTHRXP0_118 MGTHRXN0_118
MGTHTXP1_118 MGTHTXN1_118 MGTHRXP1_118 MGTHRXN1_118
MGTHTXP2_118 MGTHTXN2_118 MGTHRXP2_118 MGTHRXN2_118
MGTHTXP3_118 MGTHTXN3_118 MGTHRXP3_118 MGTHRXN3_118
CLK_SYNTH_SDCLKOUT7_P H6
CLK_SYNTH_SDCLKOUT7_N H5
MGTREFCLK0P_118
MGTREFCLK0N_118
MGTCLK2_5338_P H6
MGTCLK2_5338_N H5
MGTREFCLK1P_118
MGTREFCLK1N_118
XC7VX330T-2FFG1157C
U1P
Bank 116
Y2 Y1 AA4 AA3 V2 V1 W4 W3
DP8_C2M_P T2 DP8_C2M_N T1 DP8_M2C_P U4 DP8_M2C_N U3
DP9_C2M_P P2 DP9_C2M_N P1 DP9_M2C_P R4 DP9_M2C_N R3
MGTHTXP0_116 MGTHTXN0_116 MGTHRXP0_116 MGTHRXN0_116
MGTHTXP1_116 MGTHTXN1_116 MGTHRXP1_116 MGTHRXN1_116
MGTHTXP2_116 MGTHTXN2_116 MGTHRXP2_116 MGTHRXN2_116
MGTHTXP3_116 MGTHTXN3_116 MGTHRXP3_116 MGTHRXN3_116
CLK_SYNTH_DCLKOUT4_P T6
CLK_SYNTH_DCLKOUT4_N T5
MGTREFCLK0P_116
MGTREFCLK0N_116
V6 V5
MGTREFCLK1P_116
MGTREFCLK1N_116
XC7VX330T-2FFG1157C
U1Q
Bank 117
DP0_C2M_P M2 DP0_C2M_N M1 DP0_M2C_P N4 DP0_M2C_N N3
DP1_C2M_P K2 DP1_C2M_N K1 DP1_M2C_P L4 DP1_M2C_N L3
DP2_C2M_P H2 DP2_C2M_N H1 DP2_M2C_P K6 DP2_M2C_N K5
DP3_C2M_P F2 DP3_C2M_N F1 DP3_M2C_P J4 DP3_M2C_N J3
MGTHTXP0_117 MGTHTXN0_117 MGTHRXP0_117 MGTHRXN0_117
MGTHTXP1_117 MGTHTXN1_117 MGTHRXP1_117 MGTHRXN1_117
MGTHTXP2_117 MGTHTXN2_117 MGTHRXP2_117 MGTHRXN2_117
MGTHTXP3_117 MGTHTXN3_117 MGTHRXP3_117 MGTHRXN3_117
GBTCLK0_M2C_P M6
GBTCLK0_M2C_N M5
MGTREFCLK0P_117
MGTREFCLK0N_117
GBTCLK1_M2C_P P6
GBTCLK1_M2C_N P5
MGTREFCLK1P_117
MGTREFCLK1N_117
XC7VX330T-2FFG1157C
PCIE
trenz electronic
Title: TEC0330 - FPGA MGT BANKS
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
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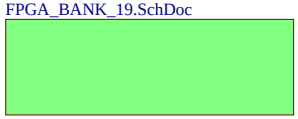
Filename: FPGA_MGT_BANKS.SchDoc

U_FPGA_BANK_19
FPGA_BANK_19.SchDoc



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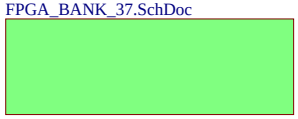

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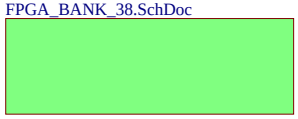

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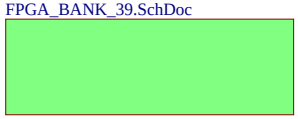
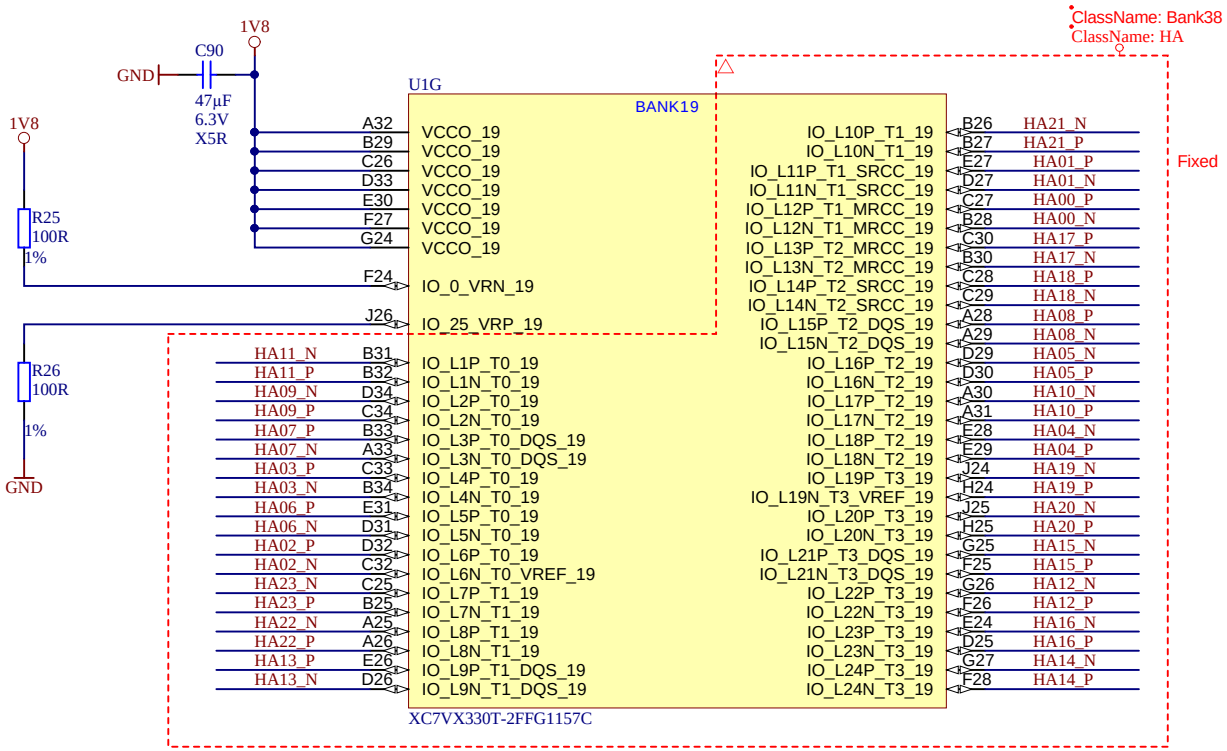


trenz electronic	Title: TEC0330 - FMC_BANKS		
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page 26 of 38
Filename: FMC_Banks.SchDoc			



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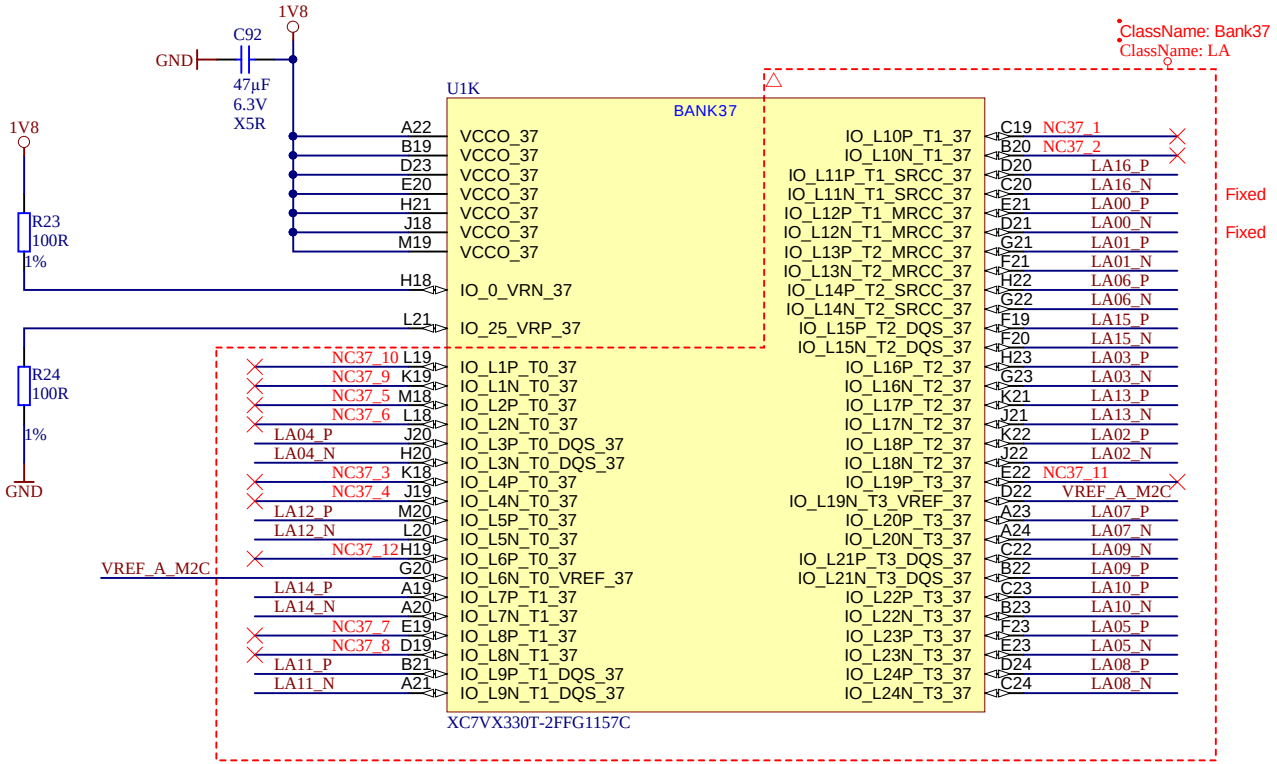
	A4	Number: TEC0330 Default	Rev. 03
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page27 of 38
	Filename: FPGA_BANK_19.SchDoc		



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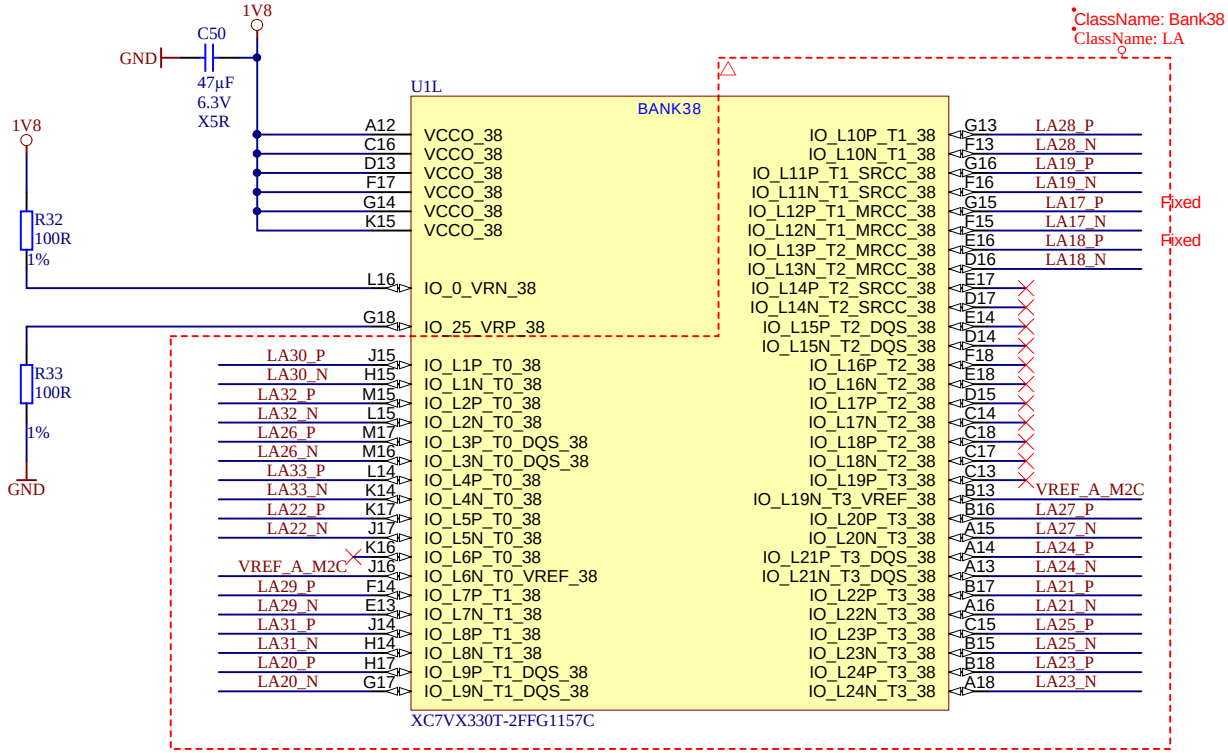
	A4	Number: TEC0330 Default	Rev. 03
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page28 of 38
	Filename: FPGA_BANK_37.SchDoc		



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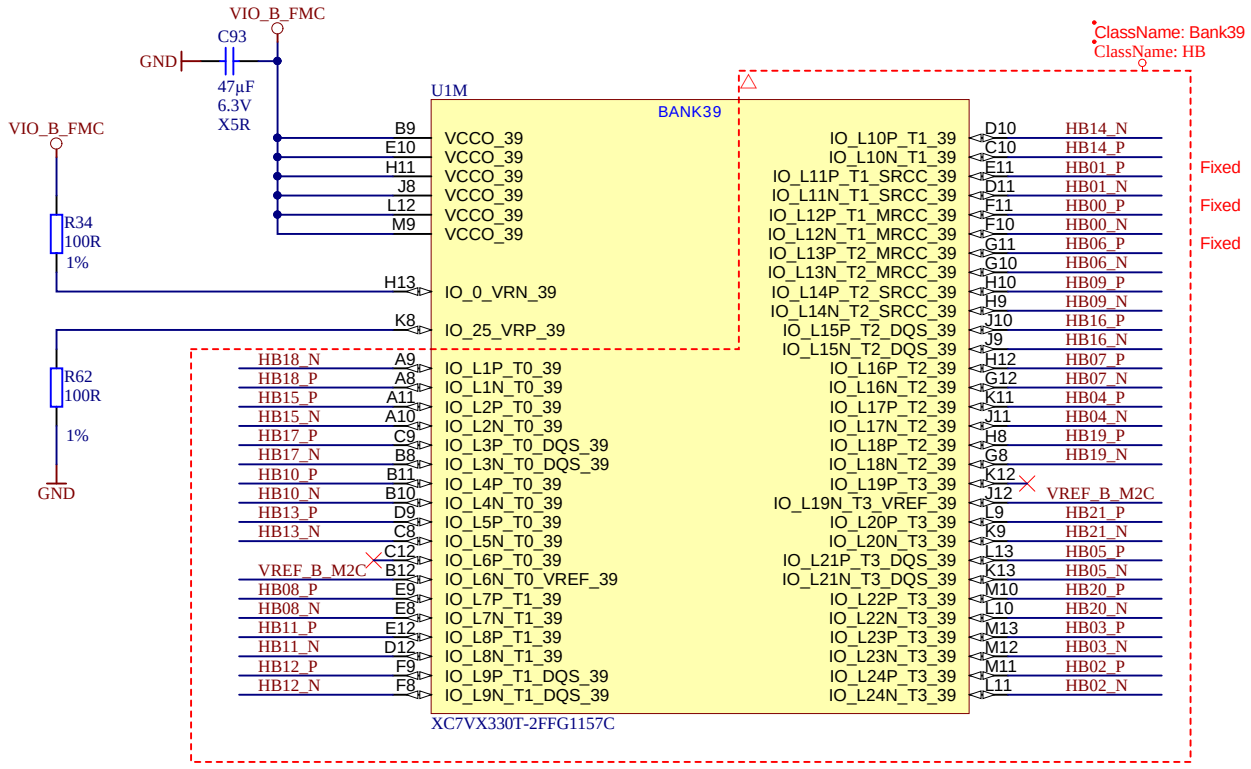
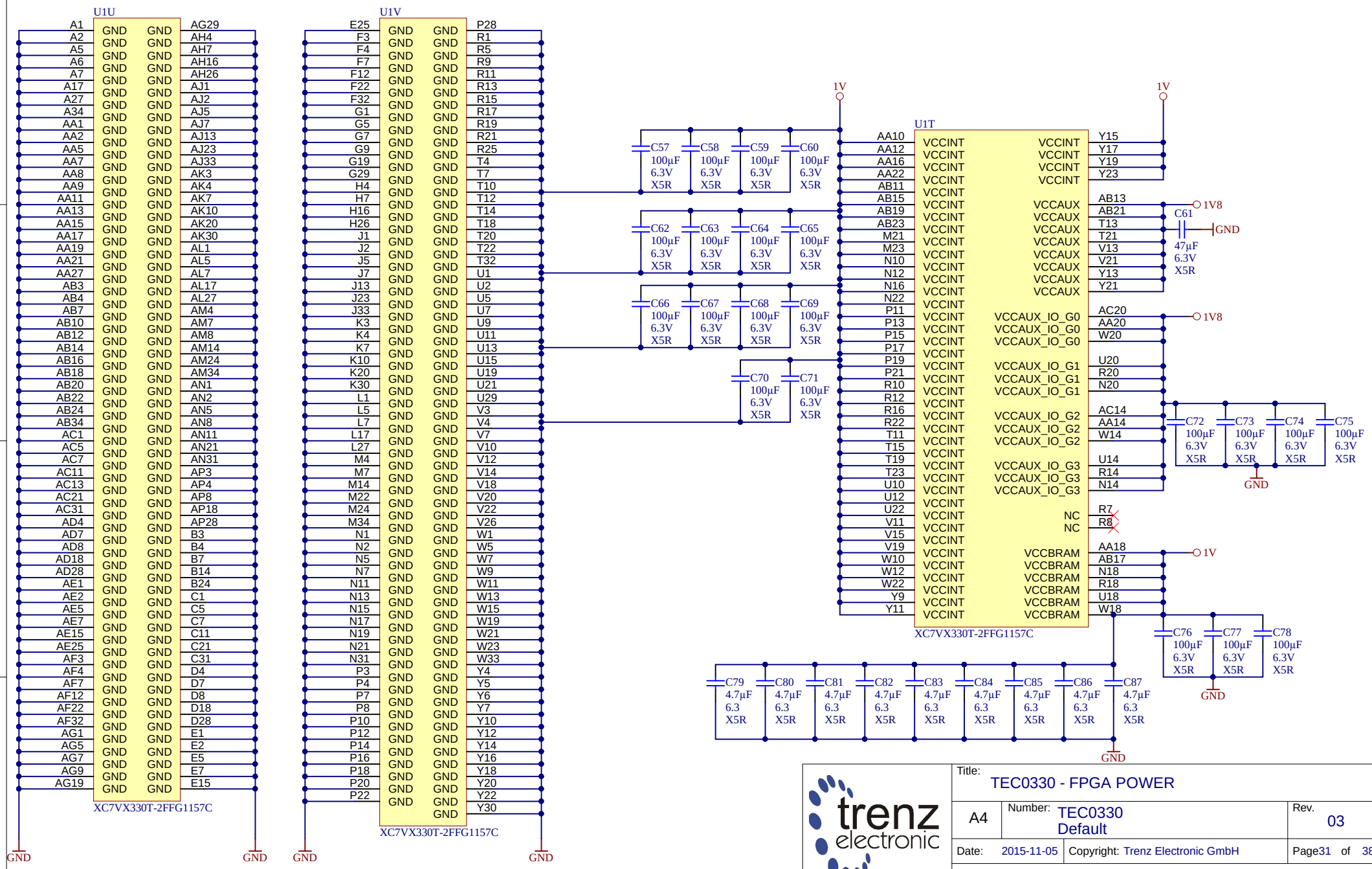
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page29 of 38
Filename: FPGA_BANK_38.SchDoc			



trenz electronic	Title: TEC0330 - FPGA B39		
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page30 of 38
Filename: FPGA_BANK_39.SchDoc			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XC7VX330T-2FFG1157C
U1V
XC7VX330T-2FFG1157C
U1T
XC7VX330T-2FFG1157C
1V
1V8
GND
C57 C58 C59 C60 100µF 6.3V X5R
C62 C63 C64 C65 100µF 6.3V X5R
C66 C67 C68 C69 100µF 6.3V X5R
C70 C71 100µF 6.3V X5R
C61 47µF 6.3V X5R
C72 C73 C74 C75 100µF 6.3V X5R
C76 C77 C78 100µF 6.3V X5R
C79 C80 C81 C82 C83 C84 C85 C86 C87 4.7µF 6.3 X5R
trenz electronic
Title: TEC0330 - FPGA POWER
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
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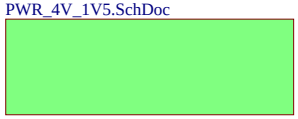
Filename: FPGA_POWER.SchDoc

U_PWR_4V_1V5
PWR_4V_1V5.SchDoc



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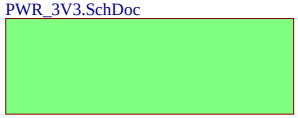

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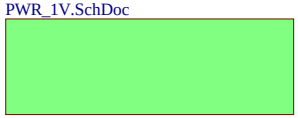
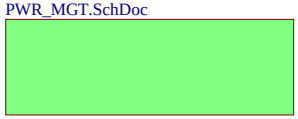


U_PWR_MGT
PWR_MGT.SchDoc



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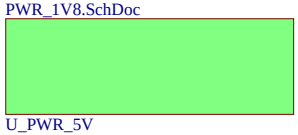

U_PWR_5V
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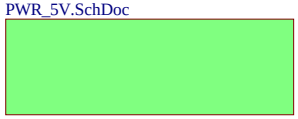

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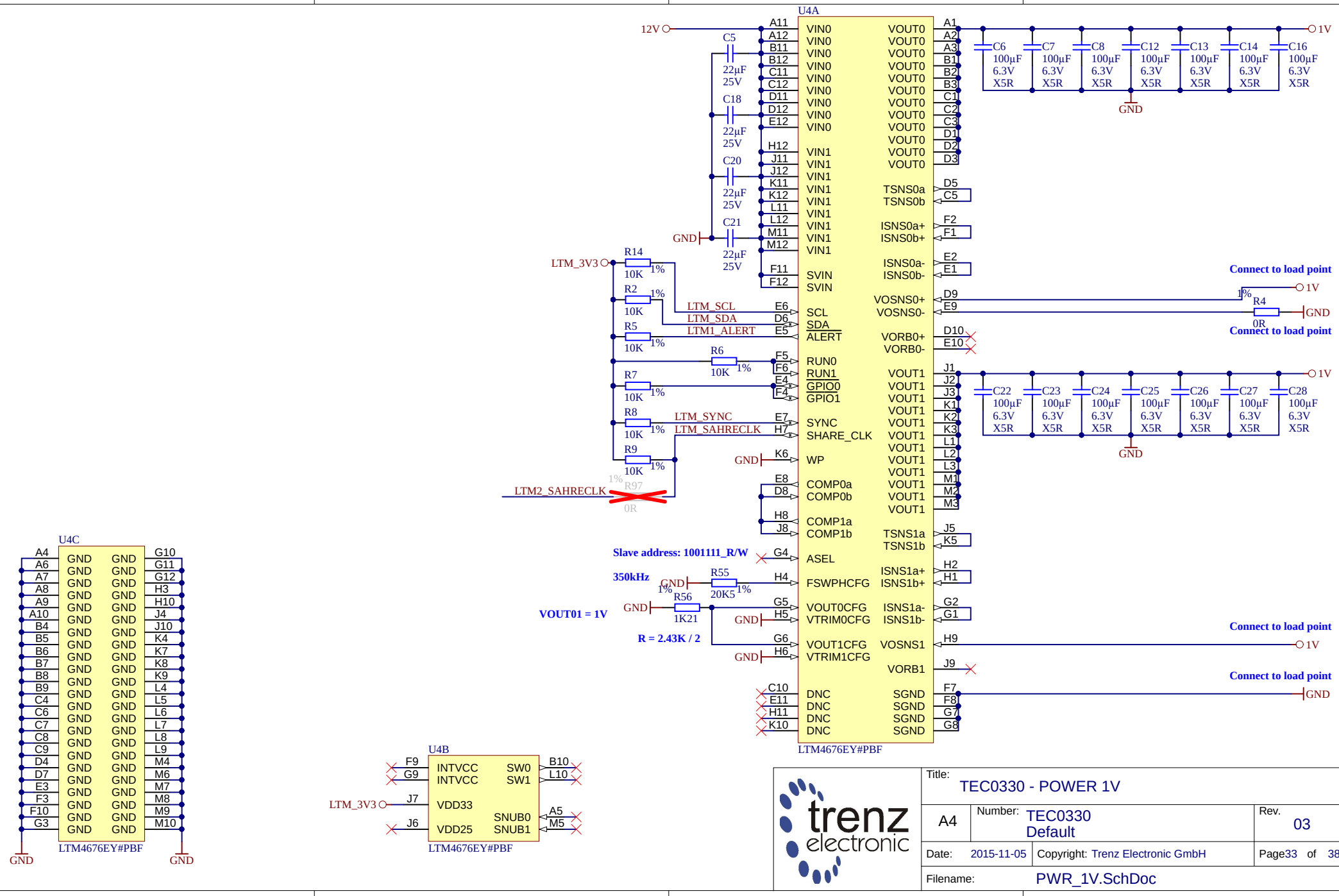
U4A
LTM4676EY#PBF
12V
1V
GND
LTM_3V3
LTM_SCL
LTM_SDA
LTM1_ALERT
LTM_SYNC
LTM_SAHRECLK
LTM2_SAHRECLK
Slave address: 1001111_R/W
350kHz
VOUT01 = 1V
R = 2.43K / 2
Connect to load point
U4C
U4B
Title: TEC0330 - POWER 1V
A4
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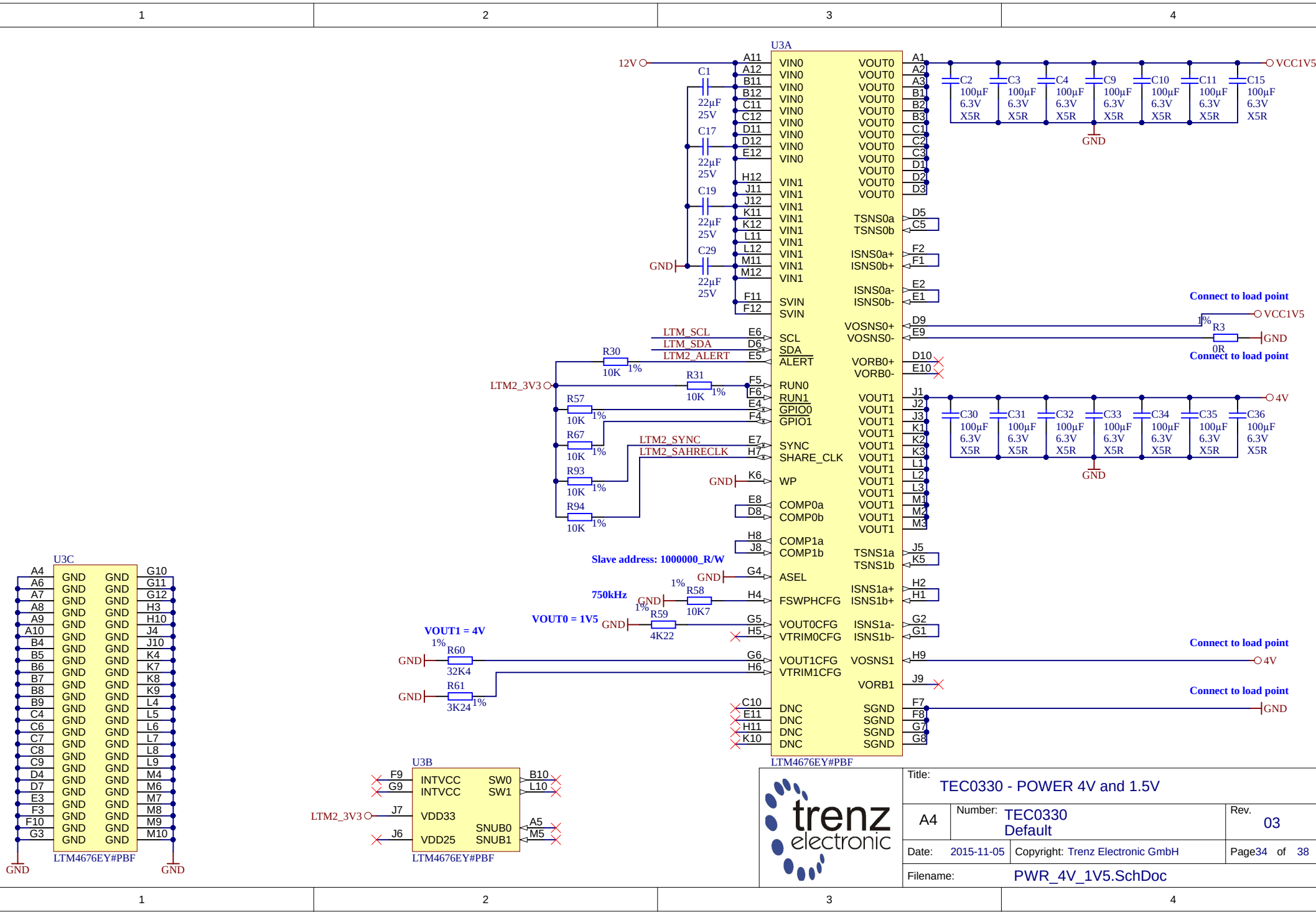
Filename: PWR_1V.SchDoc


U3A
LTM4676EY#PBF
12V
VCC1V5
4V
GND
LTM2_3V3
LTM_SCL
LTM_SDA
LTM2_ALERT
LTM2_SYNC
LTM2_SAHRECLK
Slave address: 1000000_R/W
750kHz
VOUT0 = 1V5
VOUT1 = 4V
Connect to load point
U3C
U3B
LTM4676EY#PBF
LTM4676EY#PBF
trenz electronic
Title: TEC0330 - POWER 4V and 1.5V
A4
Number: TEC0330 Default
Rev. 03
Date: 2015-11-05
Copyright: Trenz Electronic GmbH
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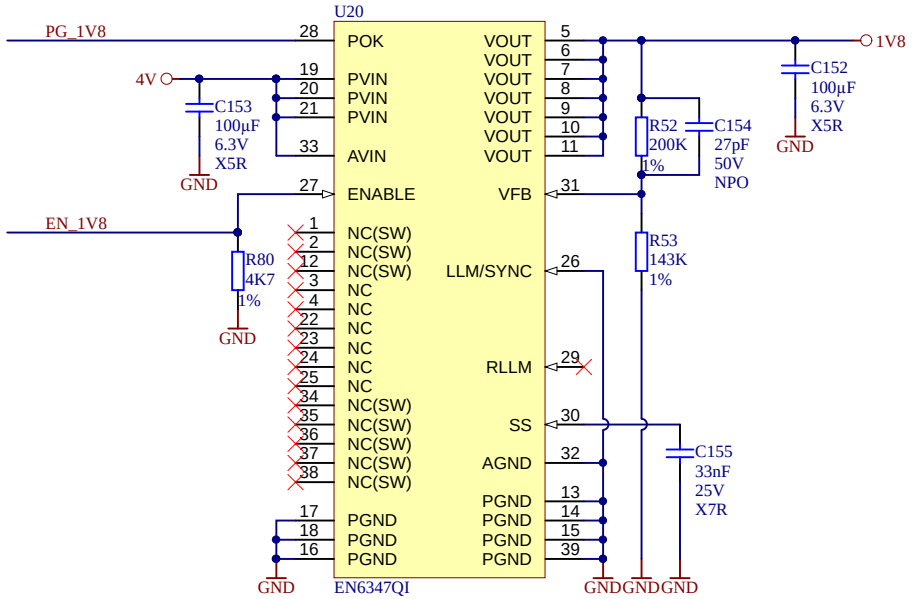
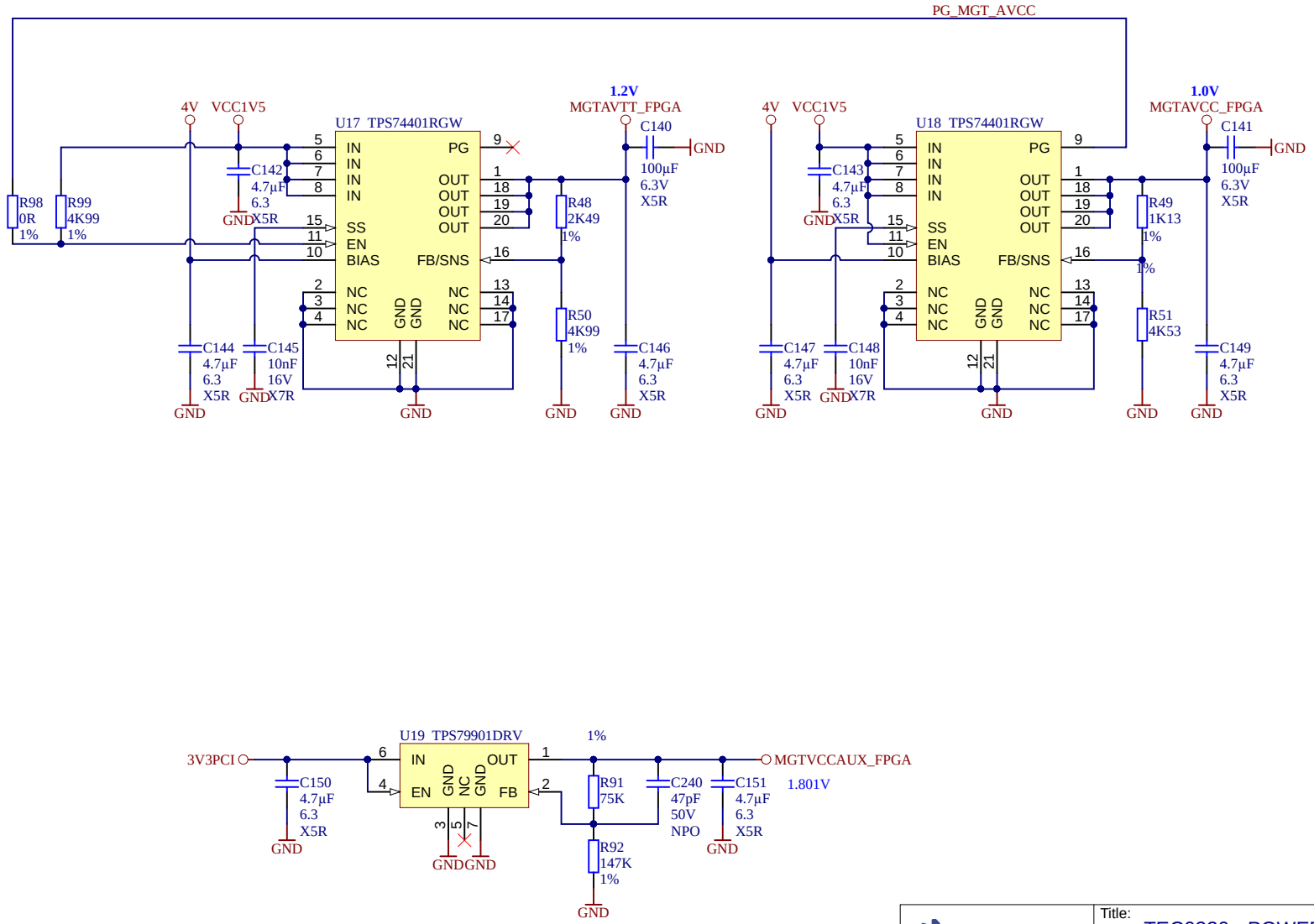
Filename: PWR_4V_1V5.SchDoc



trenz electronic	Title: TEC0330 - POWER 1V8		
	A4	Number: TEC0330 Default	Rev. 03
	Date: 2015-11-05	Copyright: Trenz Electronic GmbH	Page35 of 38
	Filename: PWR_1V8.SchDoc		



Title: TEC0330 - POWER MGT			
A4	Number: TEC0330 Default		Rev. 03
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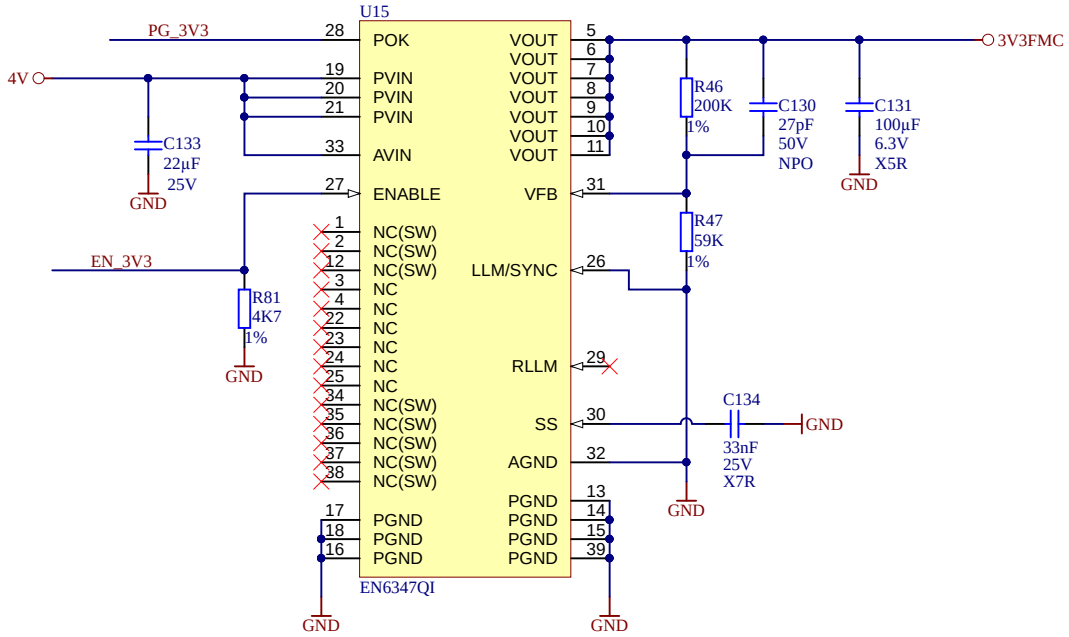
Filename: PWR_MGT.SchDoc			



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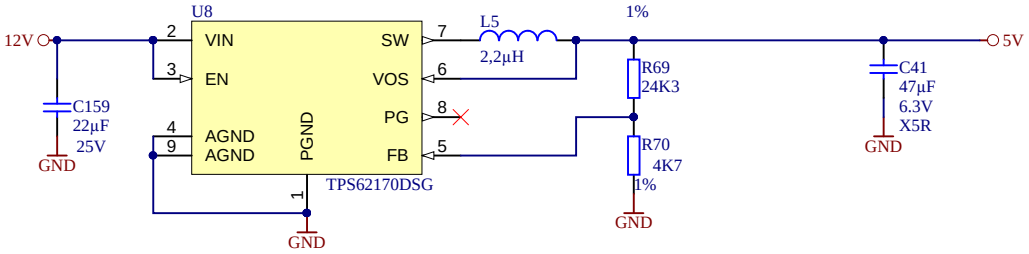
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page37 of 38
Filename: PWR_3V3.SchDoc			



Title: TEC0330 - POWER 5V			
A4	Number: TEC0330 Default		Rev. 03
Date: 2015-11-05	Copyright: Trenz Electronic GmbH		Page 38 of 38
Filename: PWR_5V.SchDoc			