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U\_FPGA  
FPGA.SchDoc



U\_SODIMM  
SODIMM.SchDoc



U\_CLOCK  
CLOCK.SchDoc



U\_POWER  
POWER.SchDoc



U\_CONN  
CONN.SchDoc



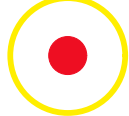
U\_CPLD  
CPLD.SchDoc



PM1

PM2

PM3



FIDU-DOT - small

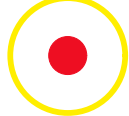
FIDU-DOT - small

FIDU-DOT - small

PM4

PM5

PM6



FIDU-DOT - small

FIDU-DOT - small

FIDU-DOT - small

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT



Title: <b>TEC0330 - Overview</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page1 of 38
Filename: <b>TEC0330.SchDoc</b>		

1

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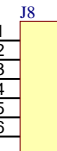
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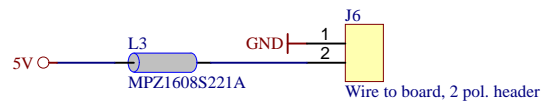
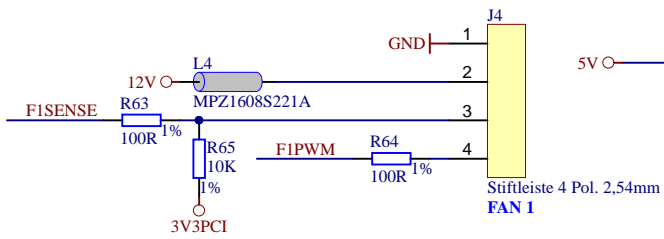
U\_FMC  
FMC.SchDoc

U\_PCIE\_CONN  
PCIE\_CONN.SchDoc

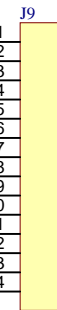
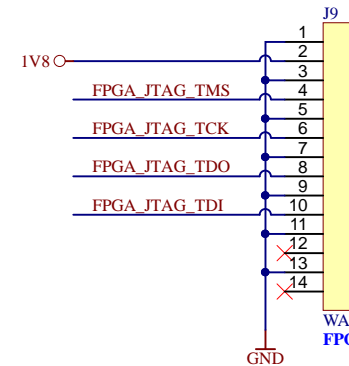
U\_MLVDS\_CONN  
MLVDS\_CONN.SchDoc



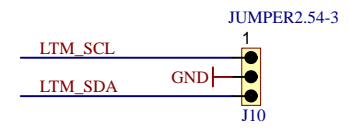
Placeholder 1 row 6 pin header  
CPLD JTAG CONNECTOR



- FAN 2: Wire to board, 2 pol. header
- JX1: Wire to board, 2 pol. housing
- JCT1: Crimp Terminal 4809, 22-30 AWG
- JCT2: Crimp Terminal 4809, 22-30 AWG

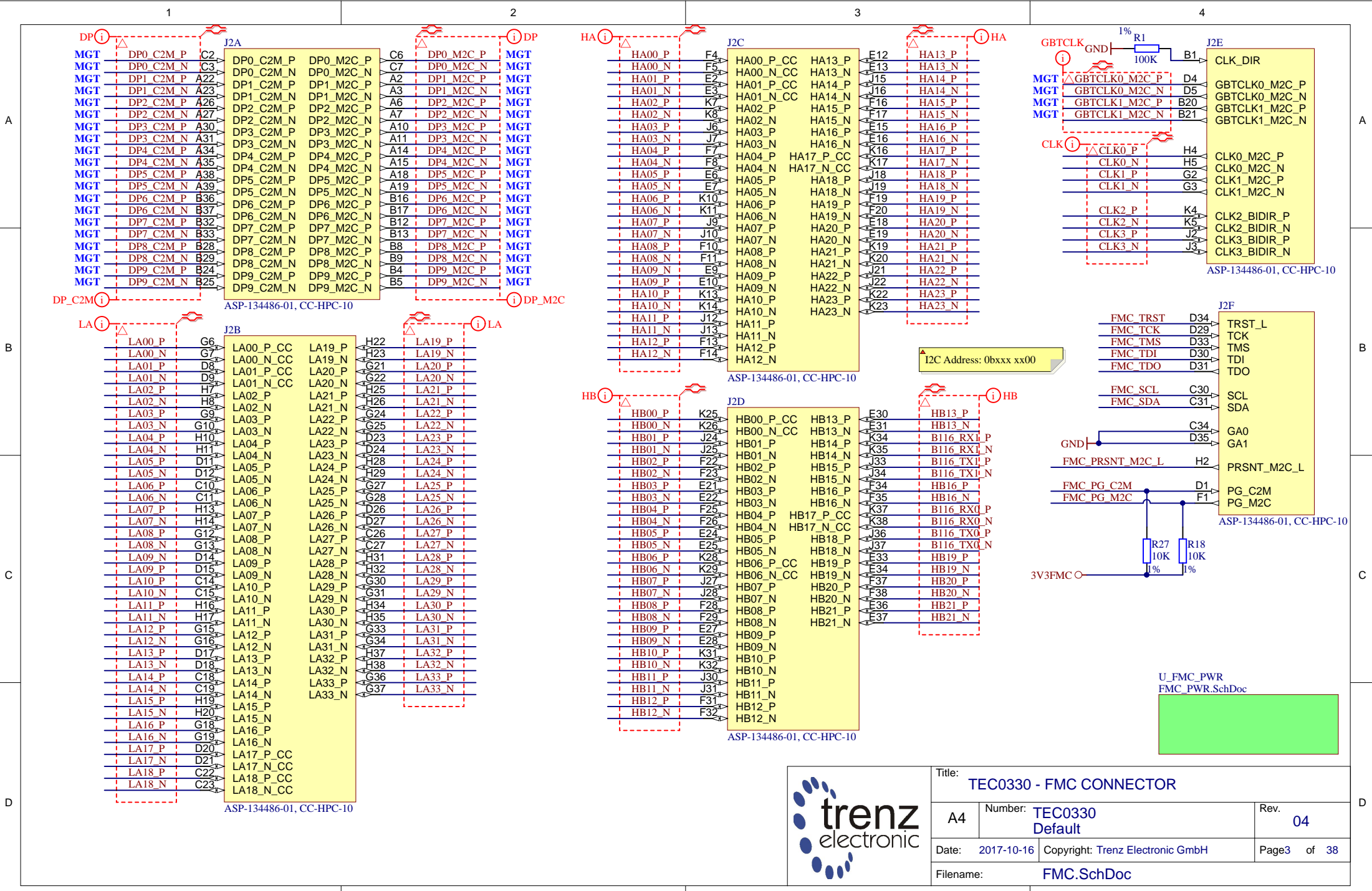


WANNE2mm2R-14  
FPGA JTAG CONNECTOR



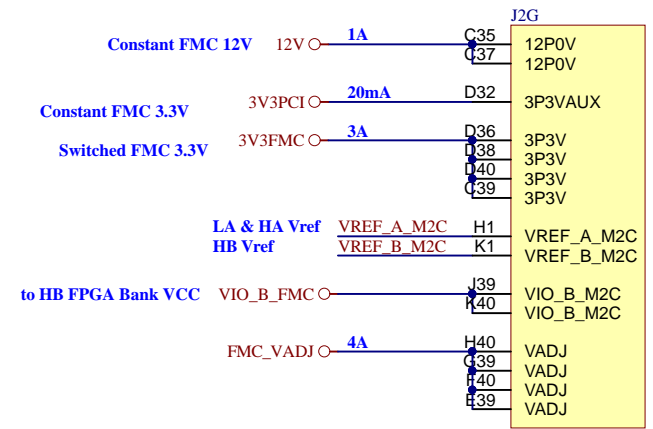
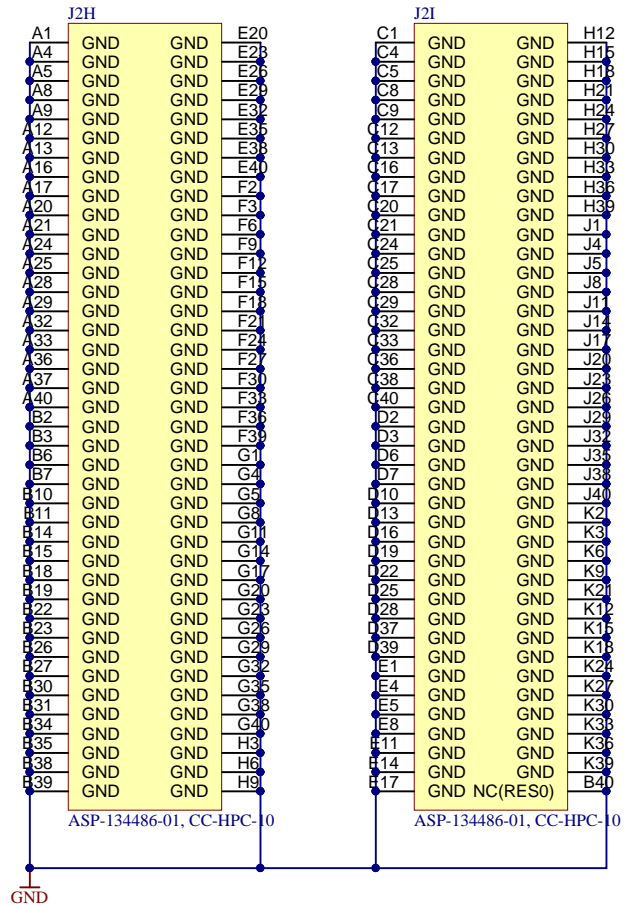
JUMPER2.54-3  
LTM I2C CONNECTOR

	Title: TEC0330 - CONNECTORS	
	A4	Number: TEC0330 Default
	Date: 2017-10-16	Copyright: Trenz Electronic GmbH
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Filename: CONN.SchDoc		Rev. 04

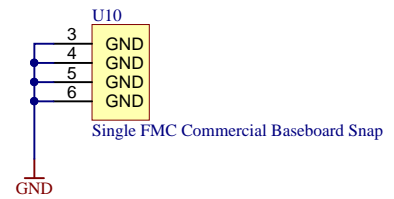
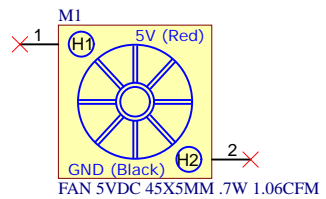
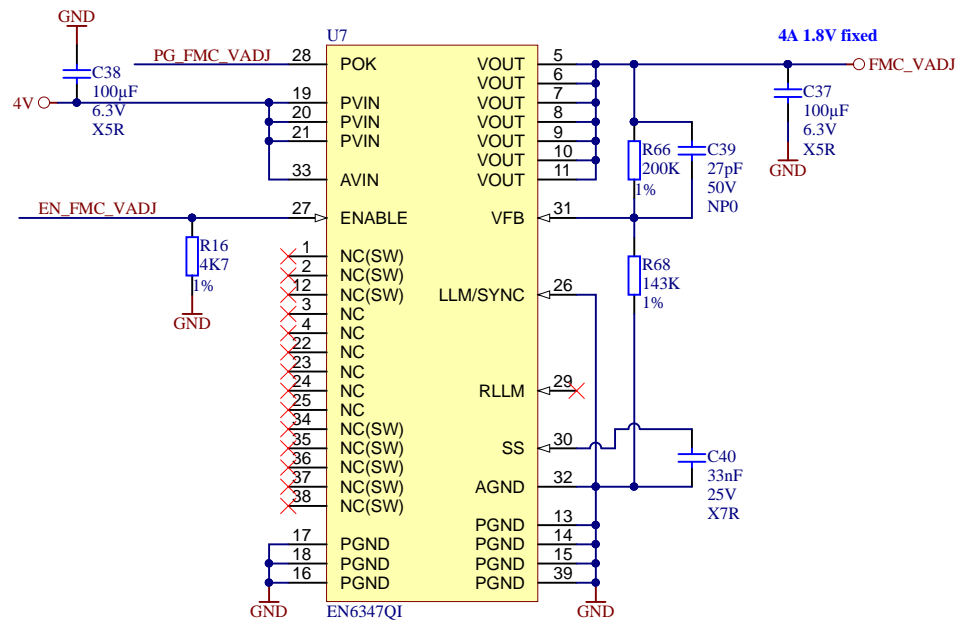


Title: <b>TEC0330 - FMC CONNECTOR</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>FMC.SchDoc</b>		

U\_FMC\_PWR  
FMC\_PWR.SchDoc



ASP-134486-01, CC-HPC-10



Title: <b>TEC0330 - FMC CONNECTOR POWER</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>FMC_PWR.SchDoc</b>		

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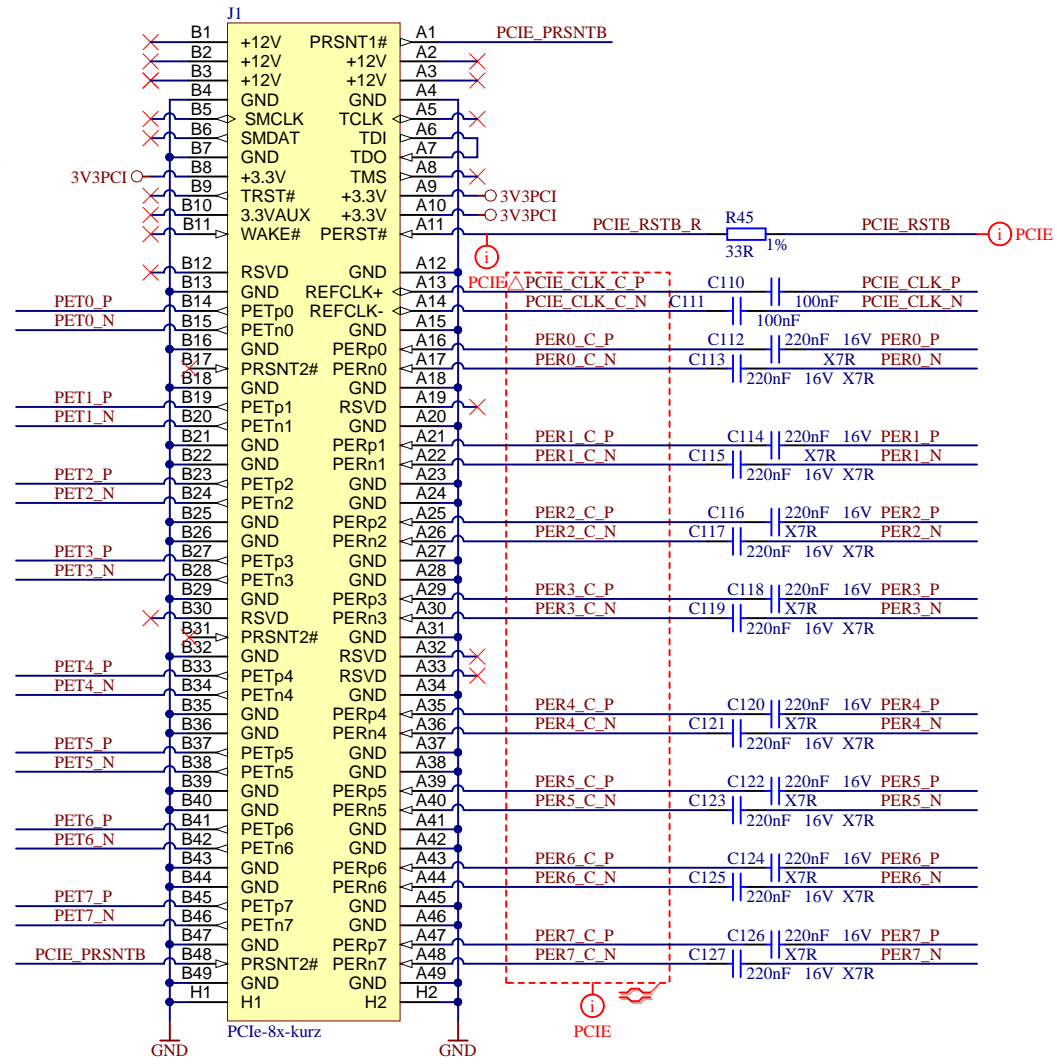
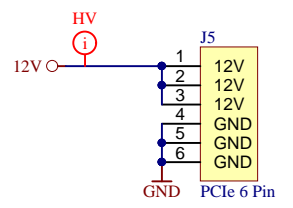
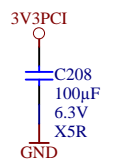
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Title: TEC0330 - PCIE CONNECTOR		
A4	Number: TEC0330 Default	Rev. 04
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Filename: PCIE_CONN.SchDoc		

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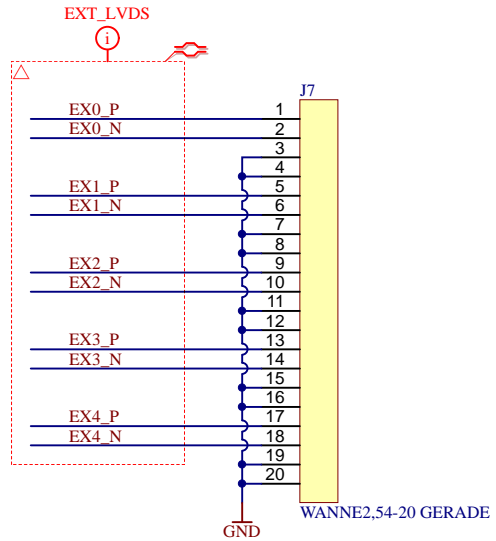
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Title: <b>TEC0330 - MLVDS CONNECTOR</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>38</b>
Filename: <b>MLVDS_CONN.SchDoc</b>		

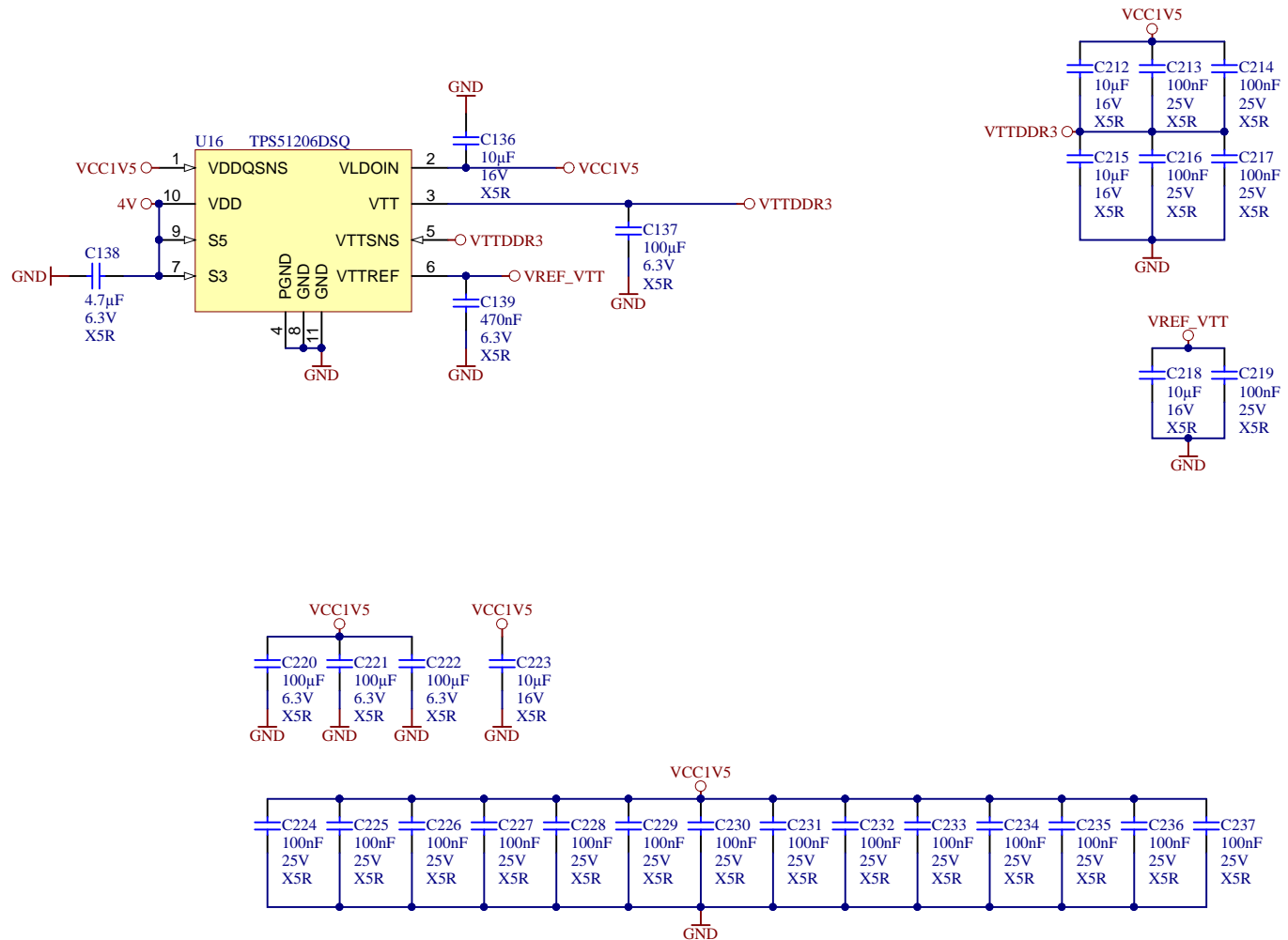
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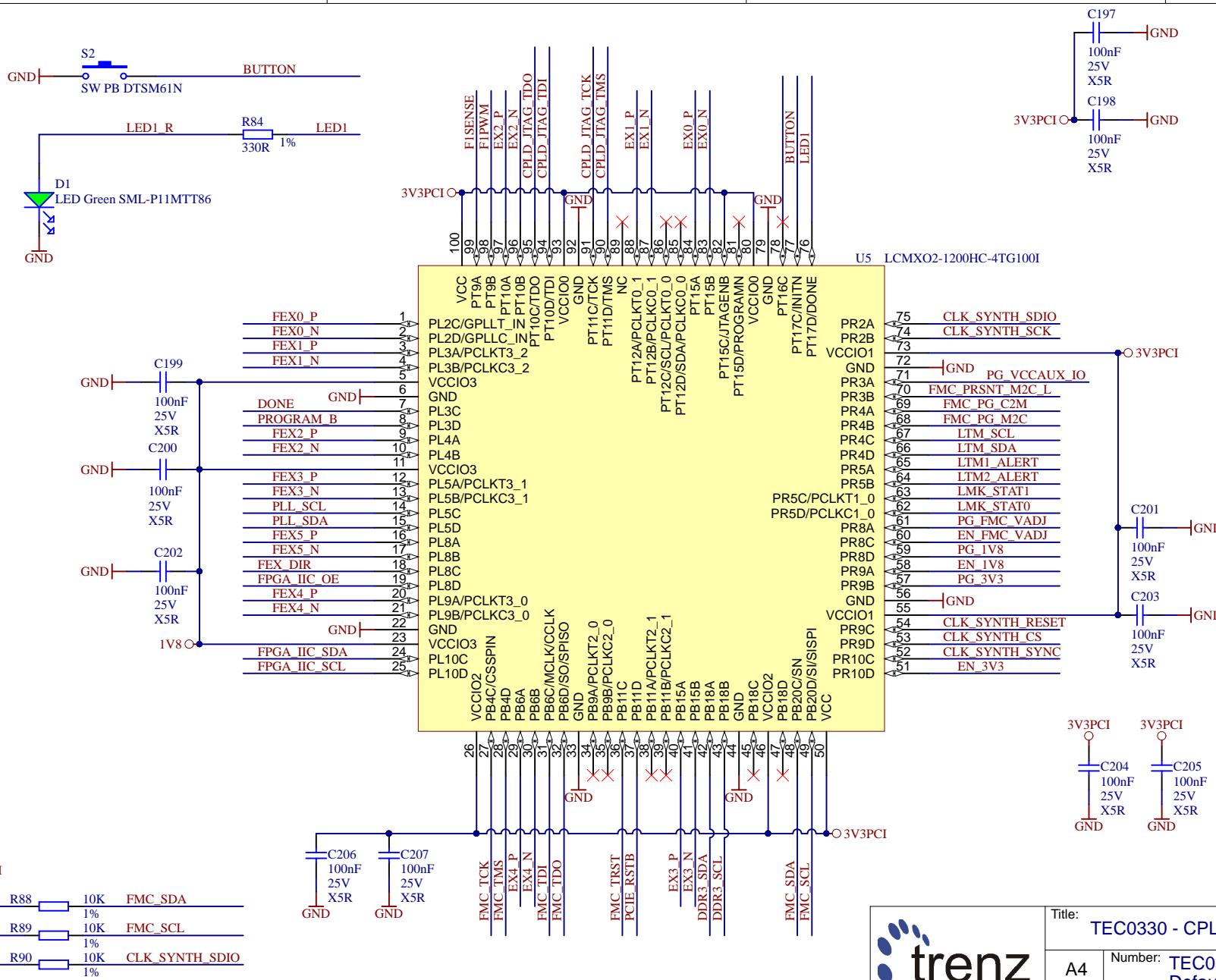
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Title: <b>TEC0330 - SODIMM MEMORY</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>SODIMM_PWR.SchDoc</b>		





Title: <b>TEC0330 - CPLD</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>CPLD.SchDoc</b>		

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U\_CLK\_SYNTH  
CLK\_SYNTH.SchDoc



U\_CLK-SI5338  
CLK-SI5338.SchDoc



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Title: <b>TEC0330 - CLOCKS</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>CLOCK.SchDoc</b>		

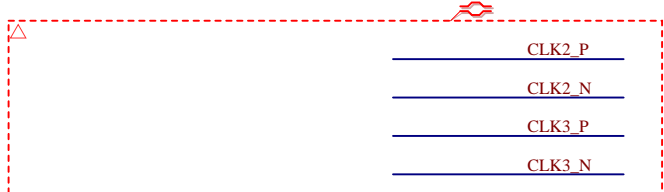
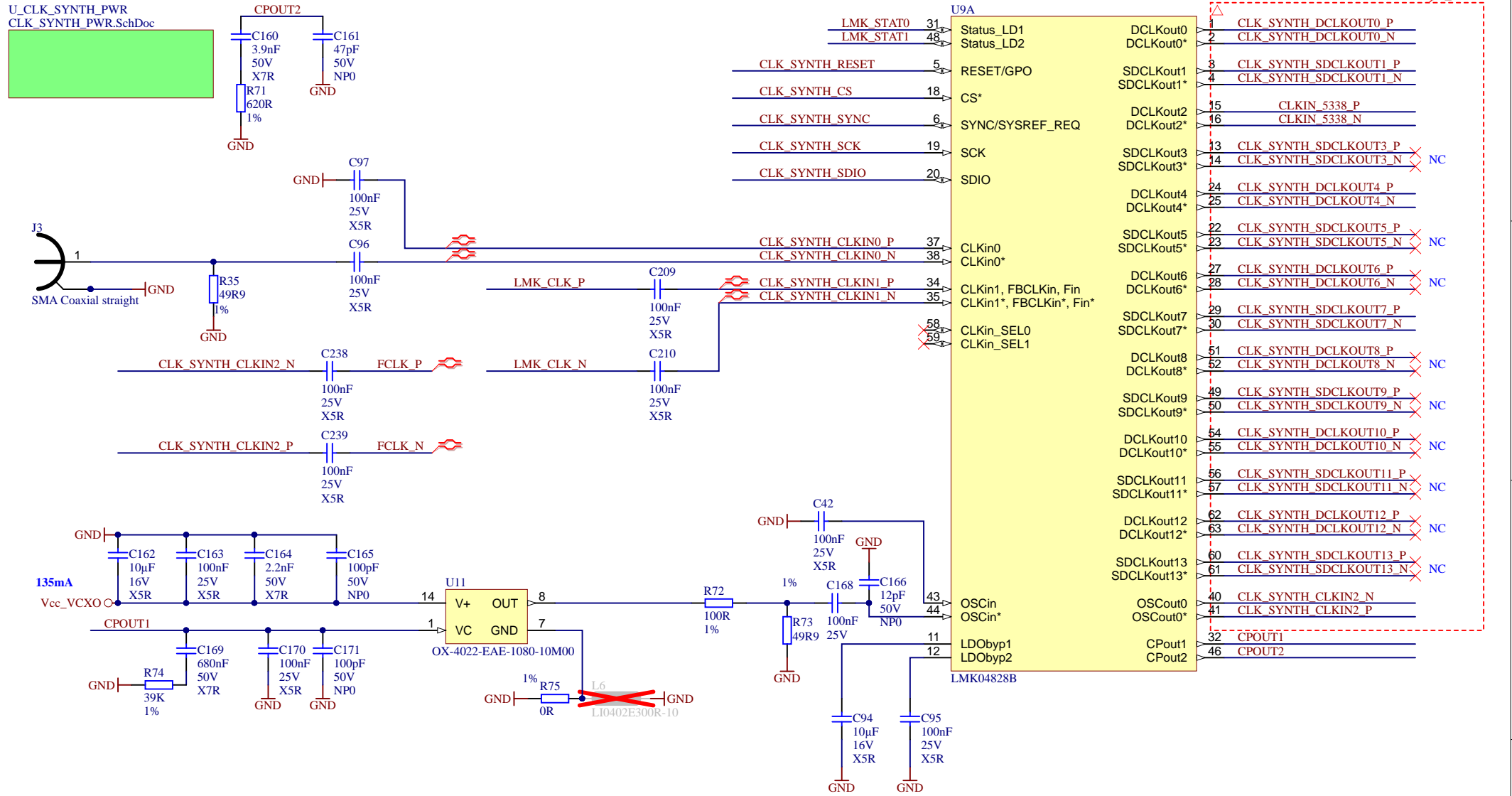
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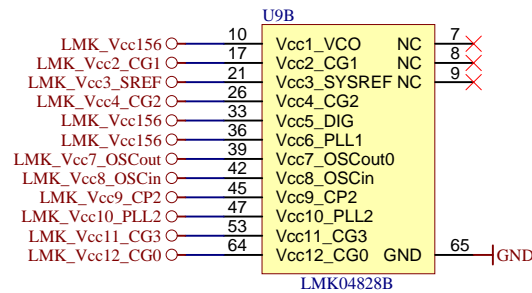
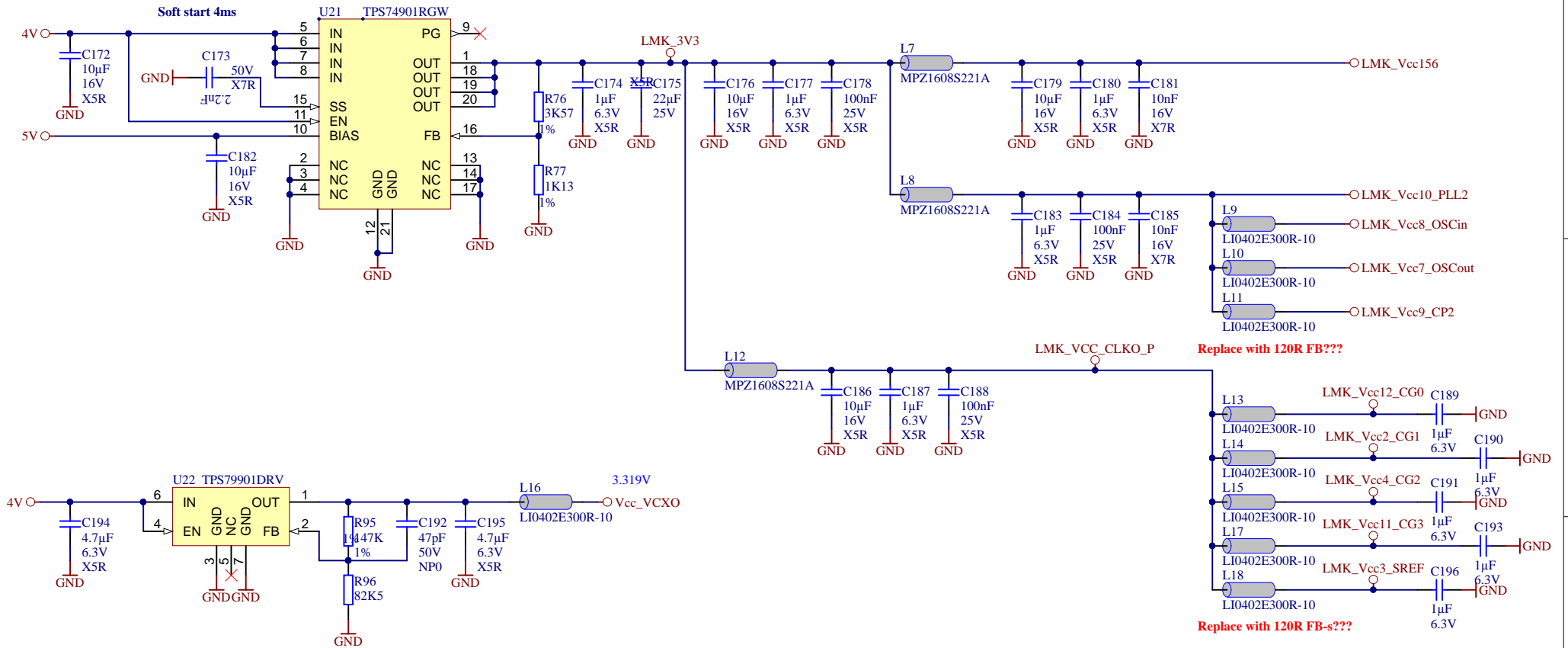
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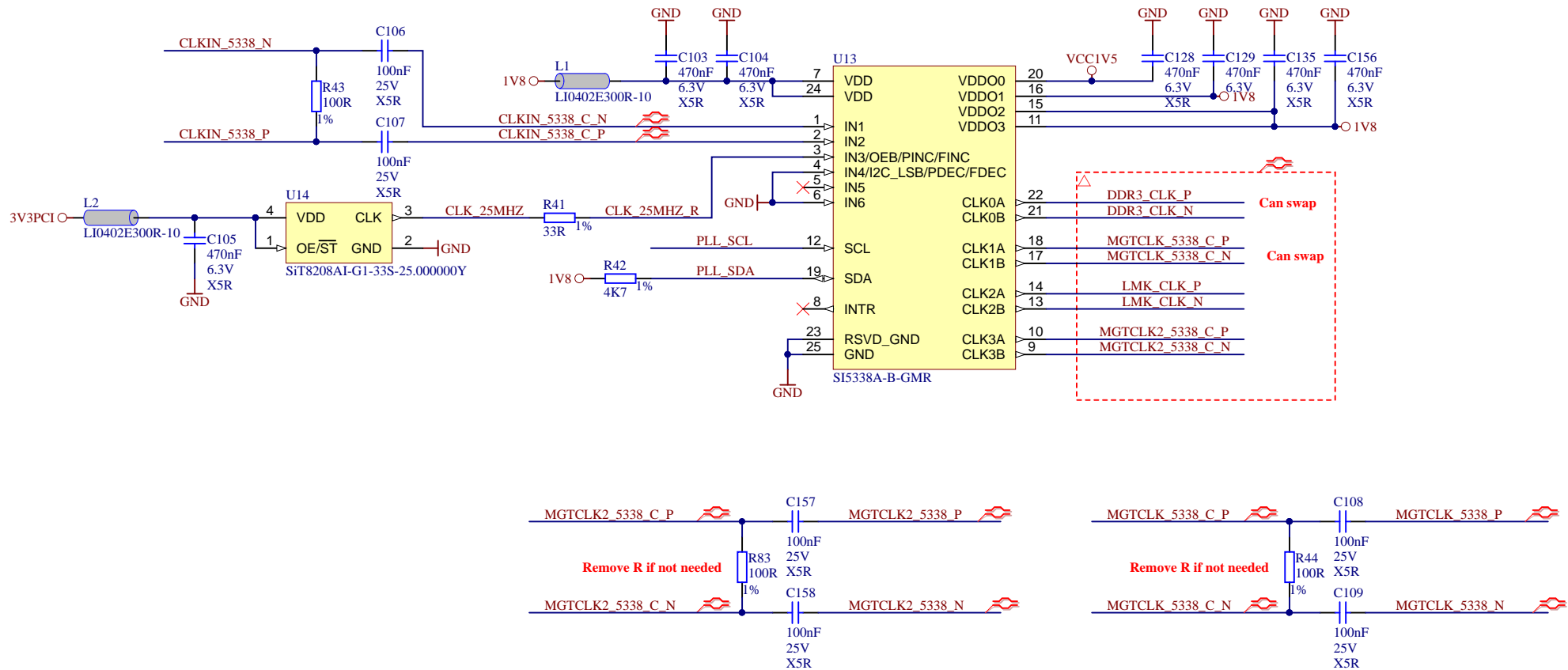
U\_CLK\_SYNTH\_PWR  
CLK\_SYNTH\_PWR.SchDoc




Title: <b>TEC0330 - CLK_SYNTH</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>CLK_SYNTH.SchDoc</b>		



Title: TEC0330 - CLK_SYNTH_PWR		
A4	Number: TEC0330 Default	Rev. 04
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Filename: CLK_SYNTH_PWR.SchDoc		



		Title: TEC0330 - CLK_SI5338	
		A4	Number: TEC0330 Default
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A

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U\_FPGA\_BANK\_14  
FPGA\_BANK\_14.SchDoc



U\_FPGA\_BANK\_15  
FPGA\_BANK\_15.SchDoc



U\_FPGA\_BANK\_16  
FPGA\_BANK\_16.SchDoc



U\_FPGA\_BANK\_17  
FPGA\_BANK\_17.SchDoc



U\_FPGA\_BANK\_18  
FPGA\_BANK\_18.SchDoc



U\_DDR\_Banks  
DDR\_Banks.SchDoc



U\_FMC\_Banks  
FMC\_Banks.SchDoc



U\_FPGA\_MGT\_BANKS  
FPGA\_MGT\_BANKS.SchDoc



U\_FPGA\_CFG  
FPGA\_CFG.SchDoc



U\_FPGA\_POWER  
FPGA\_POWER.SchDoc



B

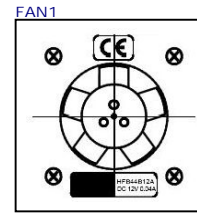
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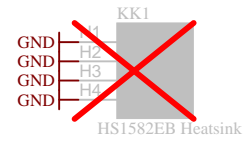
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HFB44B12A



HS1582EB Heatsink

	Title: <b>TEC0330 - FPGA</b>		
	A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
	Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>38</b>
	Filename: <b>FPGA.SchDoc</b>		

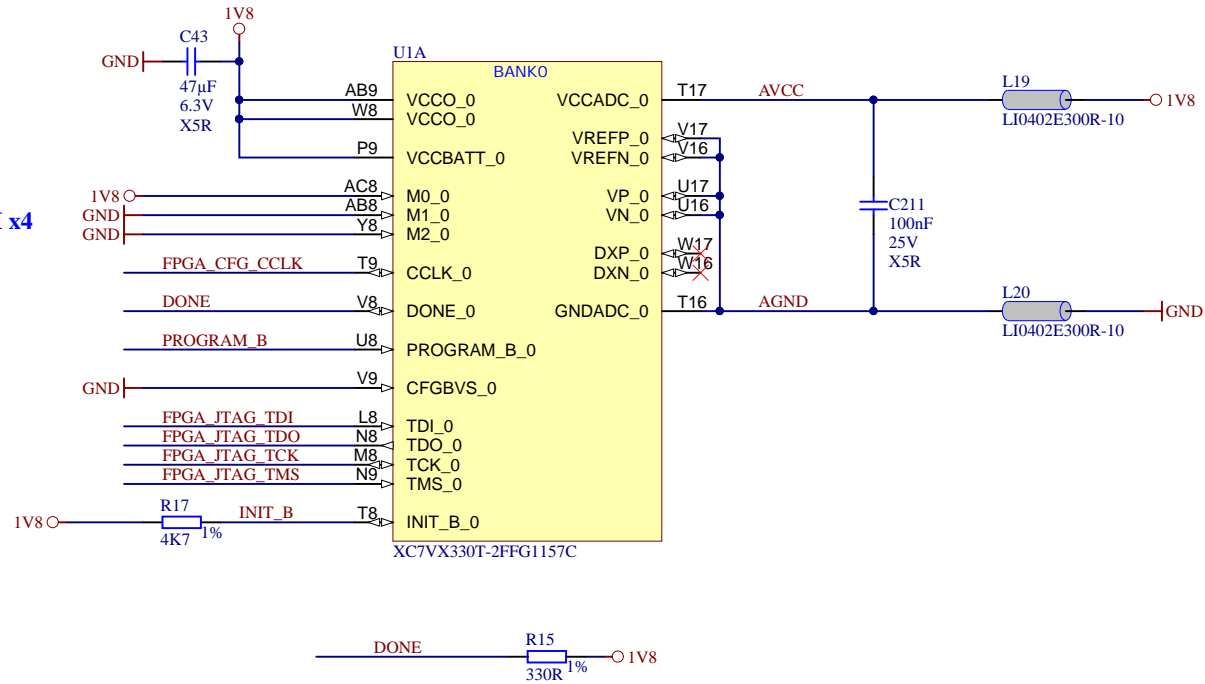
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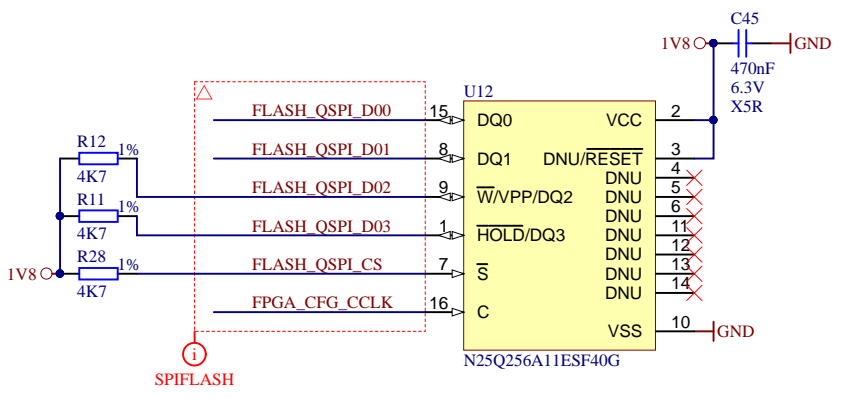
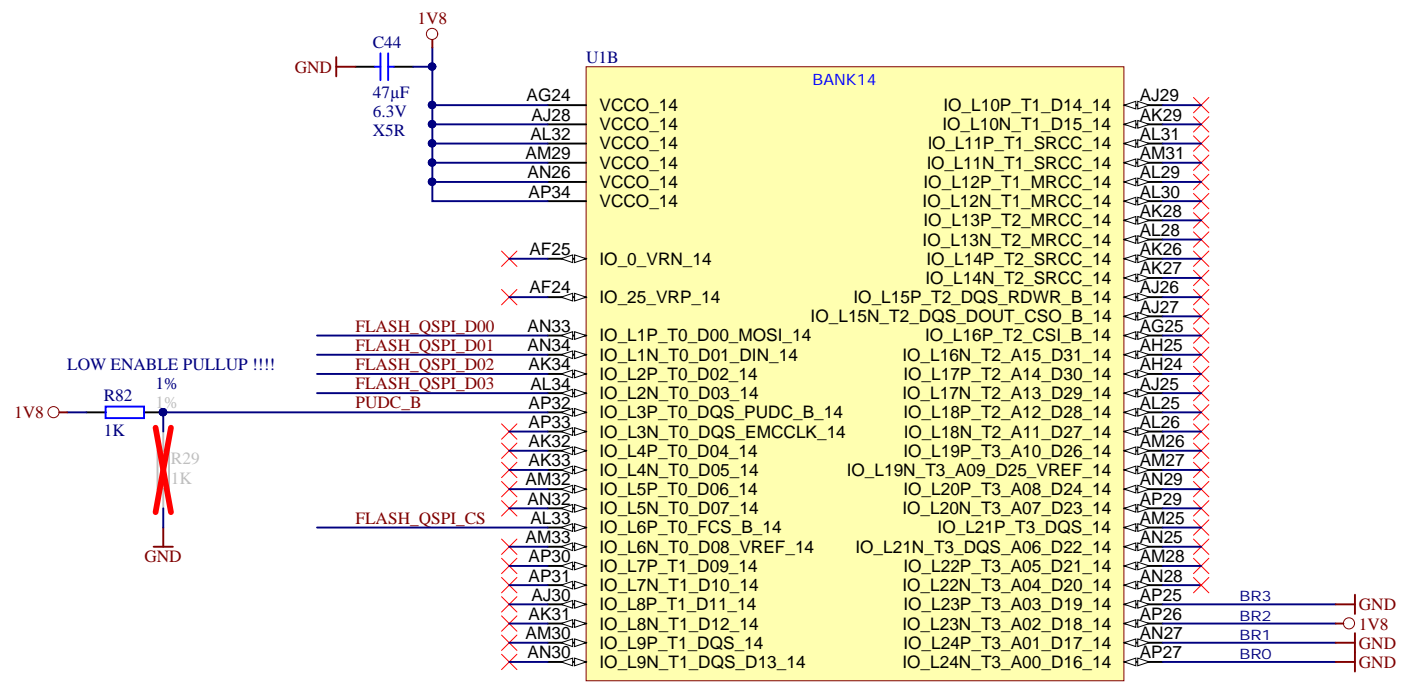
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MASTER SPI x4

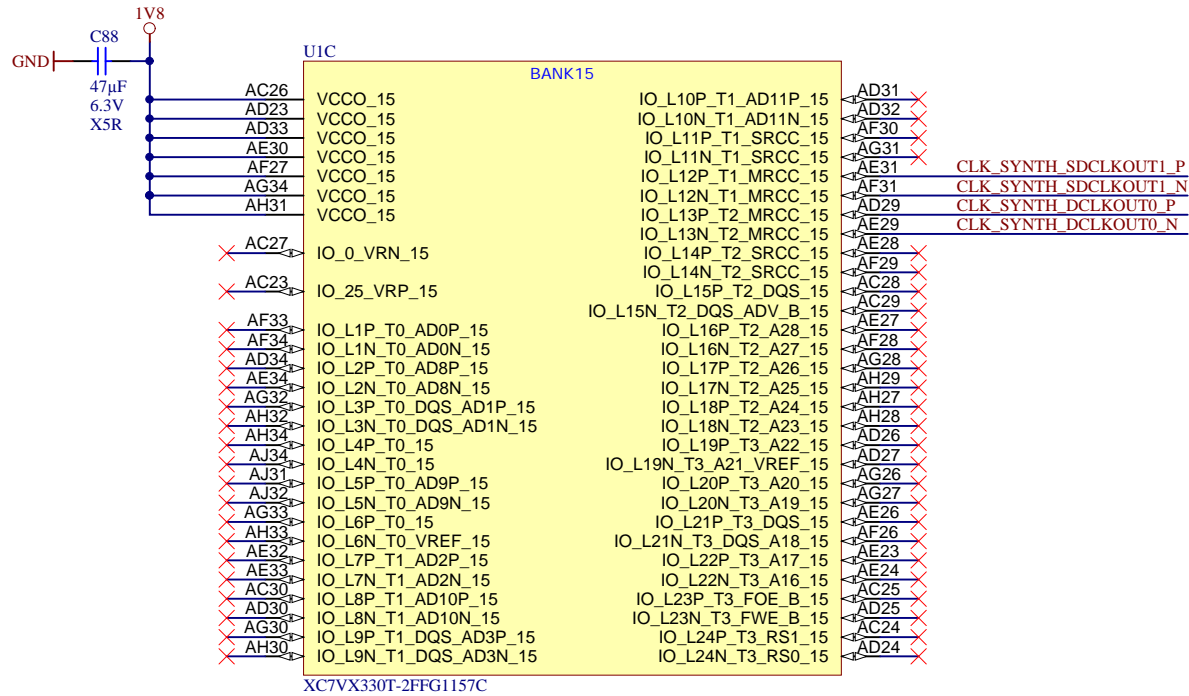


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	A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
	Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>15</b> of <b>38</b>
	Filename: <b>FPGA_CFG.SchDoc</b>		

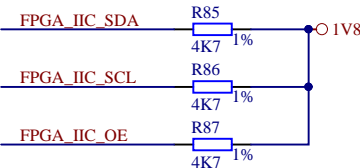
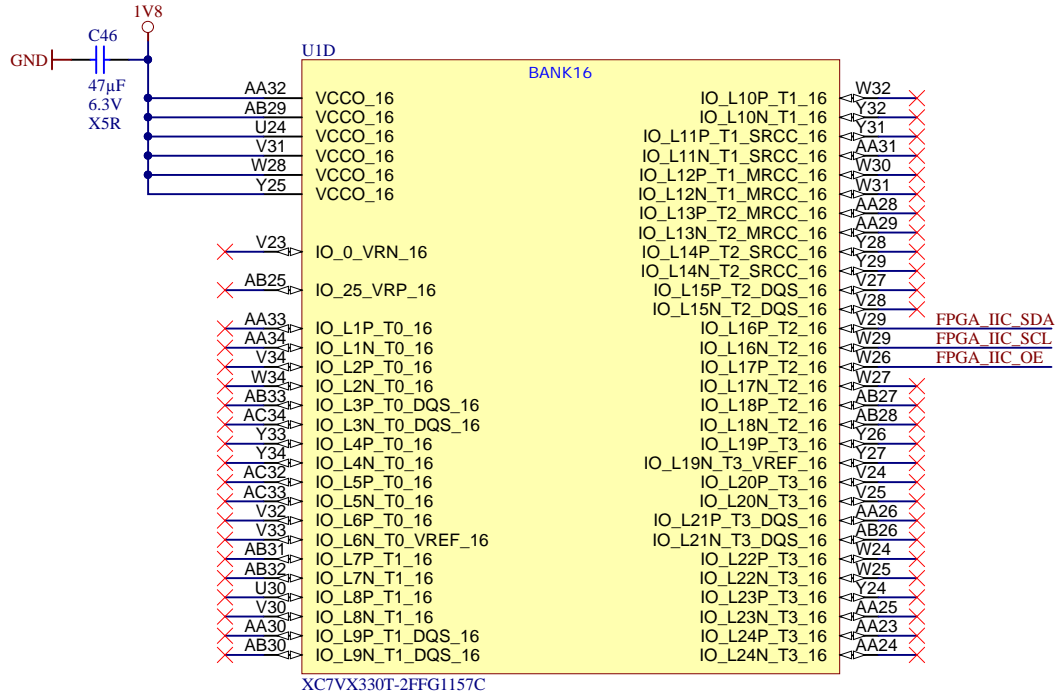



Title: <b>TEC0330 - FPGA B14</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>FPGA_BANK_14.SchDoc</b>		

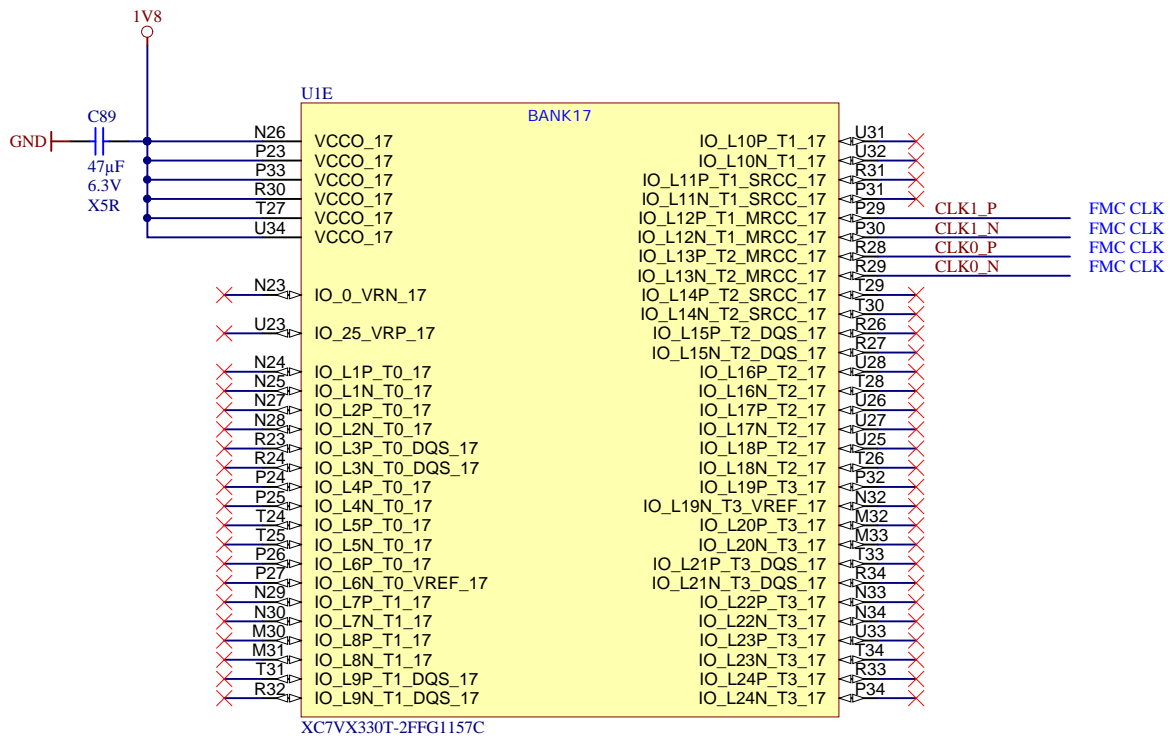




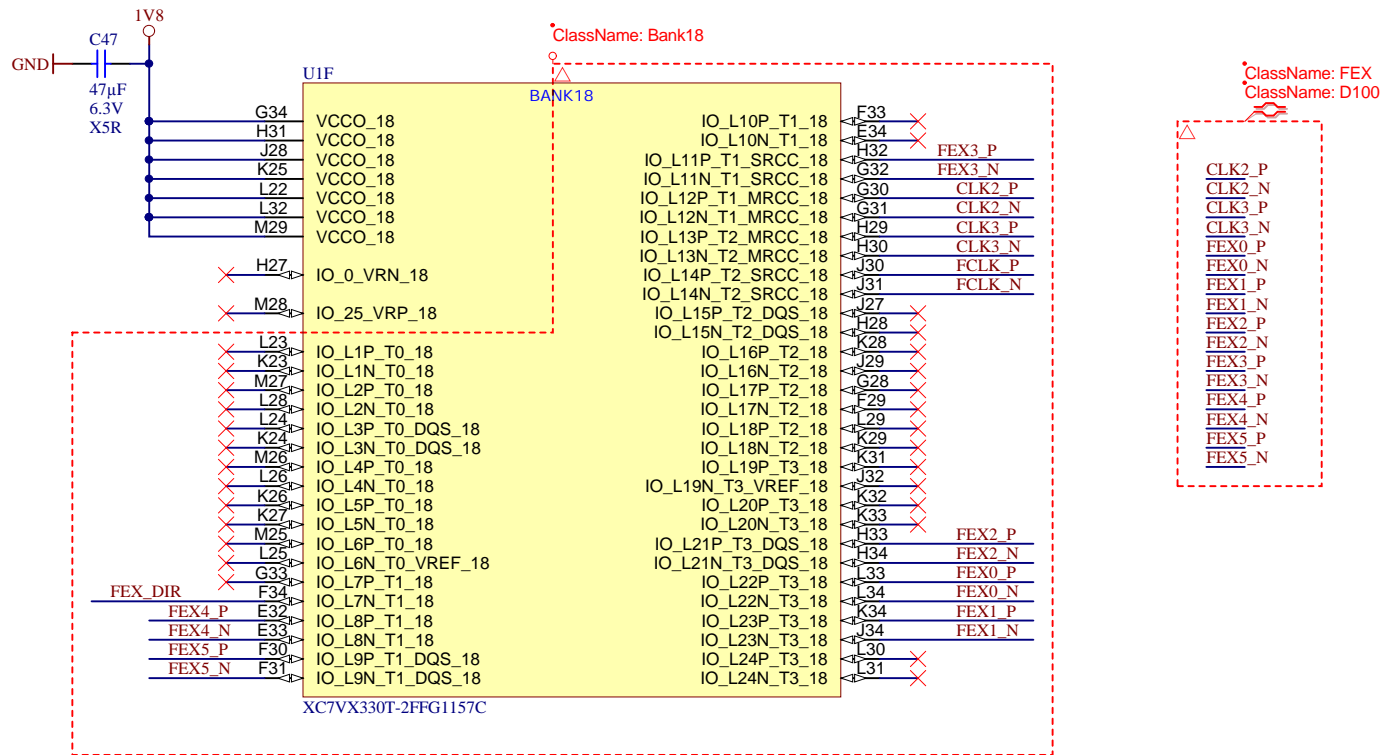
Title: <b>TEC0330 - FPGA B15</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>17</b> of <b>38</b>
Filename: <b>FPGA_BANK_15.SchDoc</b>		



		Title: <b>TEC0330 - FPGA B16</b>	
		A4	Number: <b>TEC0330 Default</b>
Date: <b>2017-10-16</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>FPGA_BANK_16.SchDoc</b>		Page <b>18</b> of <b>38</b>	



Title: <b>TEC0330 - FPGA B17</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>38</b>
Filename: <b>FPGA_BANK_17.SchDoc</b>		



Title: <b>TEC0330 - FPGA B18</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>20</b> of <b>38</b>
Filename: <b>FPGA_BANK_18.SchDoc</b>		

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U\_FPGA\_BANK\_34  
FPGA\_BANK\_34.SchDoc



U\_FPGA\_BANK\_35  
FPGA\_BANK\_35.SchDoc



U\_FPGA\_BANK\_36  
FPGA\_BANK\_36.SchDoc



A

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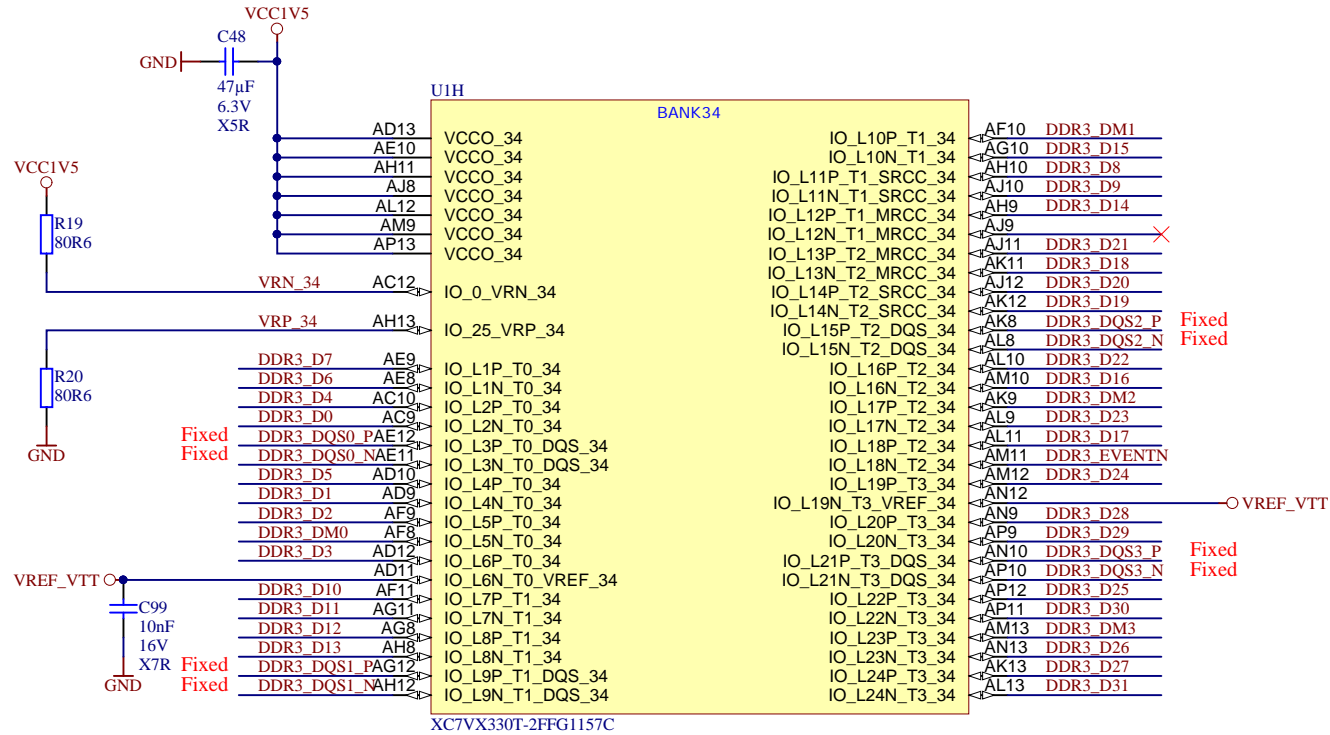
		Title: <b>TEC0330 - FPGA_DDR_BANKS</b>	
		A4	Number: <b>TEC0330 Default</b>
Date: <b>2017-10-16</b>		Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>DDR_Banks.SchDoc</b>		Page <b>21</b> of <b>38</b>	

1

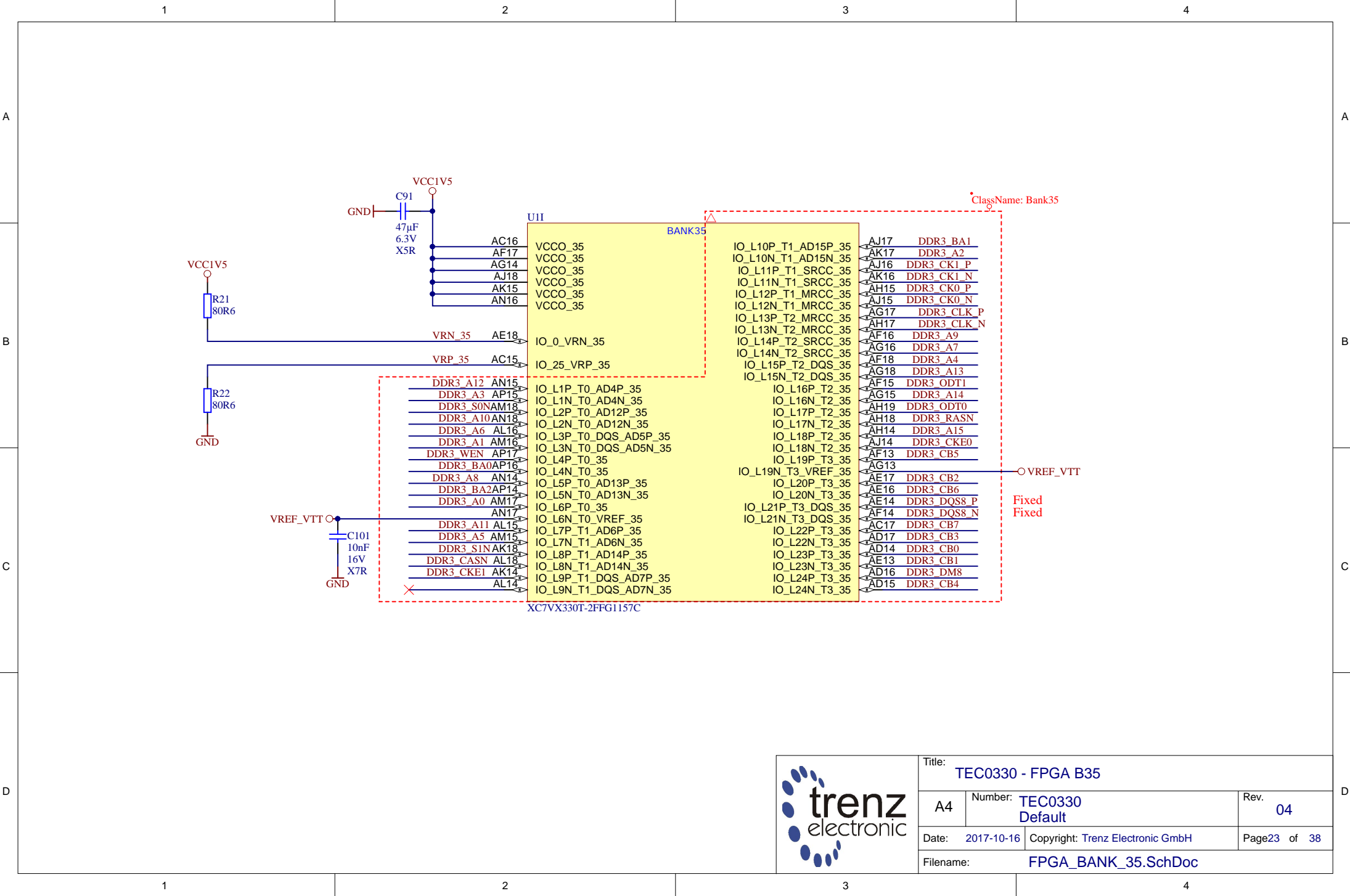
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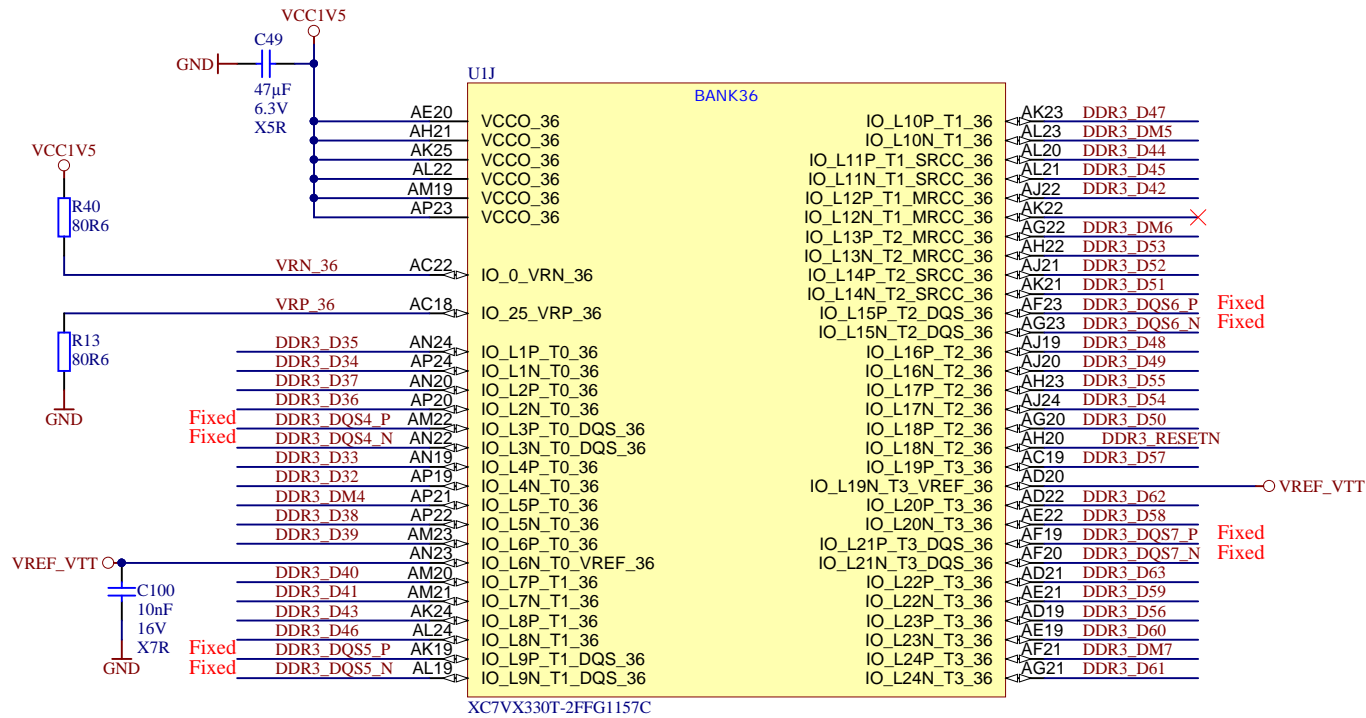
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Title: TEC0330 - FPGA B34		
A4	Number: TEC0330 Default	Rev. 04
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Filename: FPGA_BANK_34.SchDoc		

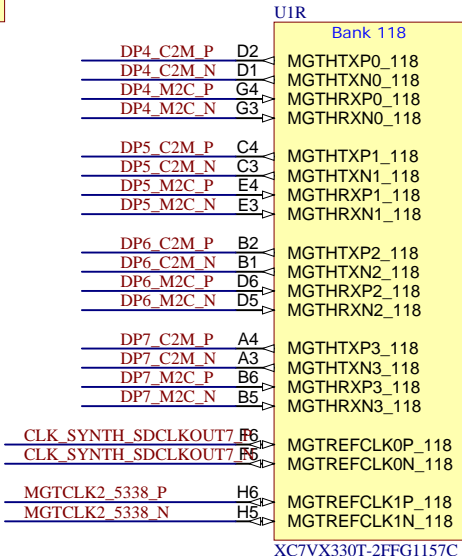
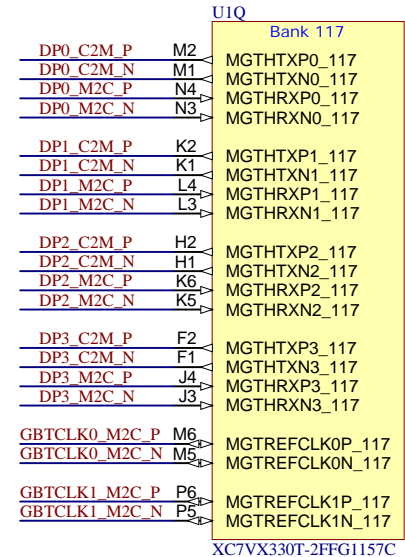
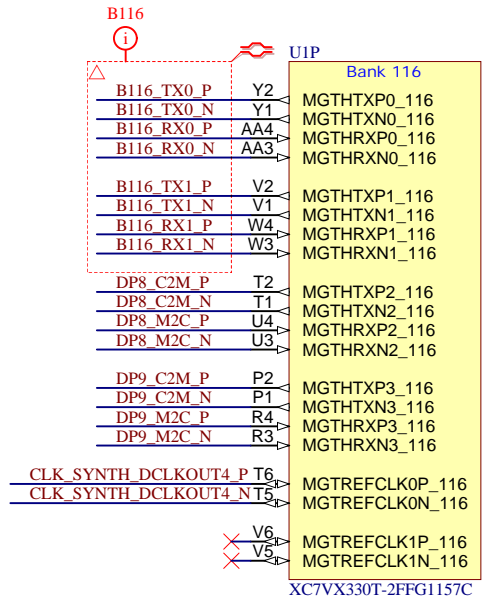
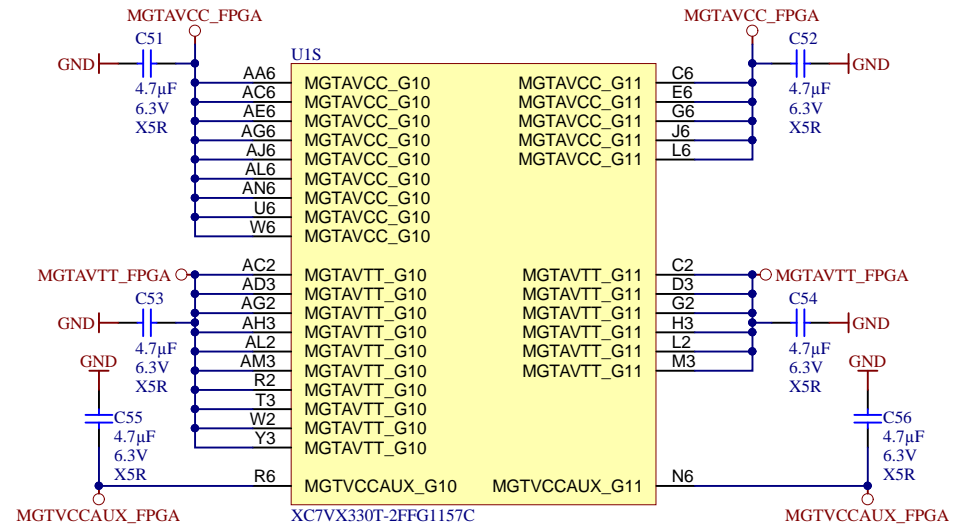
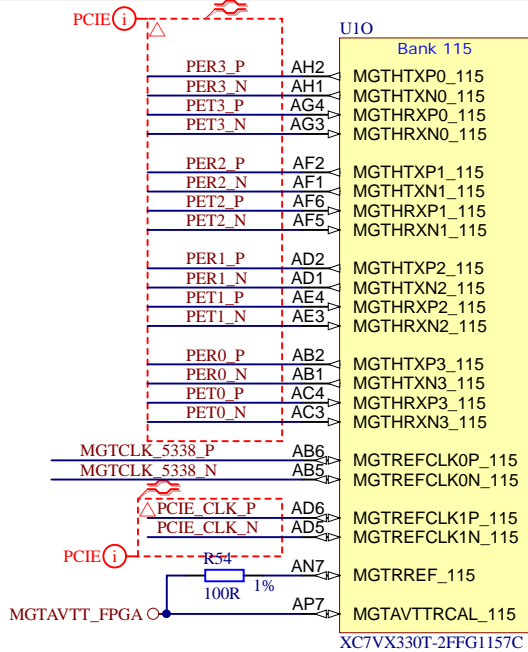
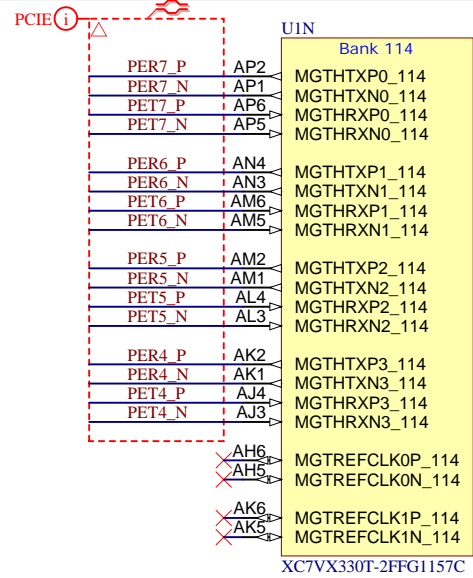


	Title: <b>TEC0330 - FPGA B35</b>	
	A4	Number: <b>TEC0330 Default</b>
	Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Rev. <b>04</b>	
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Filename: <b>FPGA_BANK_35.SchDoc</b>		



Title: <b>TEC0330 - FPGA B36</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>24</b> of <b>38</b>
Filename: <b>FPGA_BANK_36.SchDoc</b>		





Title: <b>TEC0330 - FPGA MGT BANKS</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>FPGA_MGT_BANKS.SchDoc</b>		

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U\_FPGA\_BANK\_19  
FPGA\_BANK\_19.SchDoc



U\_FPGA\_BANK\_37  
FPGA\_BANK\_37.SchDoc



U\_FPGA\_BANK\_38  
FPGA\_BANK\_38.SchDoc



U\_FPGA\_BANK\_39  
FPGA\_BANK\_39.SchDoc



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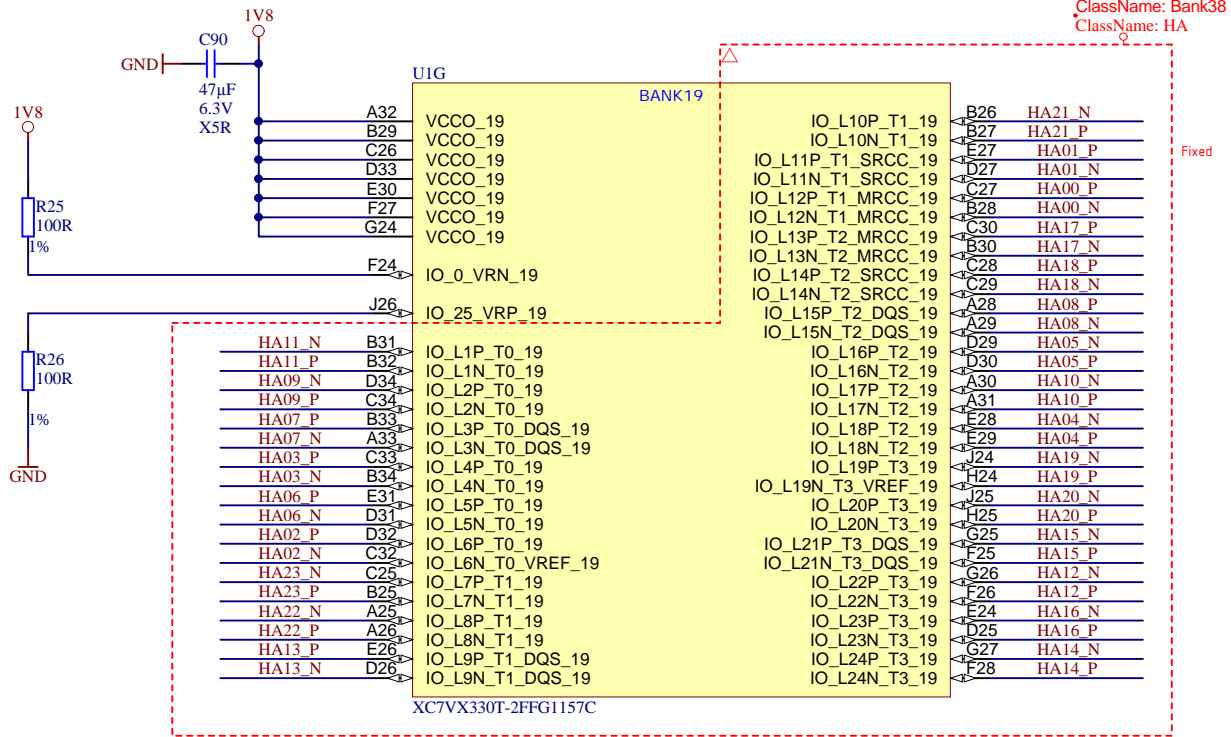
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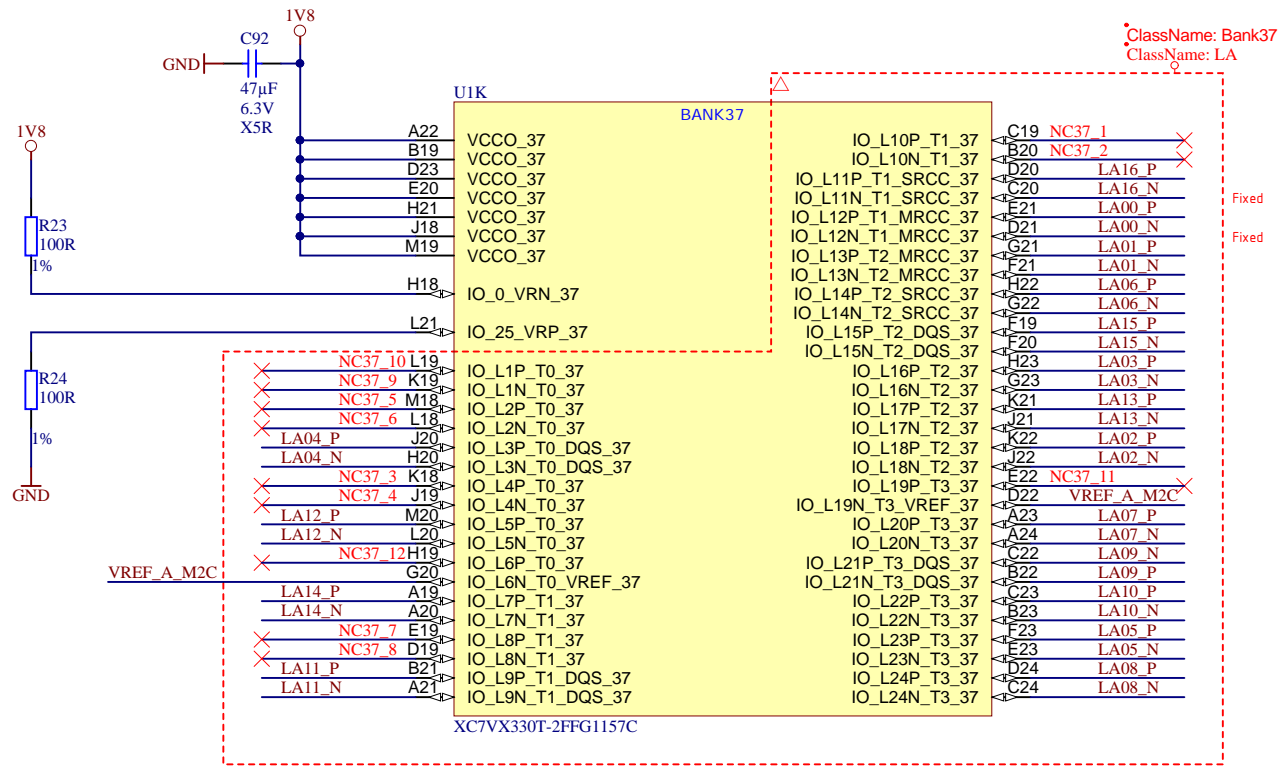
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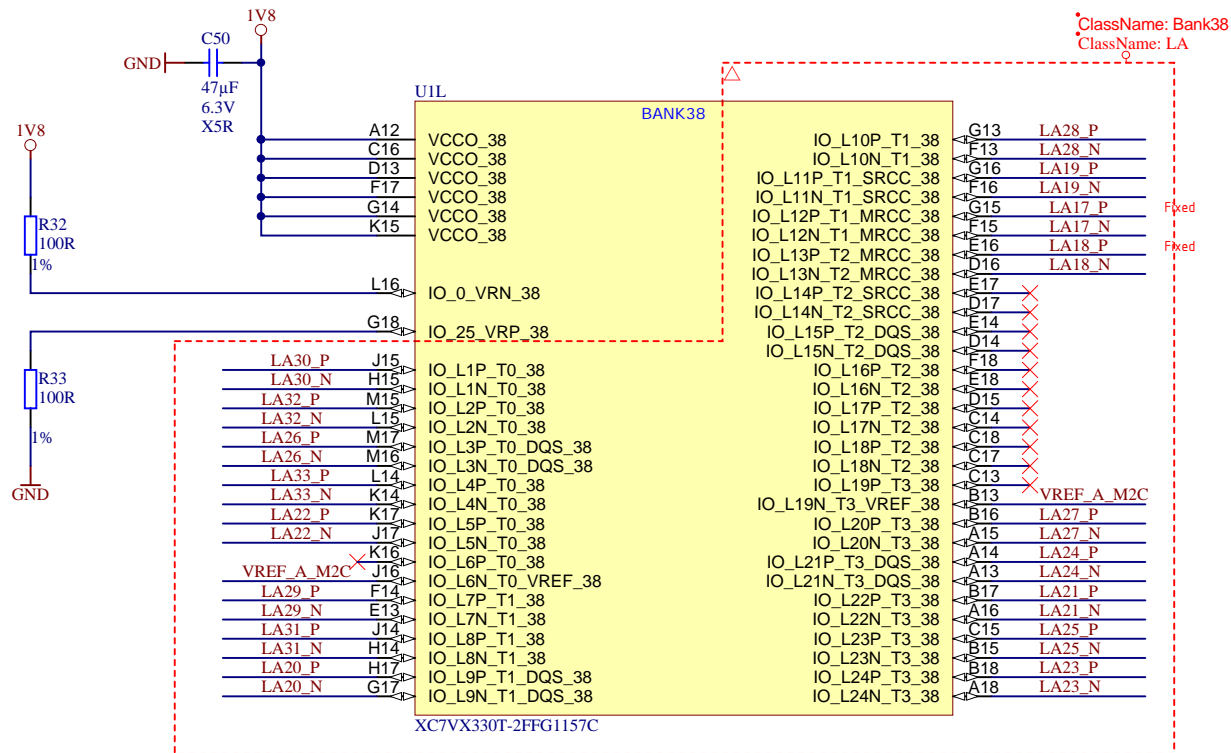
Title: <b>TEC0330 - FMC_BANKS</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>26</b> of <b>38</b>
Filename: <b>FMC_Banks.SchDoc</b>		




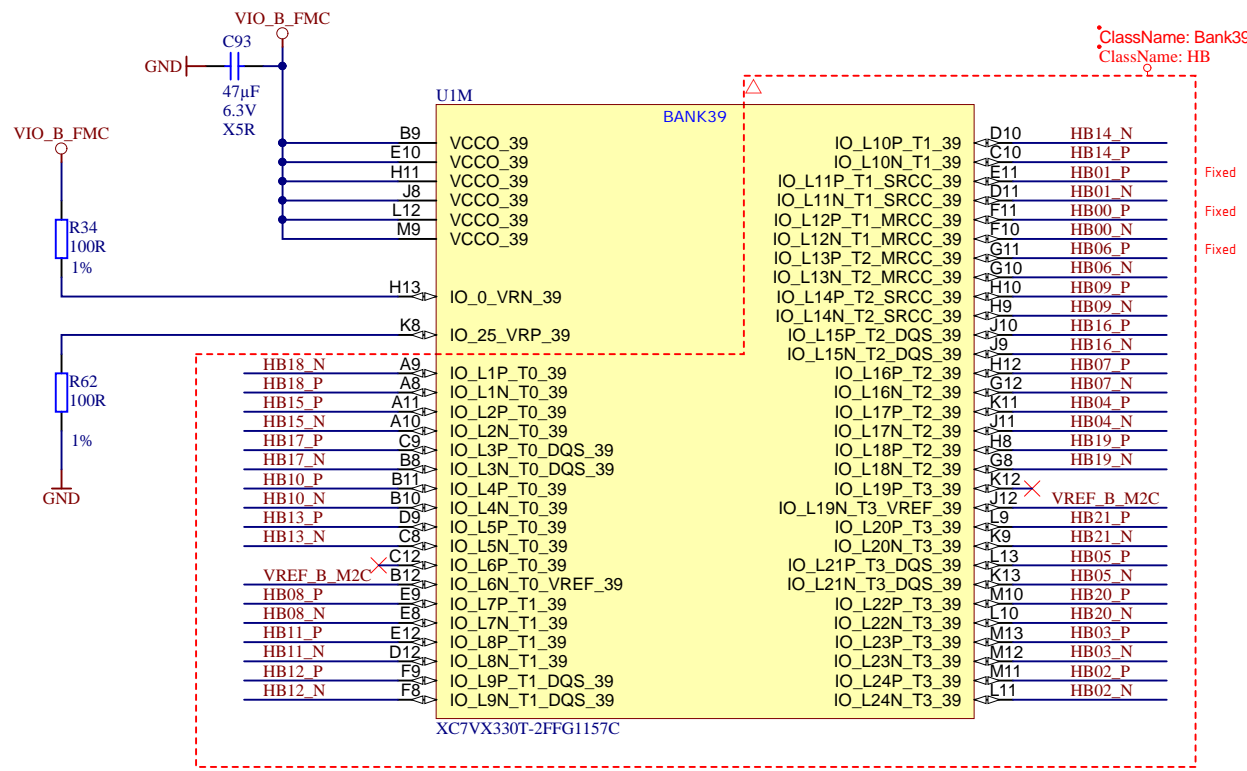
	Title: TEC0330 - FPGA B19		
	A4	Number: TEC0330 Default	Rev. 04
	Date: 2017-10-16	Copyright: Trenz Electronic GmbH	Page27 of 38
	Filename: FPGA_BANK_19.SchDoc		



Title: TEC0330 - FPGA B37		
A4	Number: TEC0330 Default	Rev. 04
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Filename: FPGA_BANK_37.SchDoc		



	Title: <b>TEC0330 - FPGA B38</b>		
	A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
	Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>29</b> of <b>38</b>
	Filename: <b>FPGA_BANK_38.SchDoc</b>		



Title: <b>TEC0330 - FPGA B39</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>30</b> of <b>38</b>
Filename: <b>FPGA_BANK_39.SchDoc</b>		

A

A

B

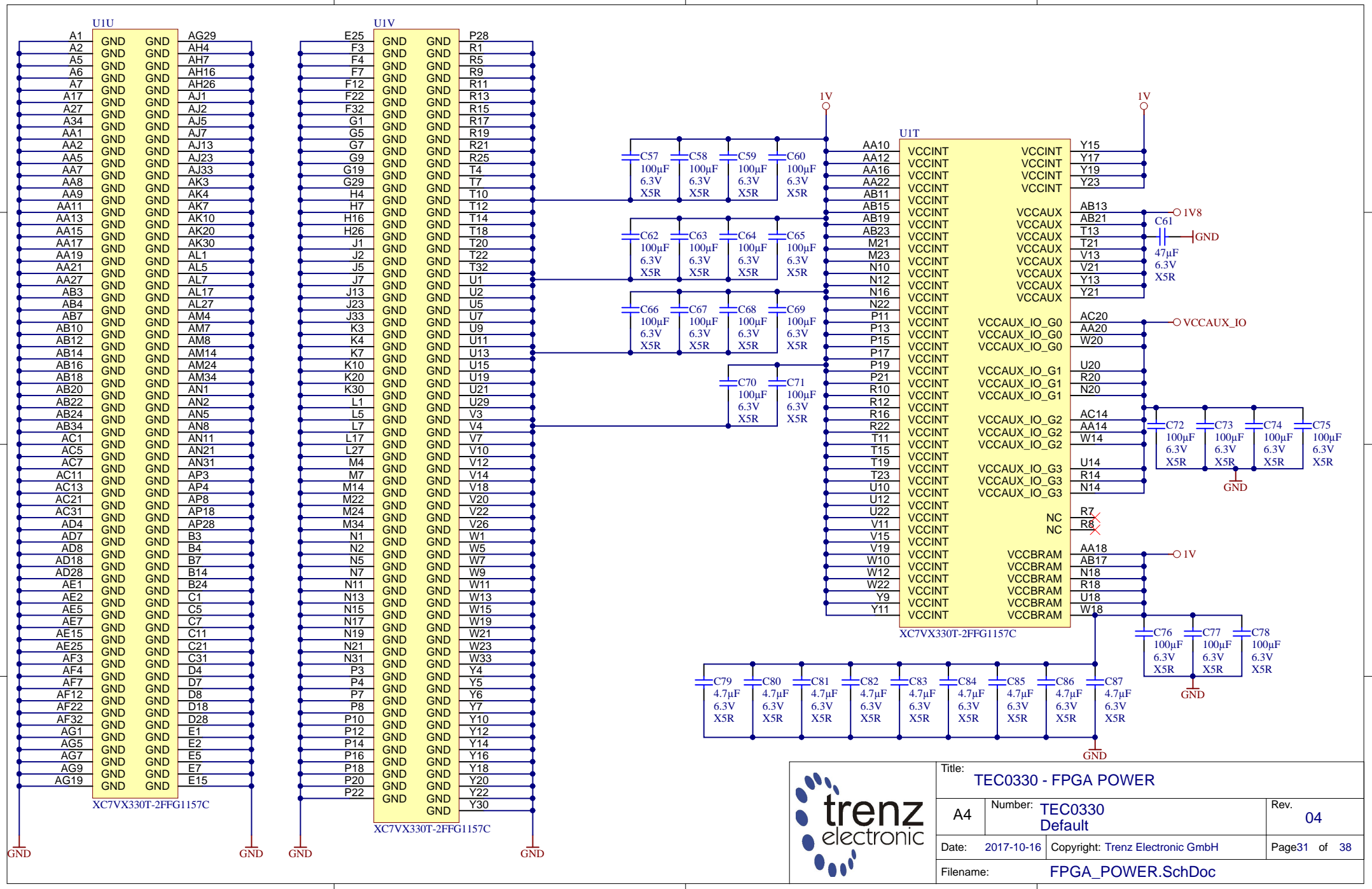
B

C

C

D

D



1

2

3

4

U\_PWR\_4V\_1V5  
PWR\_4V\_1V5.SchDoc



U\_PWR\_3V3  
PWR\_3V3.SchDoc



U\_PWR\_1V  
PWR\_1V.SchDoc



U\_PWR\_MGT  
PWR\_MGT.SchDoc



U\_PWR\_1V8  
PWR\_1V8.SchDoc



U\_PWR\_5V  
PWR\_5V.SchDoc



A

A

B

B

C

C

D


D

1

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4

	Title: <b>TEC0330 - POWER</b>		
	A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
	Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>32</b> of <b>38</b>
	Filename: <b>POWER.SchDoc</b>		



A

B

C

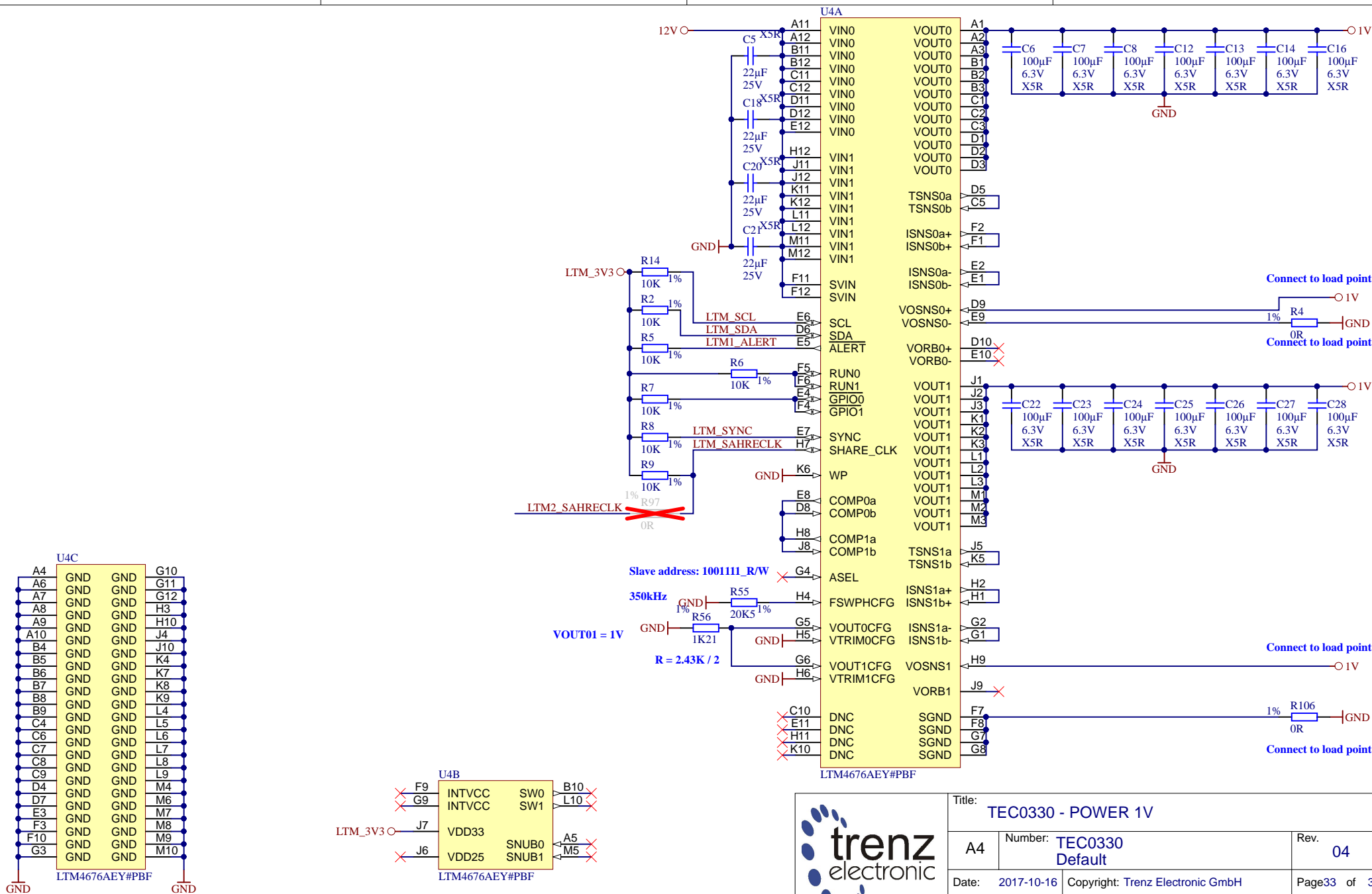
D

A

B

C

D



Title: <b>TEC0330 - POWER 1V</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: 2017-10-16	Copyright: Trenz Electronic GmbH	Page33 of 38
Filename: <b>PWR_1V.SchDoc</b>		

1

2

3

4

A

A

B

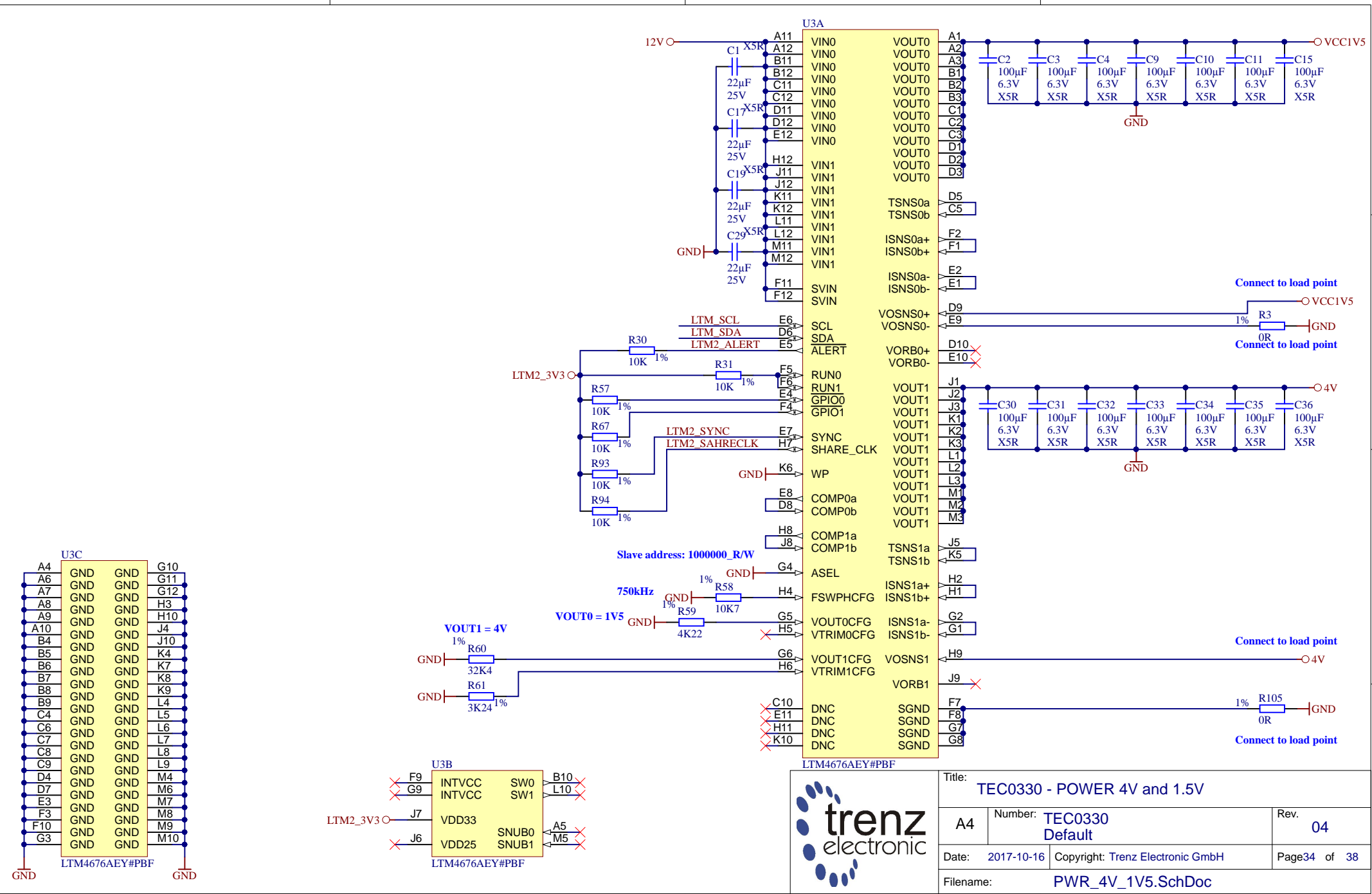
B

C

C

D

D



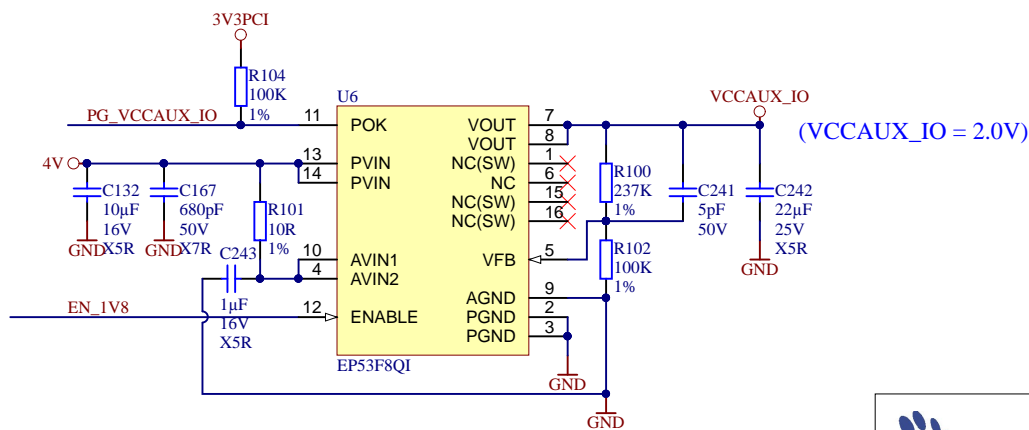
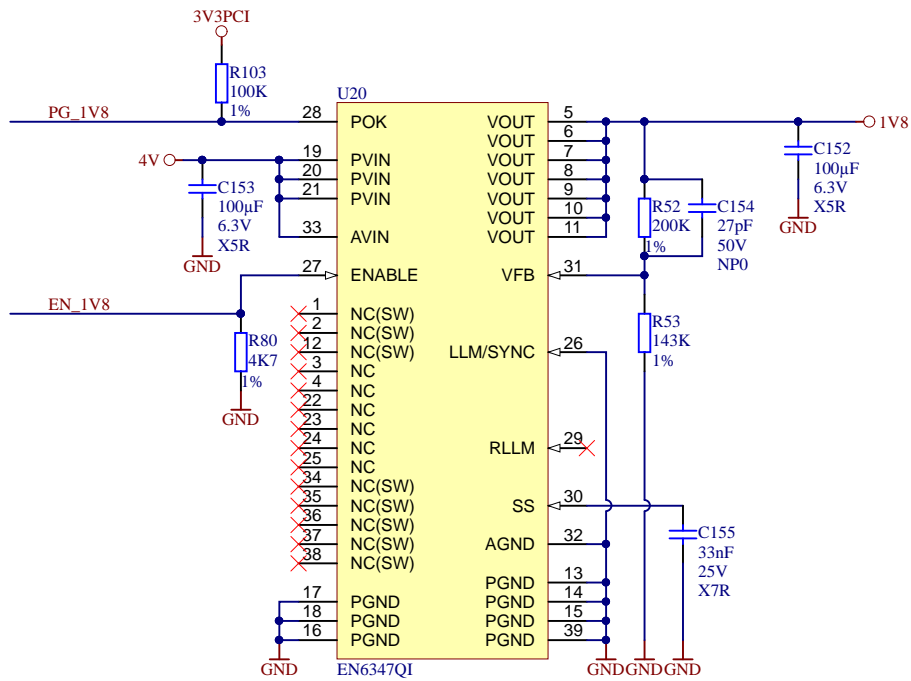
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A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
Date: <b>2017-10-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>34</b> of <b>38</b>
Filename: <b>PWR_4V_1V5.SchDoc</b>		

1

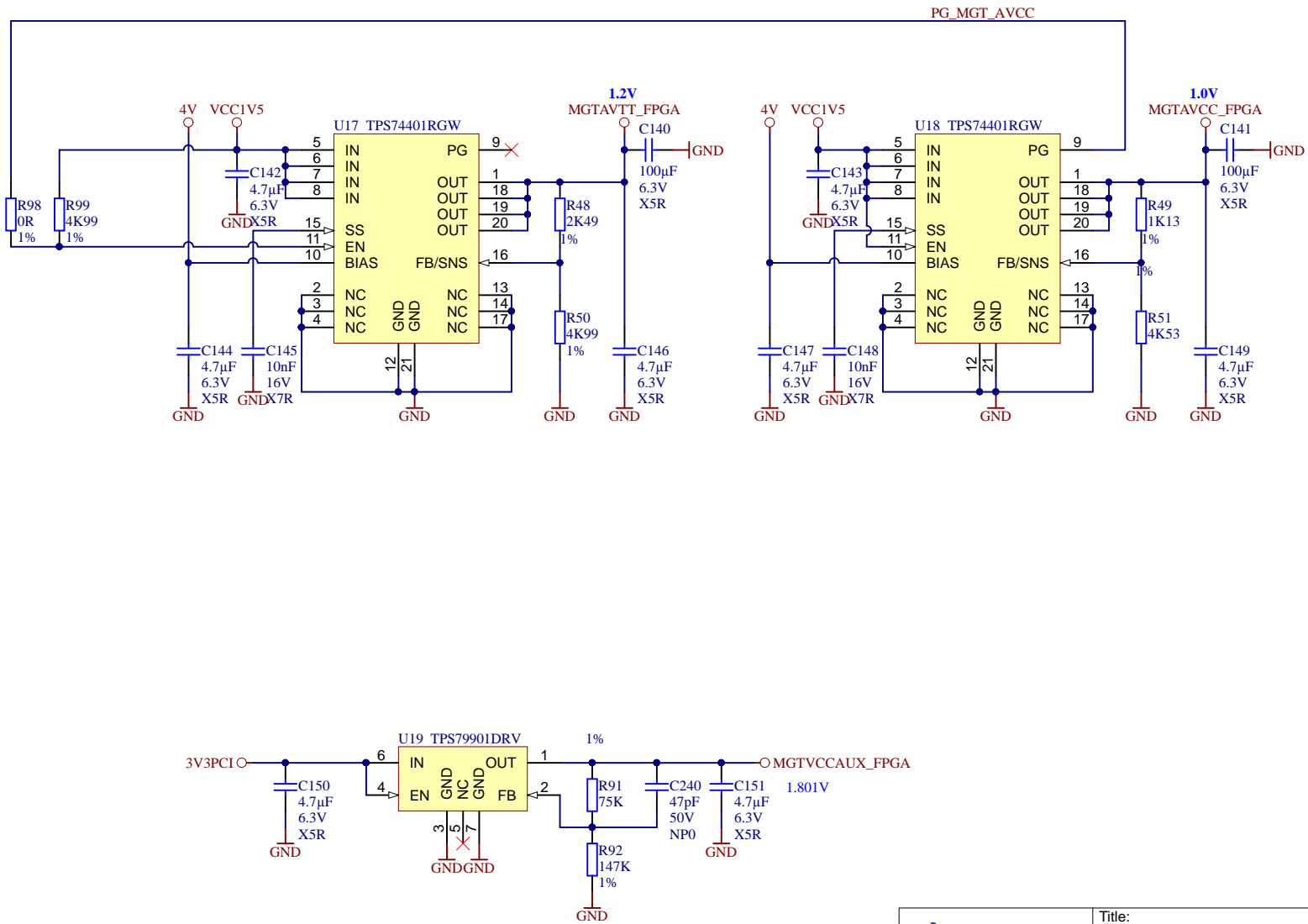
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3

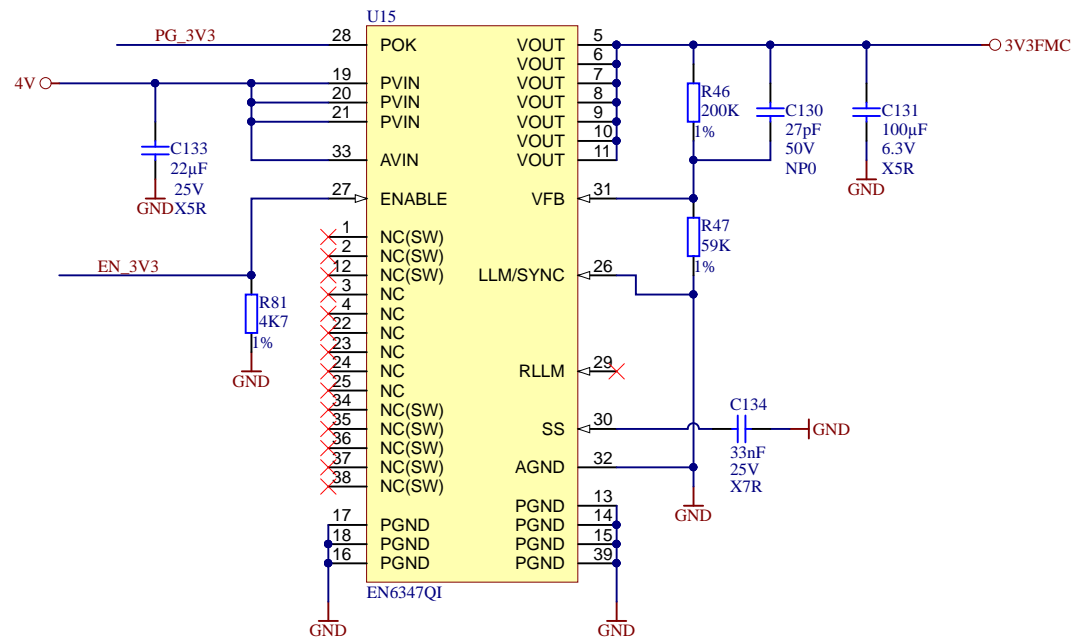
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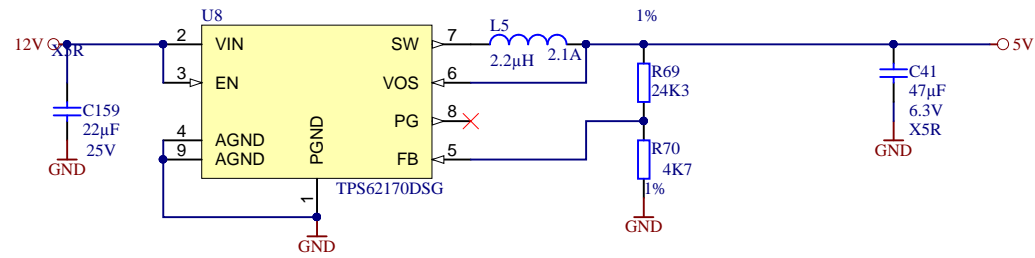
Title: TEC0330 - POWER 1V8		
A4	Number: TEC0330 Default	Rev. 04
Date: 2017-10-16	Copyright: Trenz Electronic GmbH	Page 35 of 38
Filename: PWR_1V8.SchDoc		




Title: <b>TEC0330 - POWER MGT</b>		
A4	Number: <b>TEC0330 Default</b>	Rev. <b>04</b>
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Filename: <b>PWR_MGT.SchDoc</b>		



		Title: TEC0330 - POWER 3V3FMC	
		A4	Number: TEC0330 Default
Date: 2017-10-16		Copyright: Trenz Electronic GmbH	
Filename: PWR_3V3.SchDoc		Page 37 of 38	



		Title: <b>TEC0330 - POWER 5V</b>	
		A4	Number: <b>TEC0330 Default</b>
Date: 2017-10-16		Copyright: Trenz Electronic GmbH	
Filename: <b>PWR_5V.SchDoc</b>		Page38 of 38	