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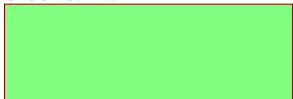
U_FPGA
FPGA.SchDoc



U_SODIMM
SODIMM.SchDoc



U_CLOCK
CLOCK.SchDoc



U_POWER
POWER.SchDoc



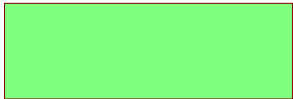
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B

U_CONN
CONN.SchDoc



U_CPLD
CPLD.SchDoc



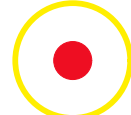
C

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PM1

PM2

PM3



FIDU-DOT - small

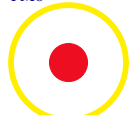
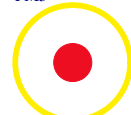
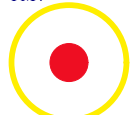
FIDU-DOT - small

FIDU-DOT - small

PM4

PM5

PM6



FIDU-DOT - small

FIDU-DOT - small

FIDU-DOT - small

Serial
Serial
Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT



Title: TEC0330 - Overview		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 1 of 39
Filename: TEC0330.SchDoc		

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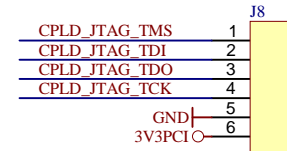
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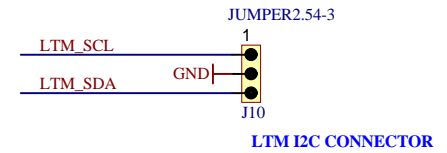
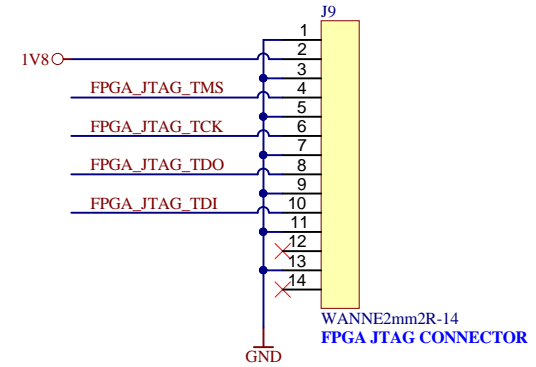
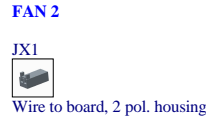
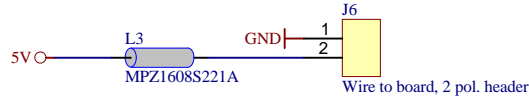
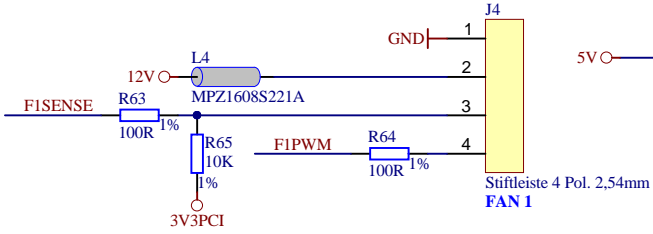
U_FMC
FMC.SchDoc

U_PCIE_CONN
PCIE_CONN.SchDoc

U_MLVDS_CONN
MLVDS_CONN.SchDoc



Placeholder 1 row 6 pin header
CPLD JTAG CONNECTOR



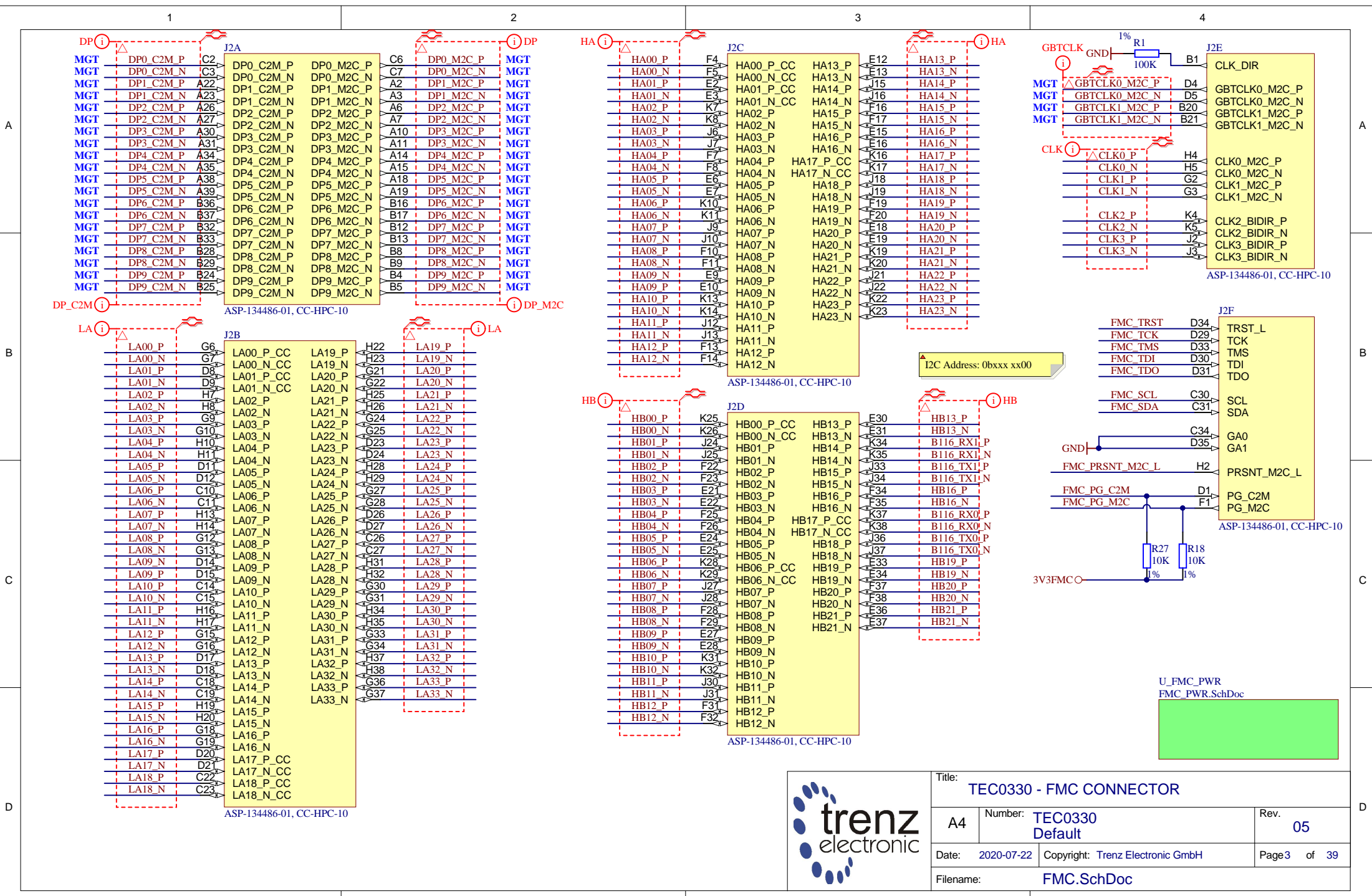
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	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 2 of 39
	Filename: CONN.SchDoc		


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			Title: TEC0330 - FMC CONNECTOR	
			A4	Number: TEC0330 Default
Date: 2020-07-22		Copyright: Trenz Electronic GmbH		Page 3 of 39
Filename: FMC.SchDoc				

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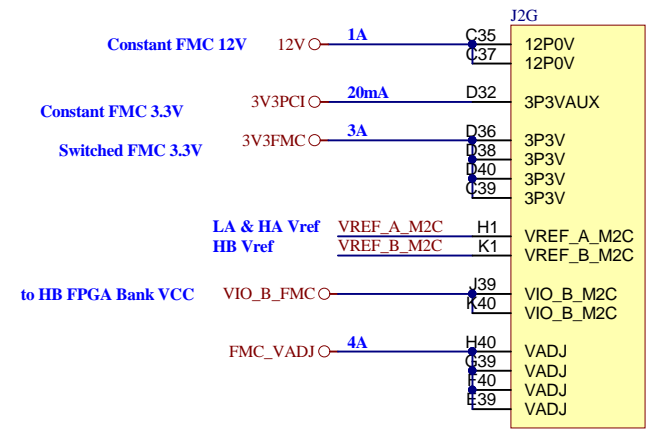
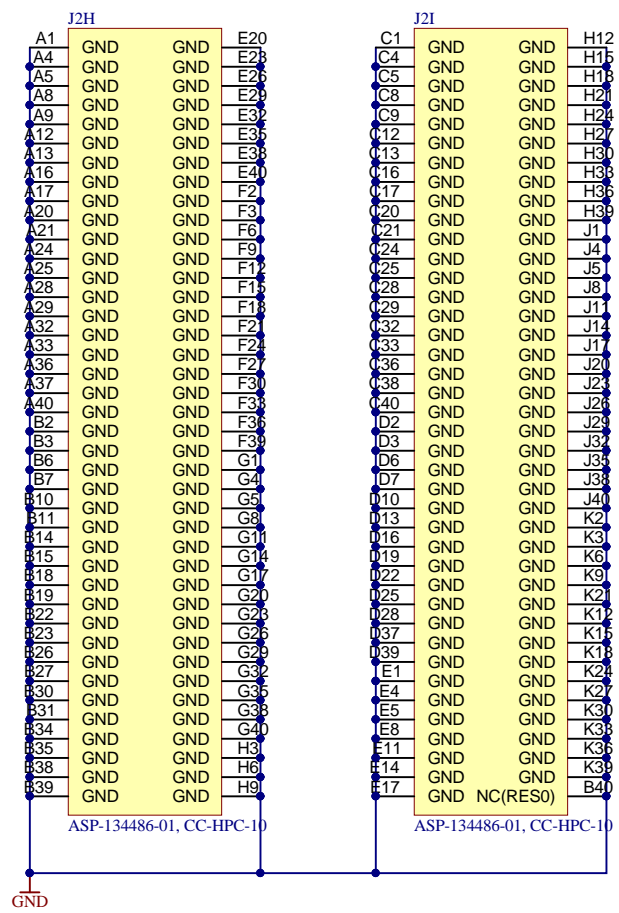
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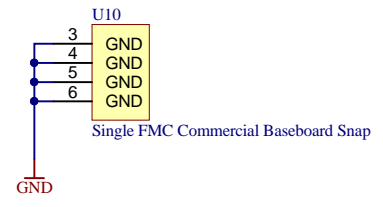
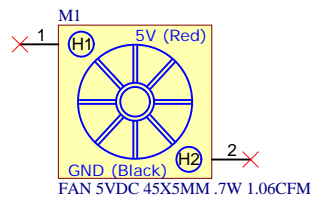
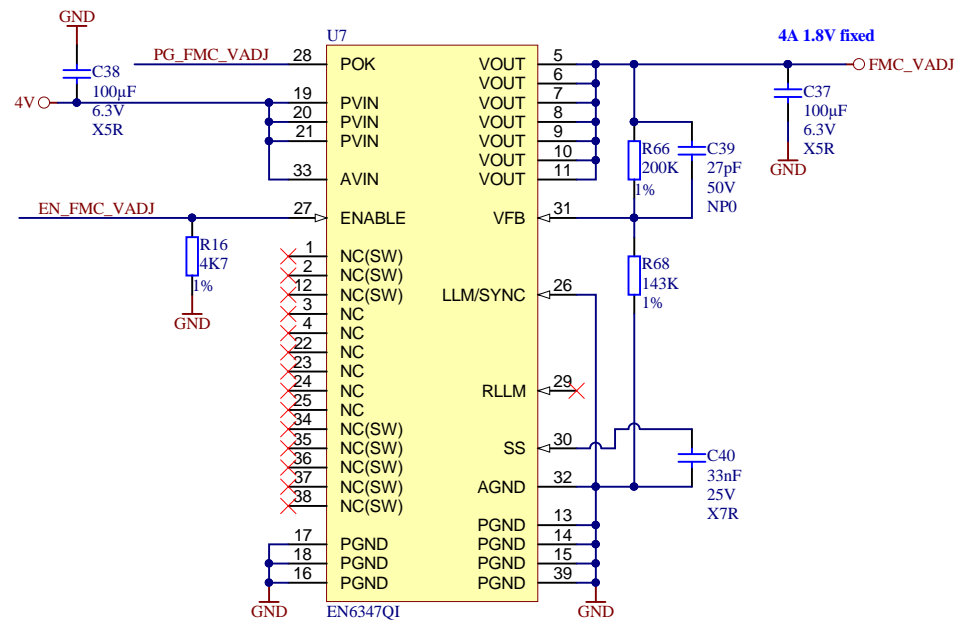
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ASP-134486-01, CC-HPC-10



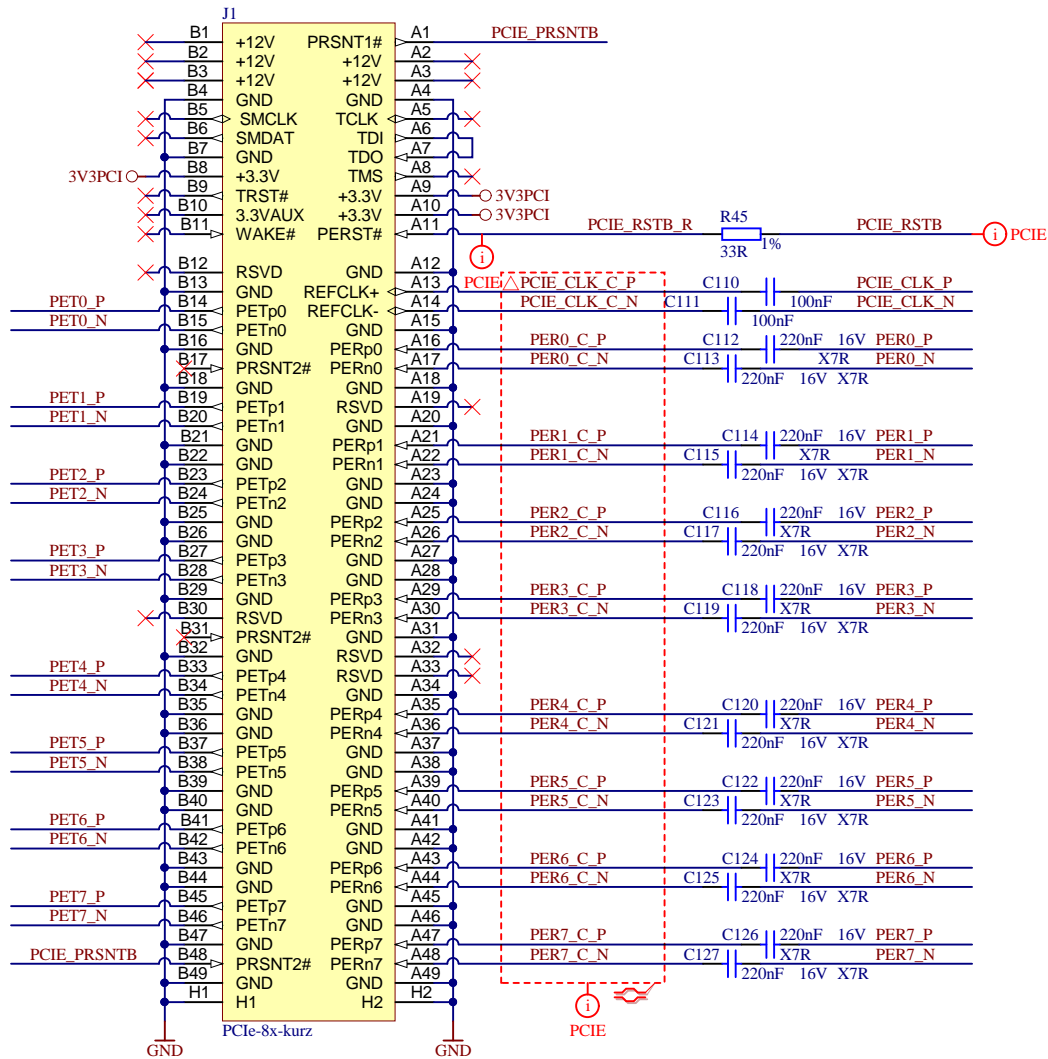
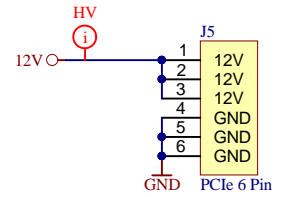
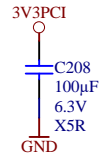
Title: TEC0330 - FMC CONNECTOR POWER		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 4 of 39
Filename: FMC_PWR.SchDoc		


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			Title: TEC0330 - PCIe CONNECTOR	
			A4	Number: TEC0330 Default
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Filename: PCIe_CONN.SchDoc				

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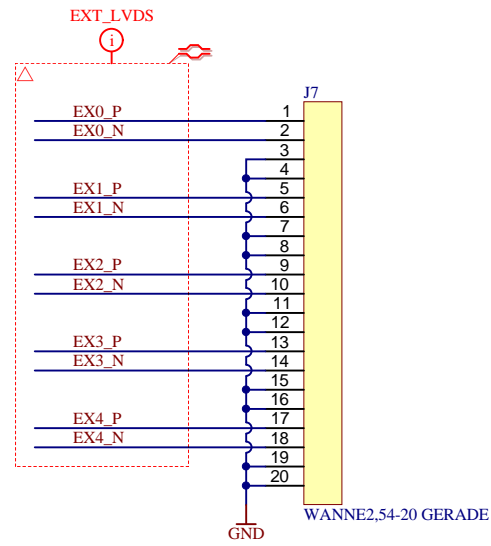
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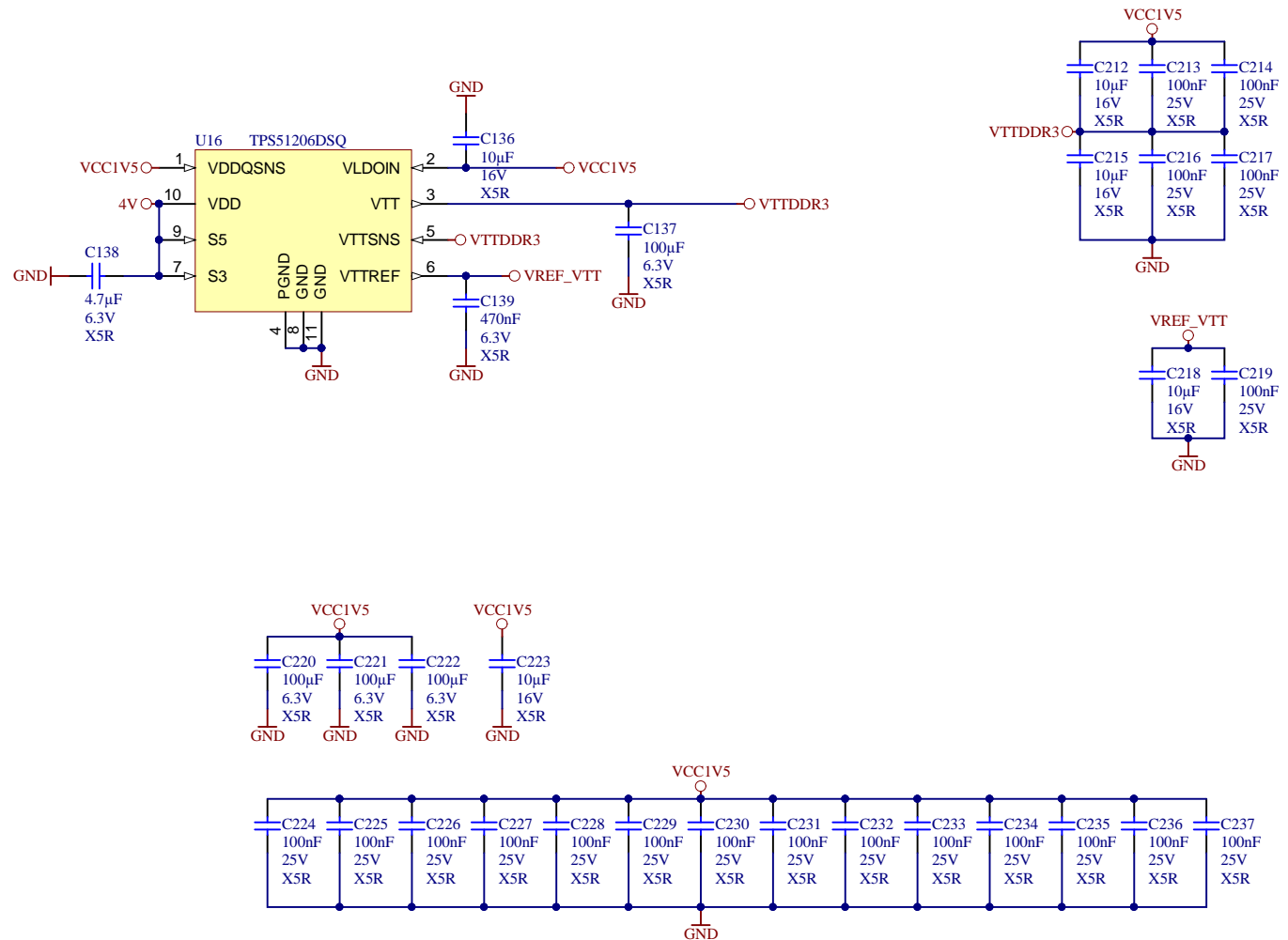
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	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 6 of 39
	Filename: MLVDS_CONN.SchDoc		


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	Title: TEC0330 - SODIMM MEMORY	
	A4	Number: TEC0330 Default
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	Filename: SODIMM_PWR.SchDoc	

Rev. **05**
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U_CLK_SYNTH
CLK_SYNTH.SchDoc



U_CLK-SI5338
CLK-SI5338.SchDoc



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	Title: TEC0330 - CLOCKS		
	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 10 of 39
	Filename: CLOCK.SchDoc		

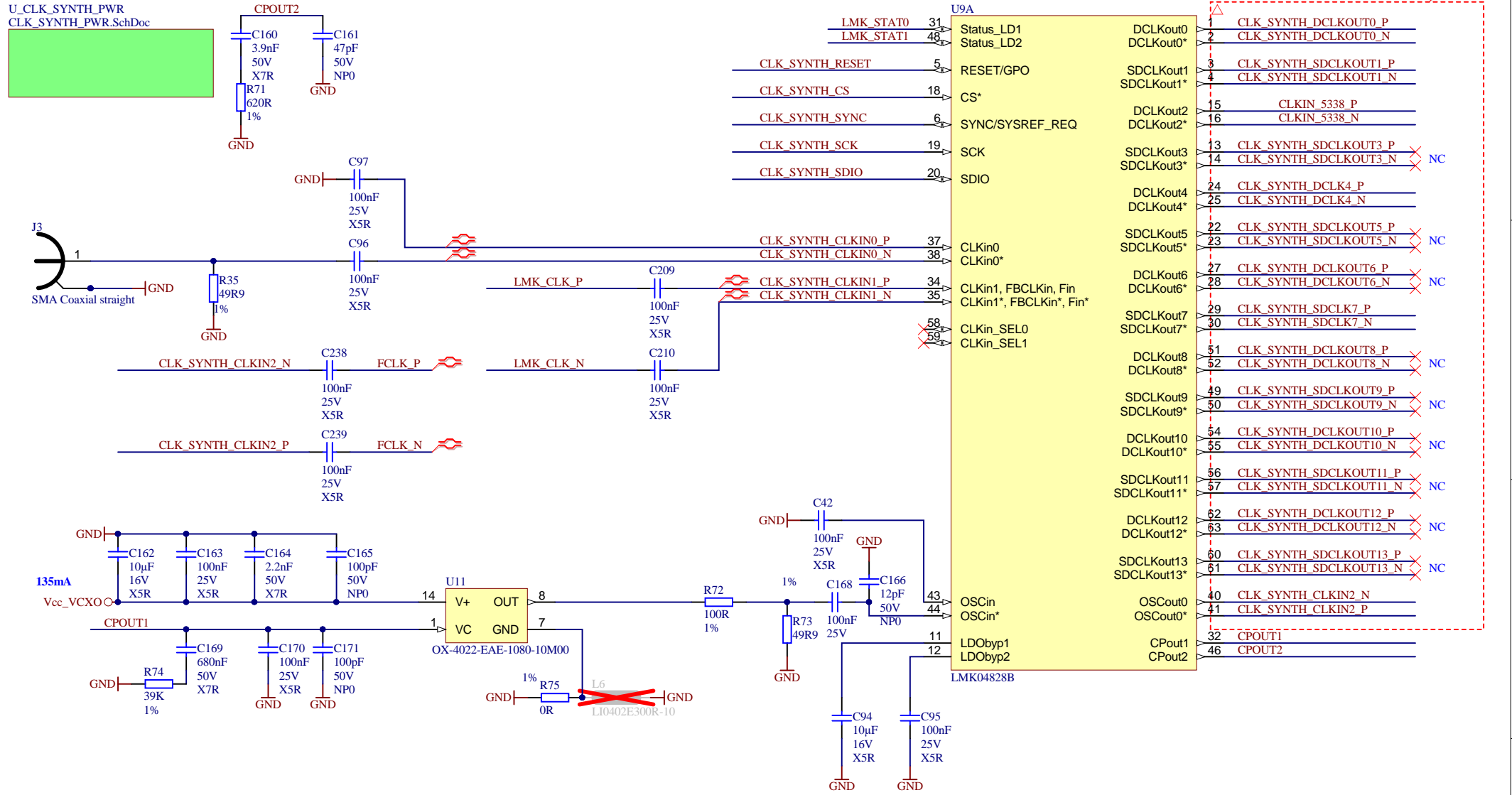
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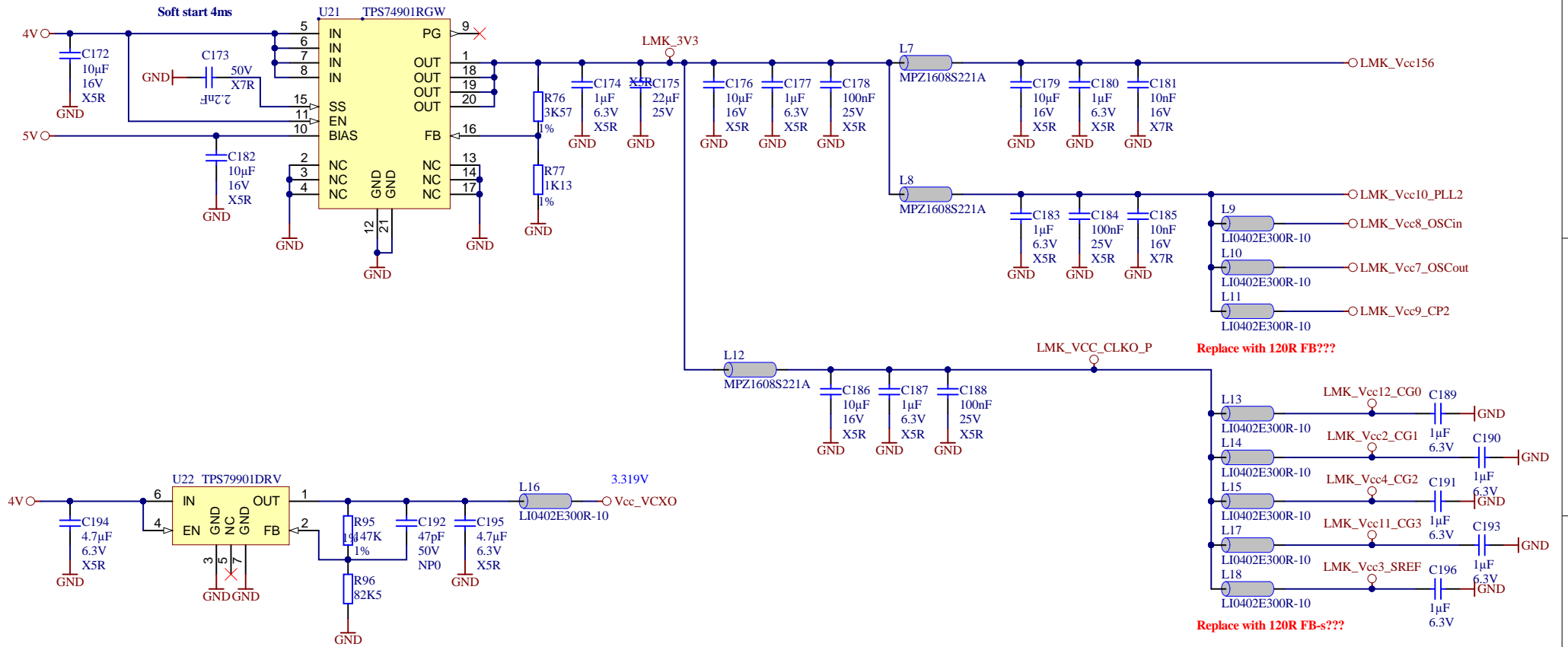
U_CLK_SYNTH_PWR
CLK_SYNTH_PWR.SchDoc



CLK_SYNTH_SDCLK7_P	C244	100nF	CLK_SYNTH_SDCLKOUT7_P
	X5R	25V	
CLK_SYNTH_SDCLK7_N	C245	100nF	CLK_SYNTH_SDCLKOUT7_N
	X5R	25V	
CLK_SYNTH_DCLK4_P	C246	100nF	CLK_SYNTH_DCLKOUT4_P
	X5R	25V	
CLK_SYNTH_DCLK4_N	C247	100nF	CLK_SYNTH_DCLKOUT4_N
	X5R	25V	



Title: TEC0330 - CLK_SYNTH		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 11 of 39
Filename: CLK_SYNTH.SchDoc		



U9B			
LMK_Vcc156	10	Vcc1_VCO	NC
LMK_Vcc2_CG1	17	Vcc2_CG1	NC
LMK_Vcc3_SREF	21	Vcc3_SYSREF	NC
LMK_Vcc4_CG2	26	Vcc4_CG2	
LMK_Vcc156	33	Vcc5_DIG	
LMK_Vcc156	36	Vcc6_PLL1	
LMK_Vcc156	39	Vcc7_OSCout0	
LMK_Vcc7_OSCout	42	Vcc8_OSCin	
LMK_Vcc8_OSCin	45	Vcc9_CP2	
LMK_Vcc9_CP2	47	Vcc10_PLL2	
LMK_Vcc10_PLL2	53	Vcc11_CG3	
LMK_Vcc11_CG3	64	Vcc12_CG0	GND
LMK_Vcc12_CG0			

LMK04828B



Title: TEC0330 - CLK_SYNTH_PWR		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 12 of 39
Filename: CLK_SYNTH_PWR.SchDoc		

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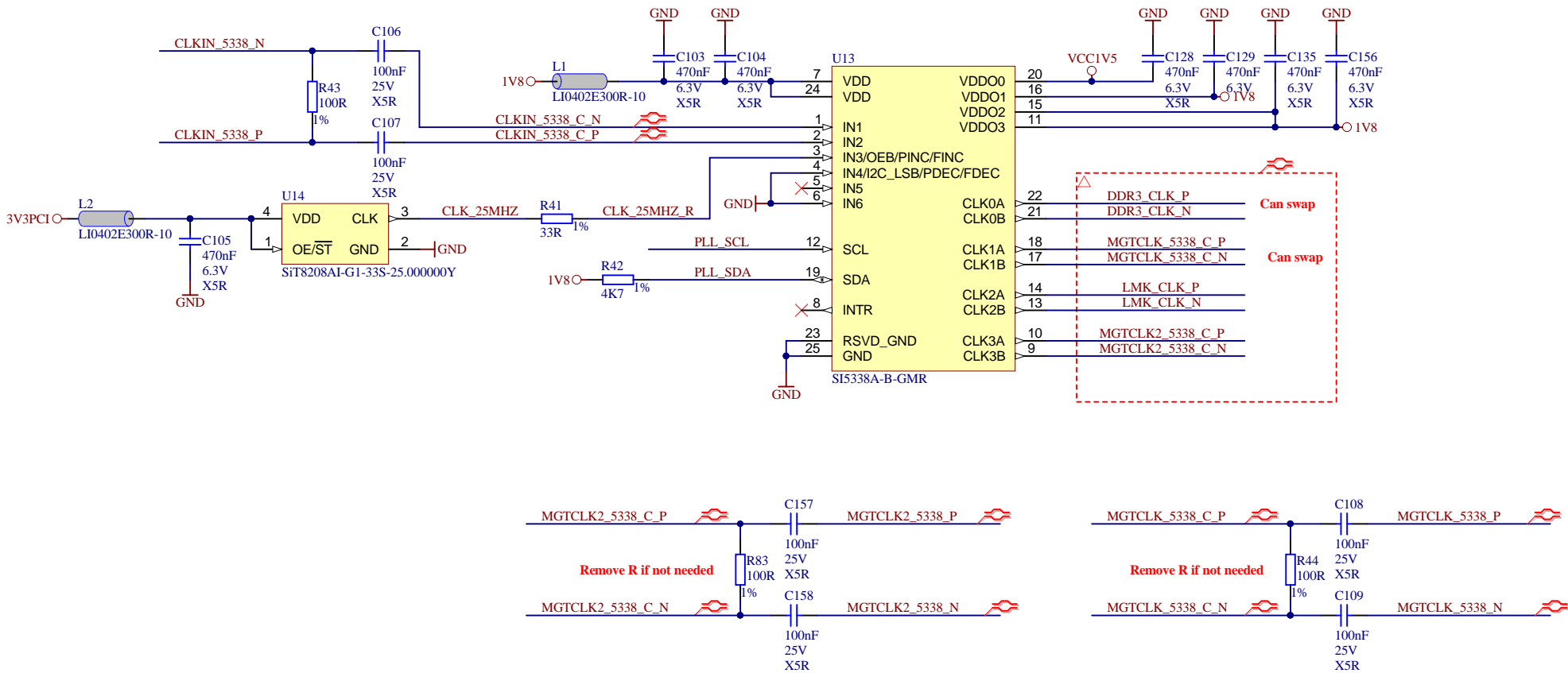
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		Title: TEC0330 - CLK_SI5338	
		A4	Number: TEC0330 Default
Date: 2020-07-22		Copyright: Trenz Electronic GmbH	
Filename: CLK-SI5338.SchDoc		Page 13 of 39	

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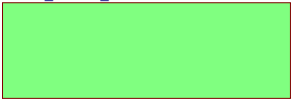
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FPGA_BANK_14.SchDoc



U_FPGA_BANK_15
FPGA_BANK_15.SchDoc



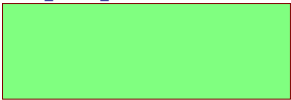
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FPGA_BANK_16.SchDoc



U_FPGA_BANK_17
FPGA_BANK_17.SchDoc



U_FPGA_BANK_18
FPGA_BANK_18.SchDoc



U_DDR_Banks
DDR_Banks.SchDoc



U_FMC_Banks
FMC_Banks.SchDoc



U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc



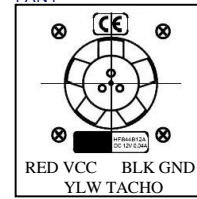
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FPGA_CFG.SchDoc



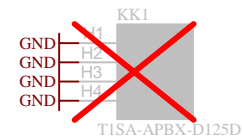
U_FPGA_POWER
FPGA_POWER.SchDoc




FAN1



HFB44B12A



TISA-APBX-D125D

	Title: TEC0330 - FPGA		
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	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 14 of 39
	Filename: FPGA.SchDoc		

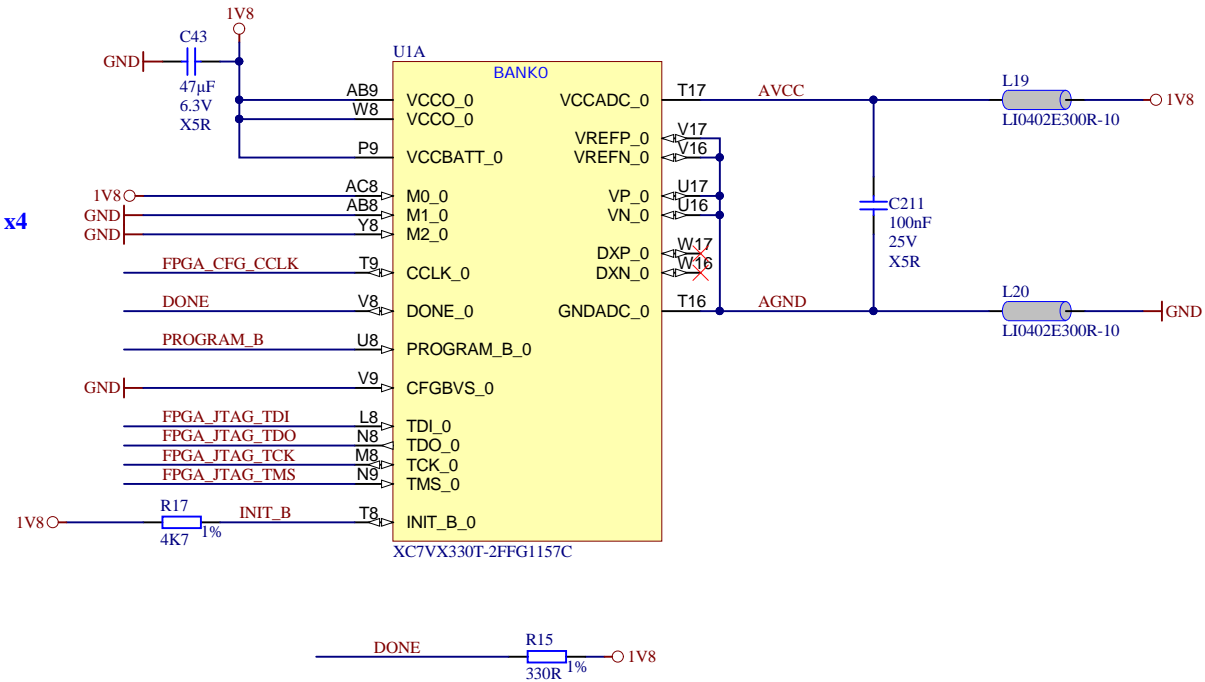
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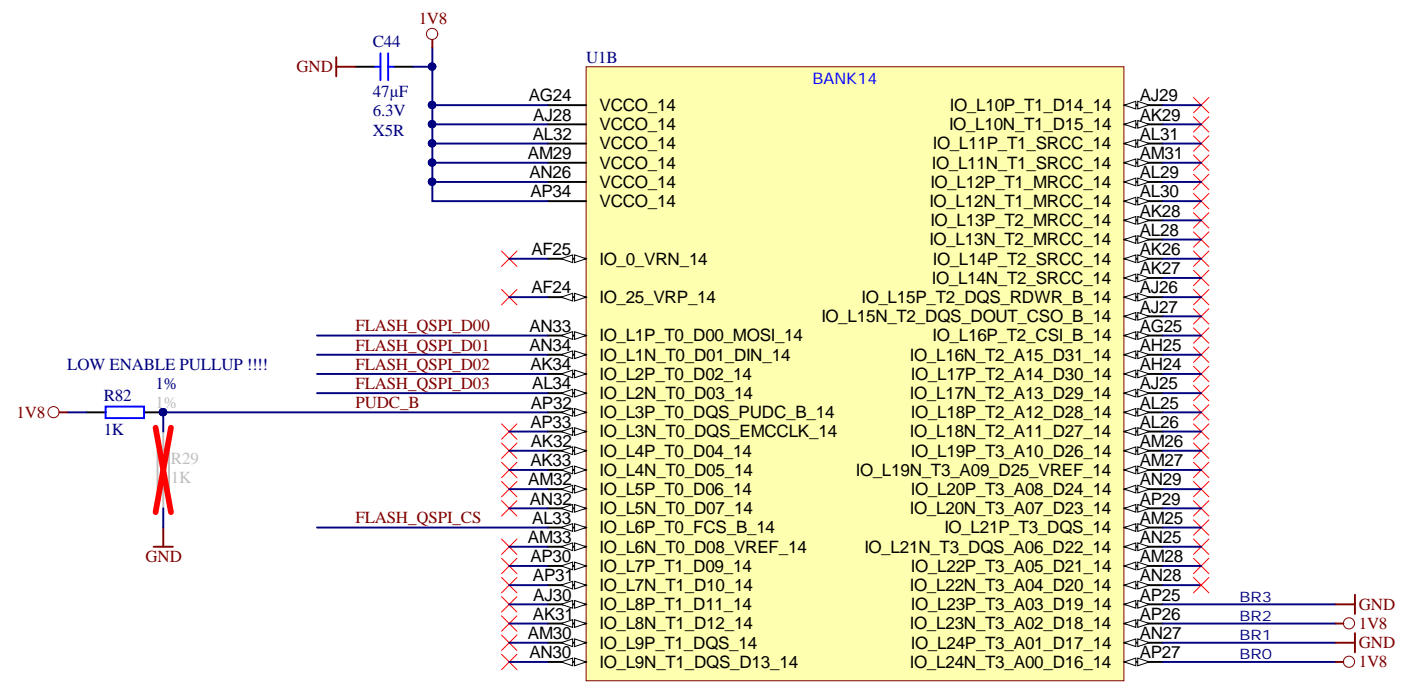
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MASTER SPI x4



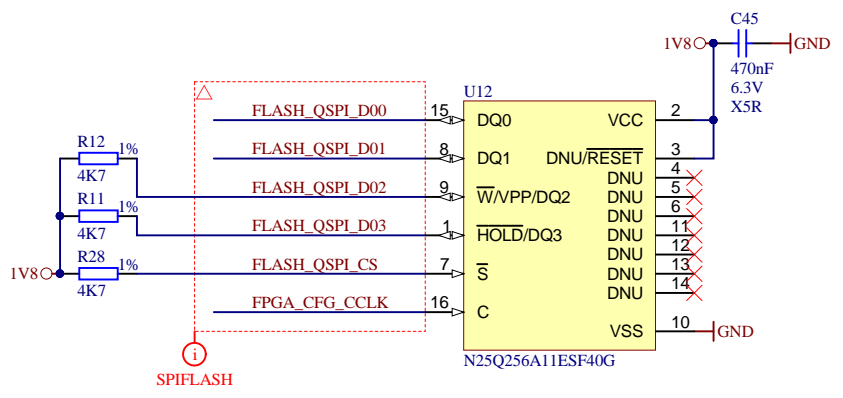
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	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 15 of 39
	Filename: FPGA_CFG.SchDoc		



XC7VX330T-2FFG1157C

Board Revisions

BR0 BR1 BR2 BR3
 1 0 1 0 | REV05

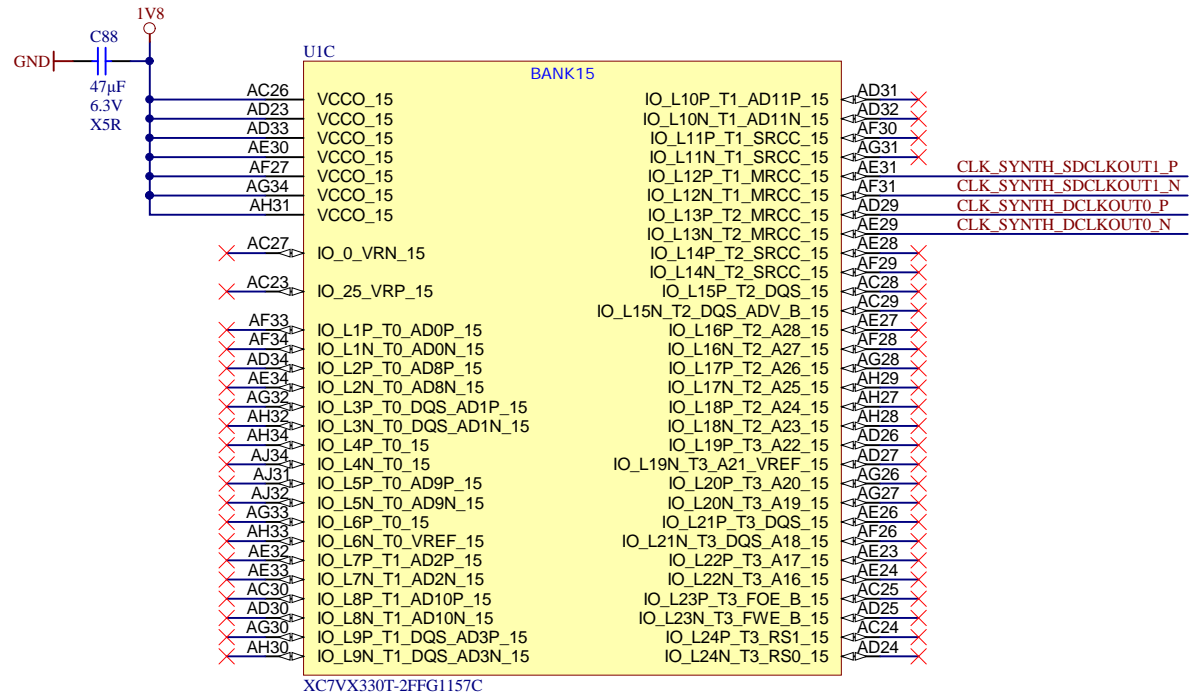


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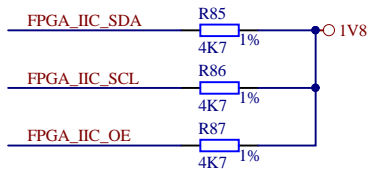
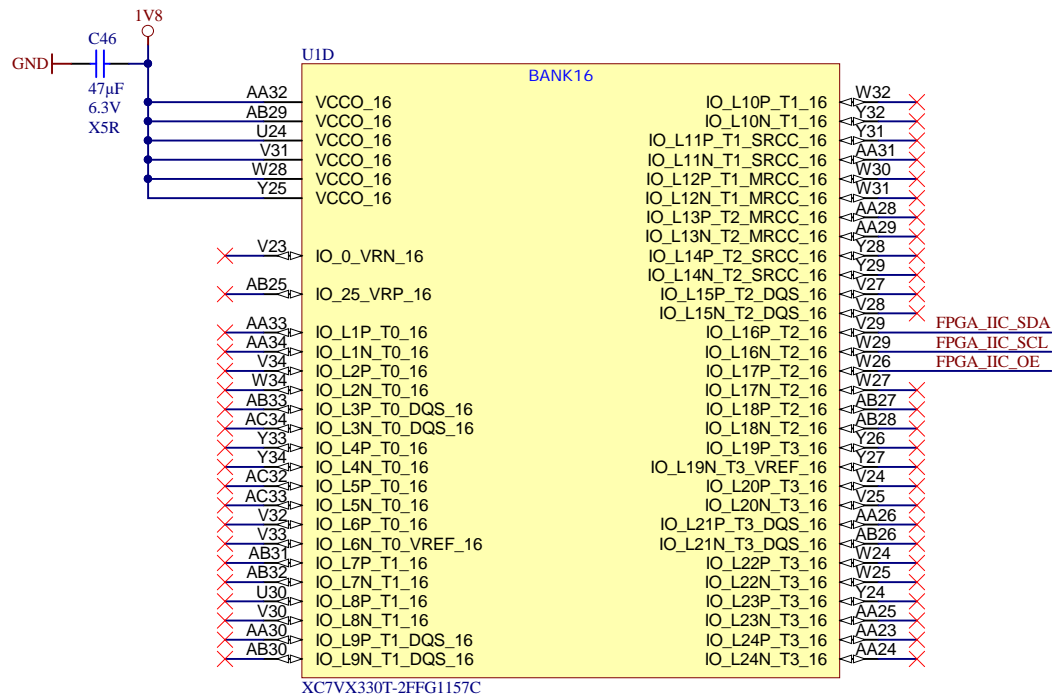
SPIFLASH




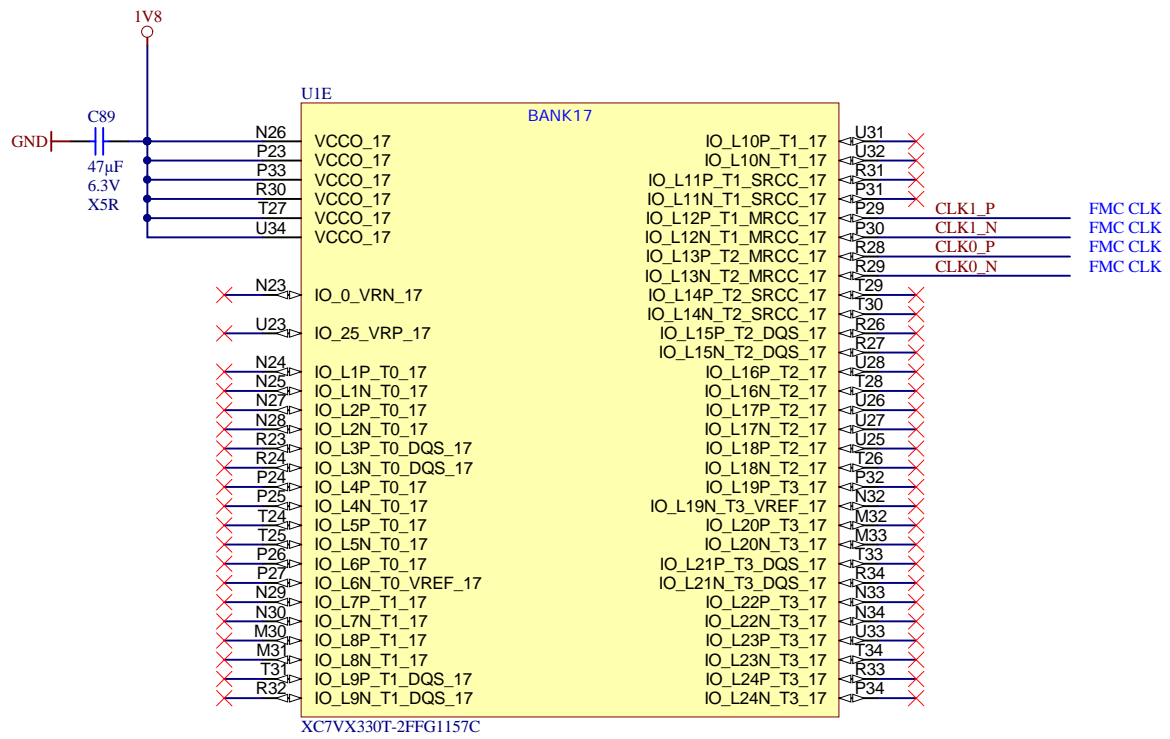
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A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 16 of 39
Filename: FPGA_BANK_14.SchDoc		




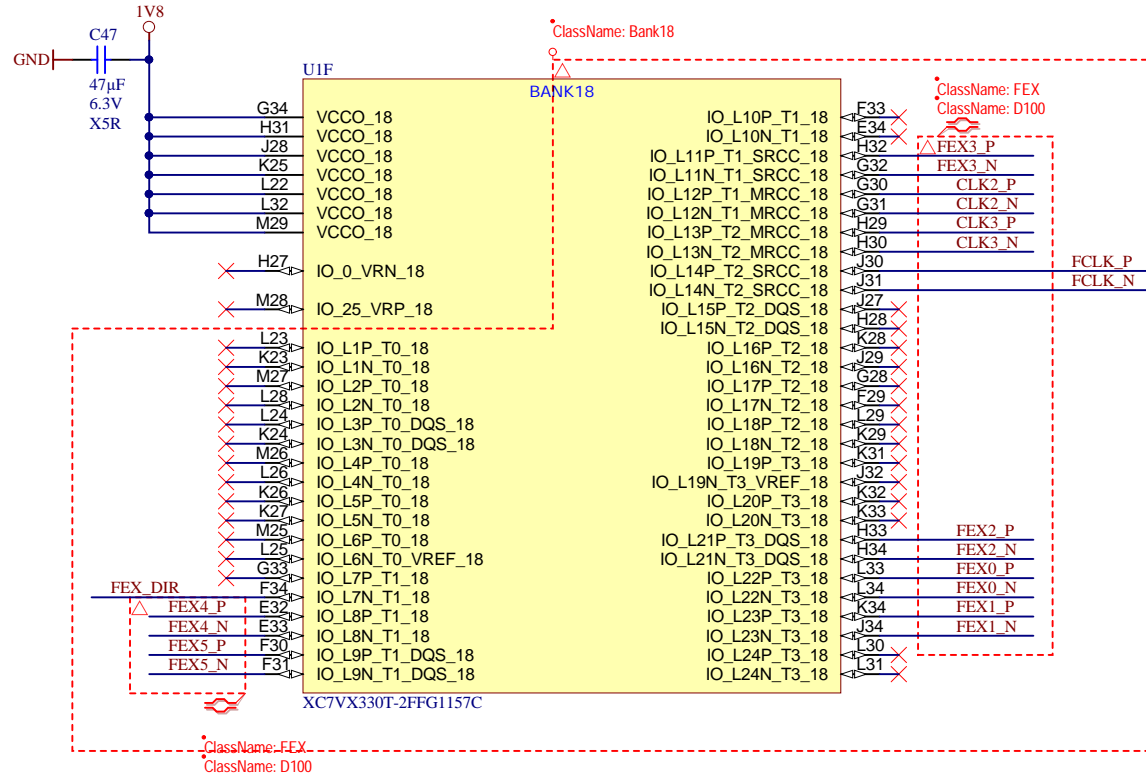
	Title: TEC0330 - FPGA B15		
	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 17 of 39
	Filename: FPGA_BANK_15.SchDoc		



		Title: TEC0330 - FPGA B16	
		A4	Number: TEC0330 Default
Date: 2020-07-22		Copyright: Trenz Electronic GmbH	
Filename: FPGA_BANK_16.SchDoc		Page 18 of 39	



	Title: TEC0330 - FPGA B17		
	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 19 of 39
	Filename: FPGA_BANK_17.SchDoc		



Title: TEC0330 - FPGA B18		
A4	Number: TEC0330 Default	Rev. 05
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Filename: FPGA_BANK_18.SchDoc		

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U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



U_FPGA_BANK_35
FPGA_BANK_35.SchDoc



U_FPGA_BANK_36
FPGA_BANK_36.SchDoc



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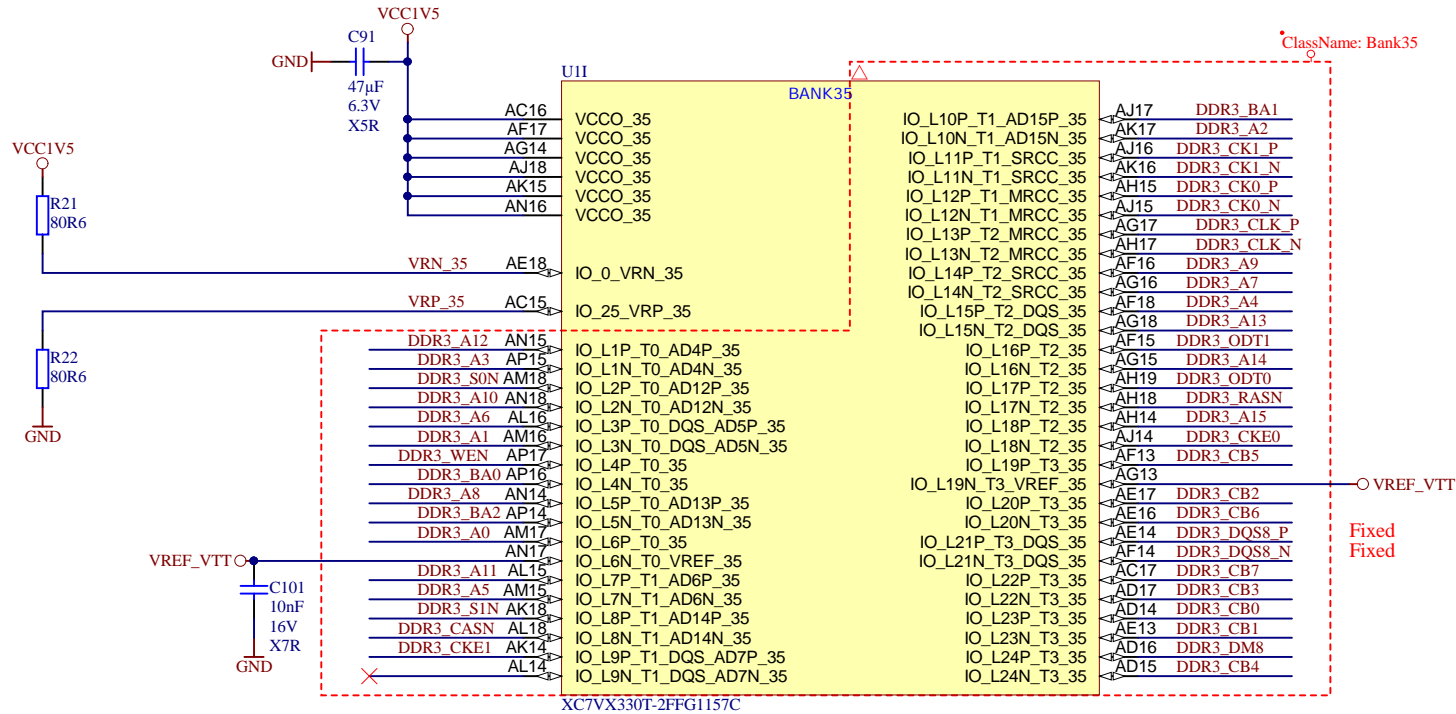
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A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 21 of 39
Filename: DDR_Banks.SchDoc		

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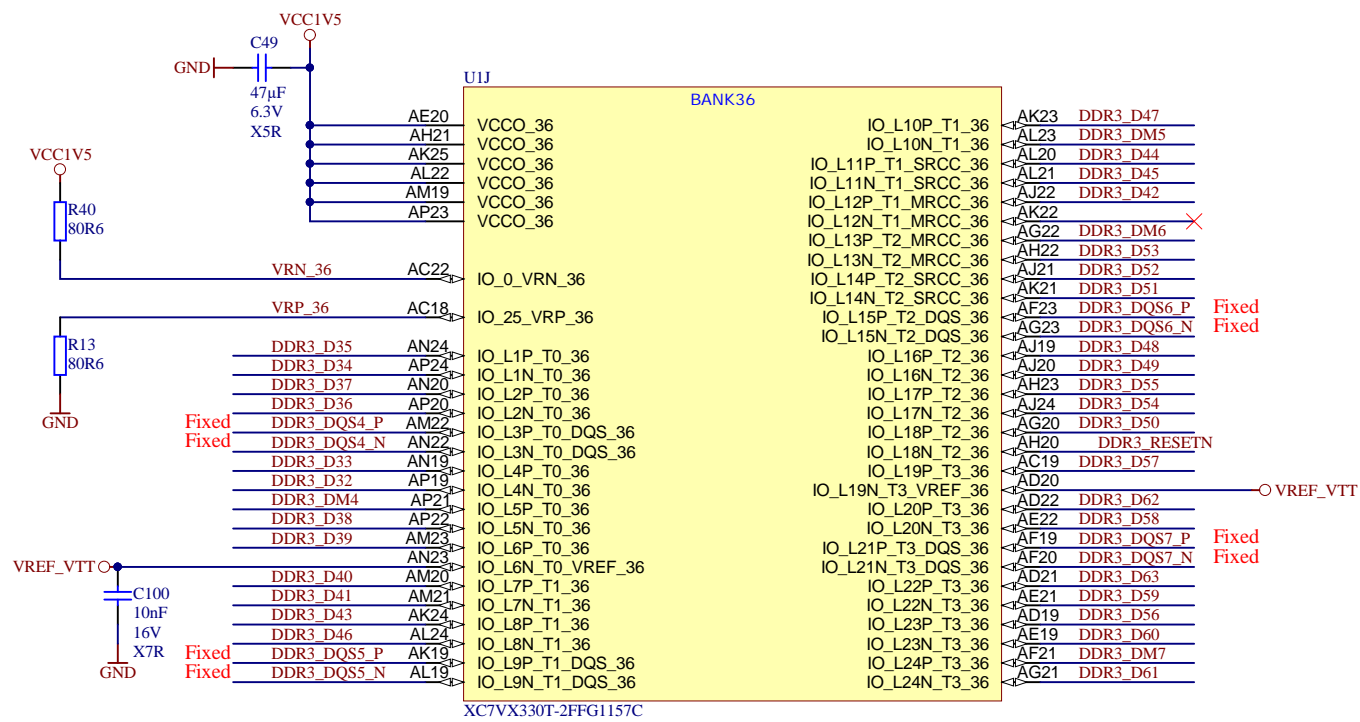
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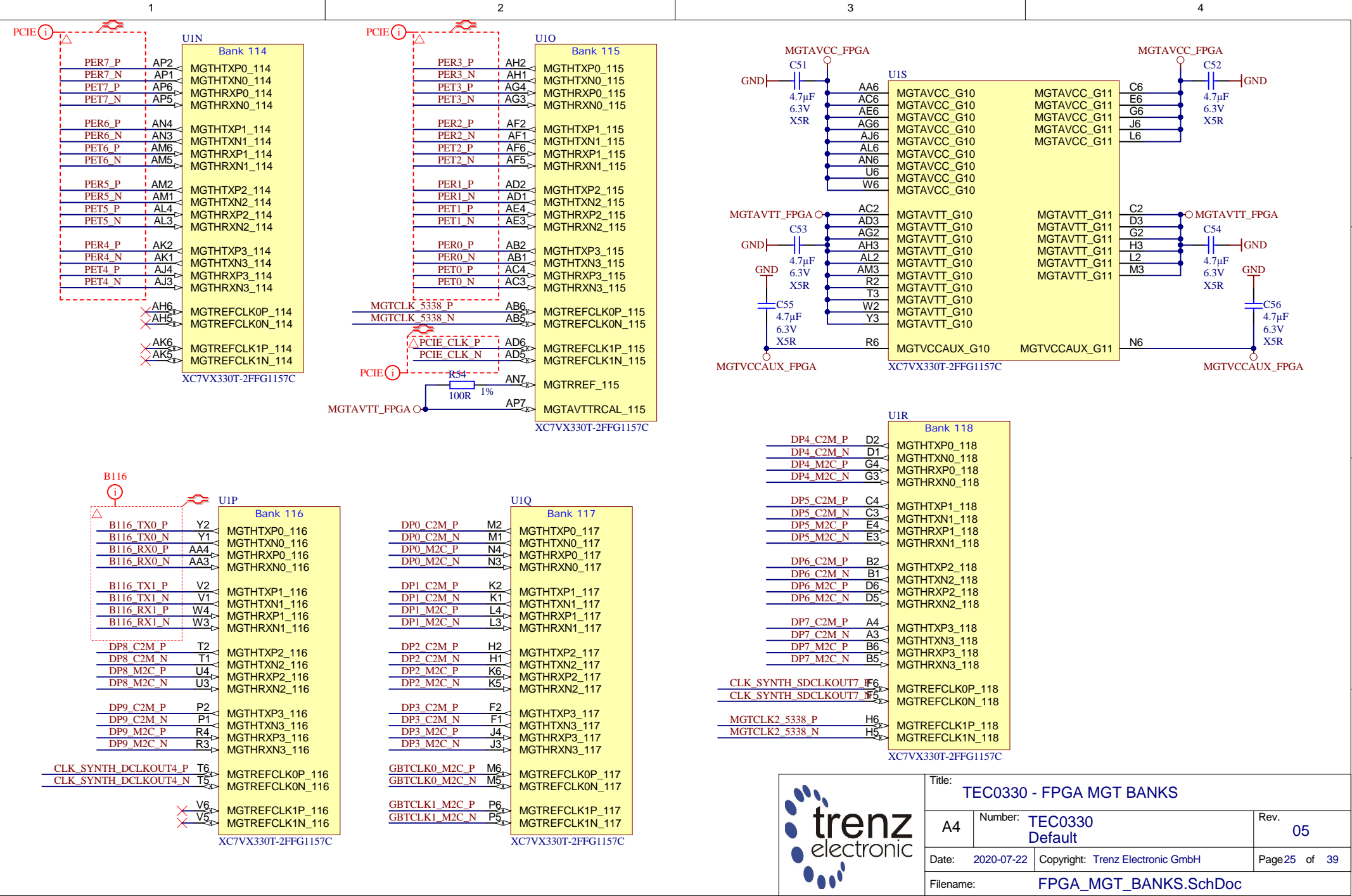
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	Title: TEC0330 - FPGA B35		
	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 23 of 39
	Filename: FPGA_BANK_35.SchDoc		



Title: TEC0330 - FPGA B36		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 24 of 39
Filename: FPGA_BANK_36.SchDoc		



Title: TEC0330 - FPGA MGT BANKS		
A4	Number: TEC0330 Default	Rev. 05
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Filename: FPGA_MGT_BANKS.SchDoc		

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U_FPGA_BANK_19
FPGA_BANK_19.SchDoc



U_FPGA_BANK_37
FPGA_BANK_37.SchDoc



U_FPGA_BANK_38
FPGA_BANK_38.SchDoc



U_FPGA_BANK_39
FPGA_BANK_39.SchDoc



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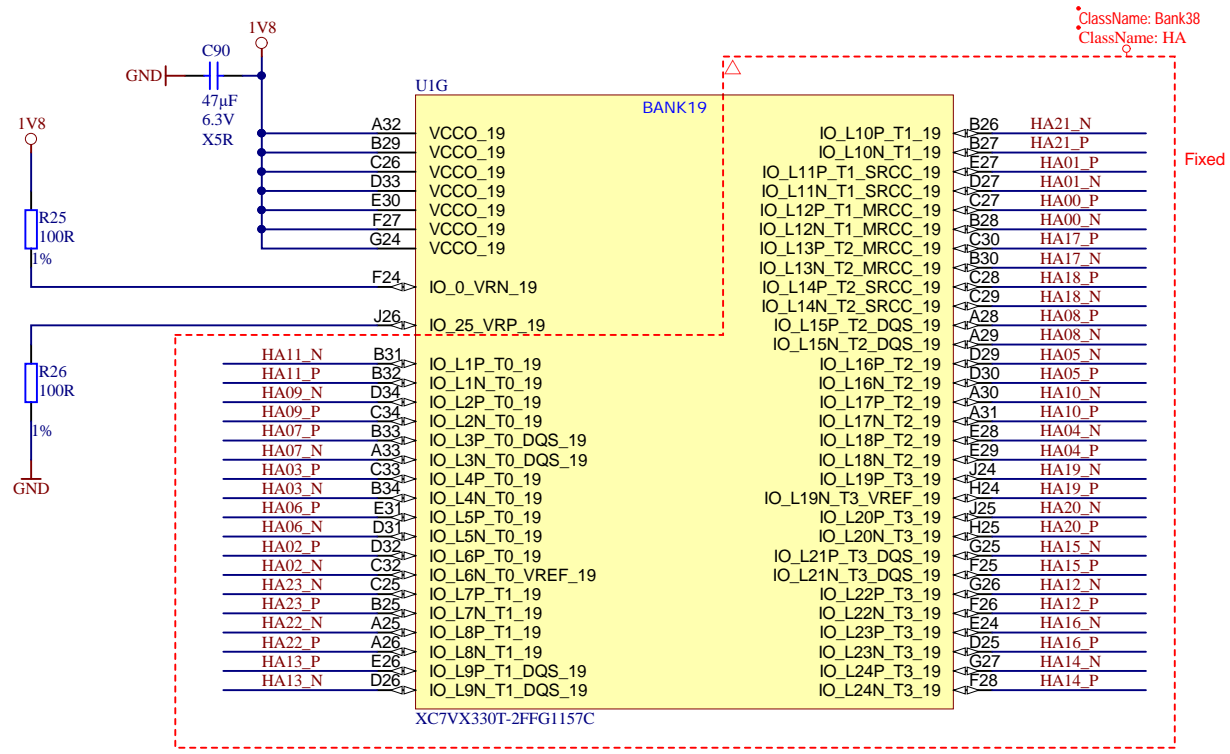
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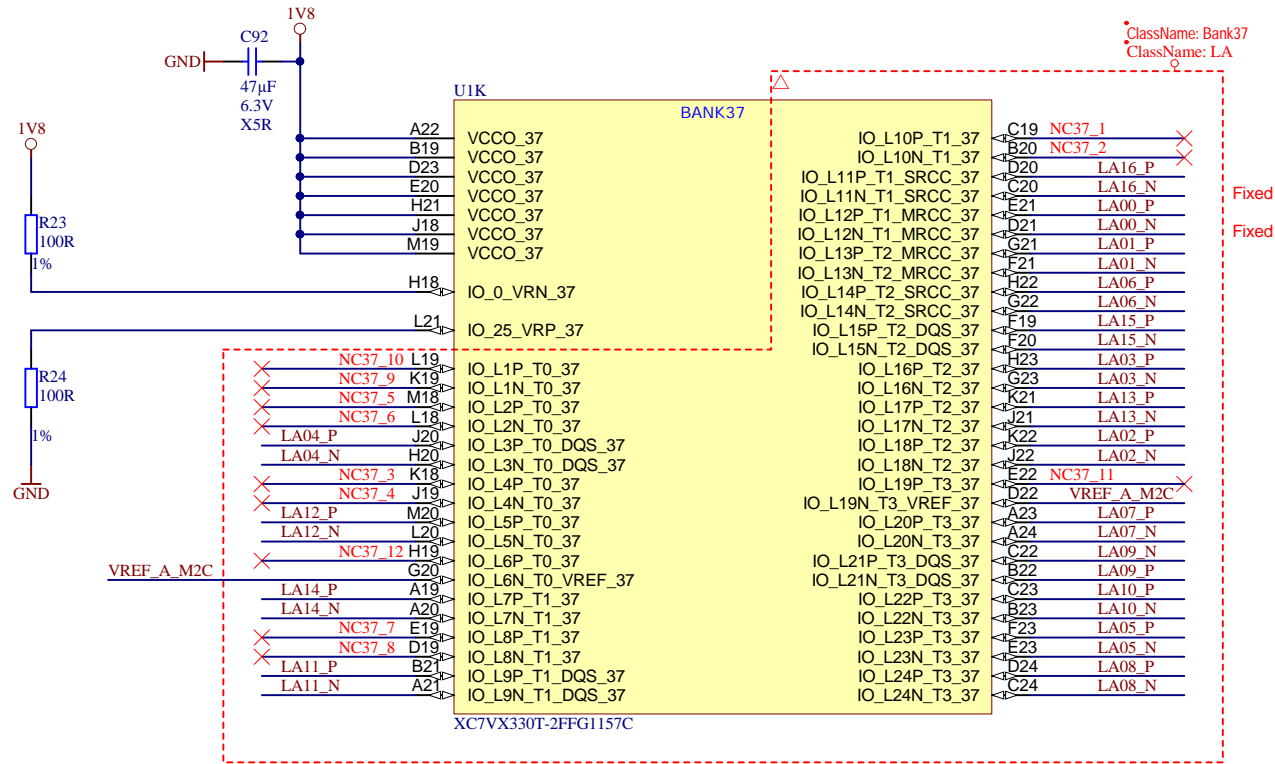
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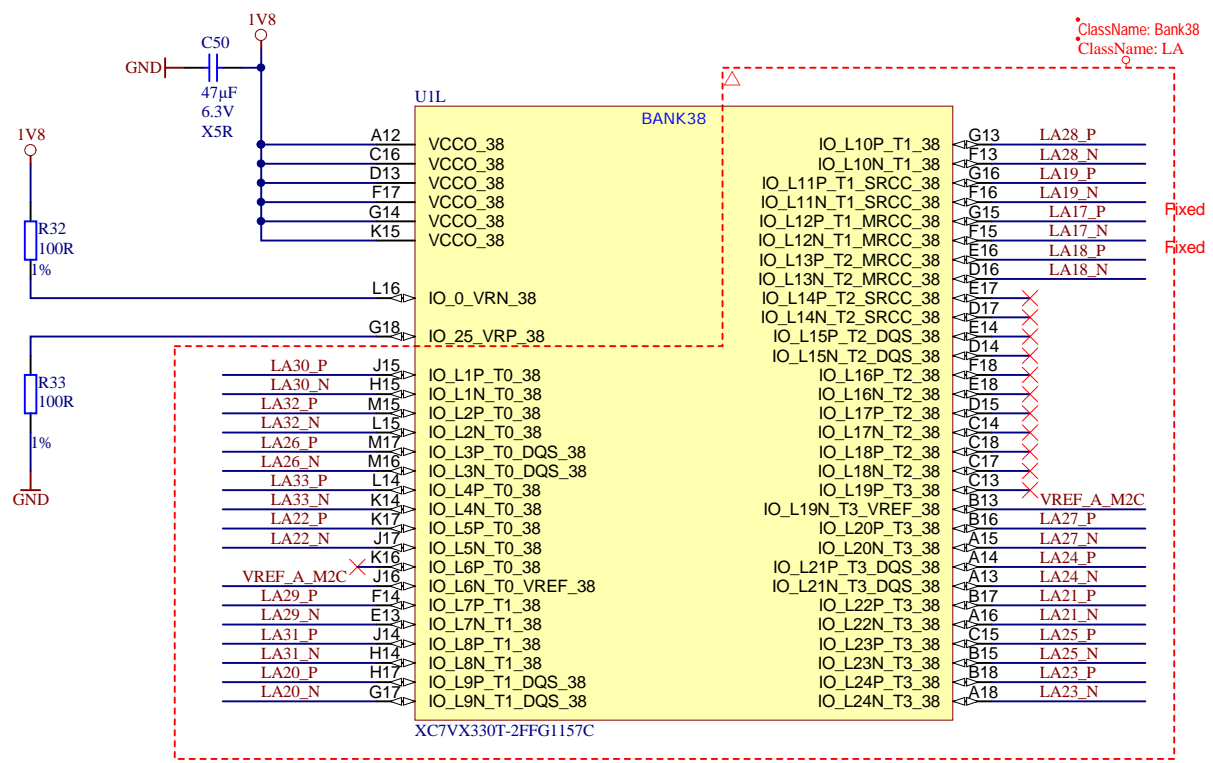
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A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 26 of 39
Filename: FMC_Banks.SchDoc		



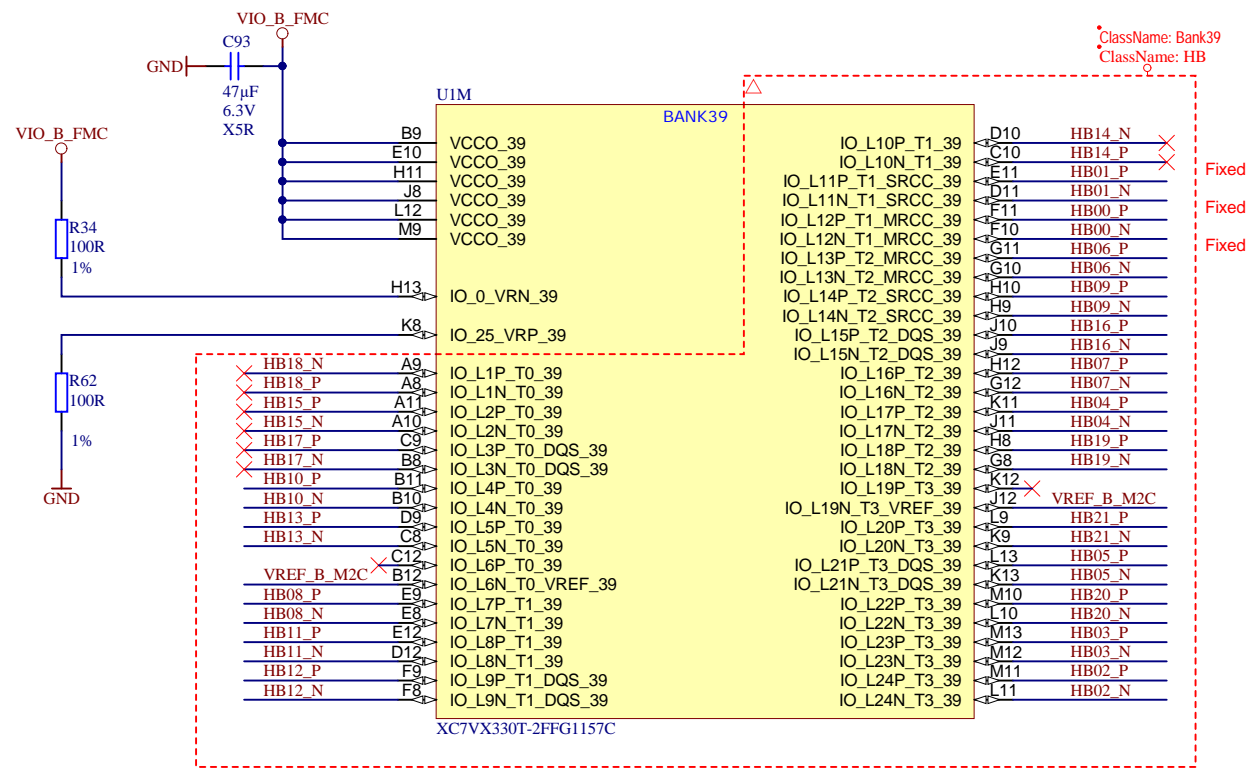
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	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 27 of 39
	Filename: FPGA_BANK_19.SchDoc		



Title: TEC0330 - FPGA B37		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 28 of 39
Filename: FPGA_BANK_37.SchDoc		



Title: TEC0330 - FPGA B38		
A4	Number: TEC0330 Default	Rev. 05
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Filename: FPGA_BANK_38.SchDoc		



Title: TEC0330 - FPGA B39		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 30 of 39
Filename: FPGA_BANK_39.SchDoc		

A

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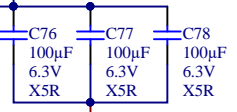
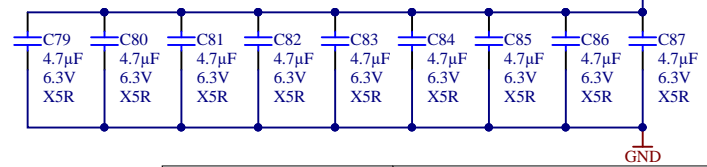
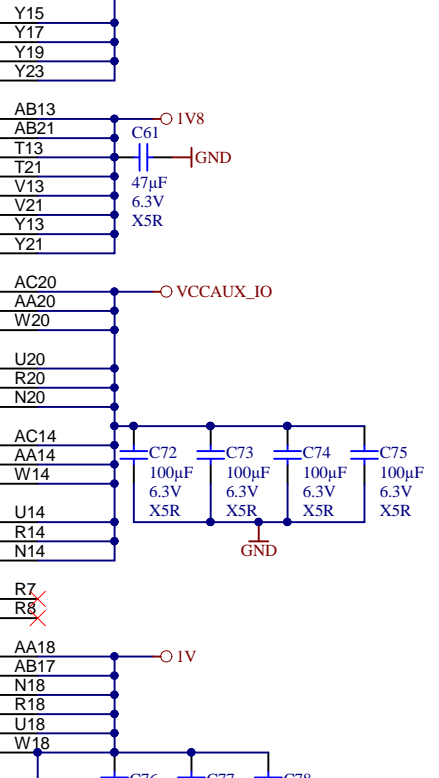
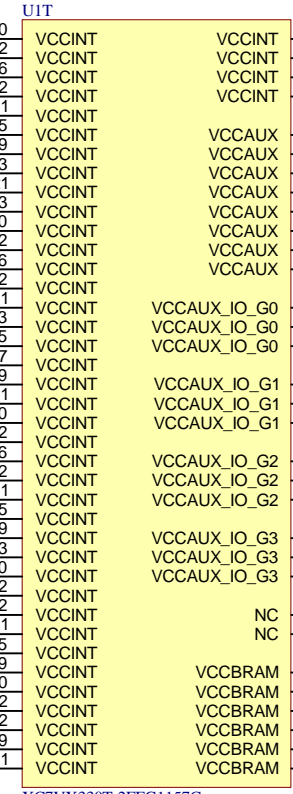
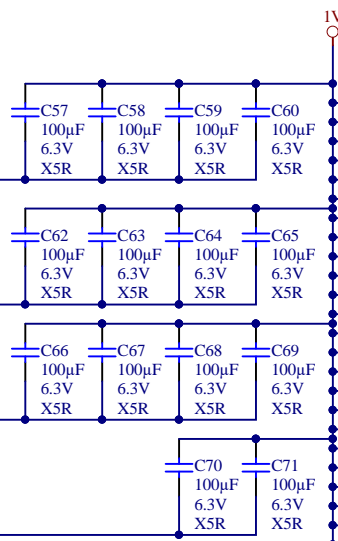
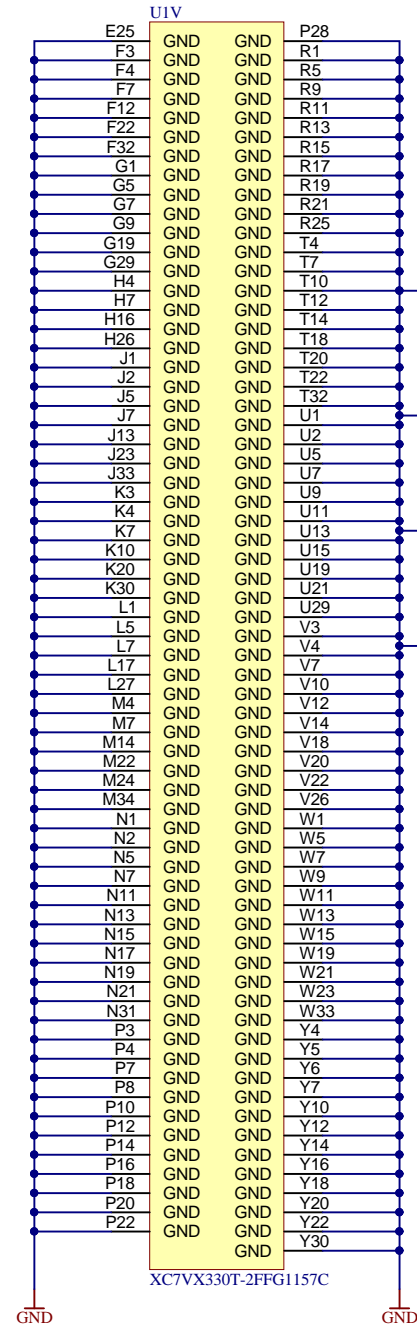
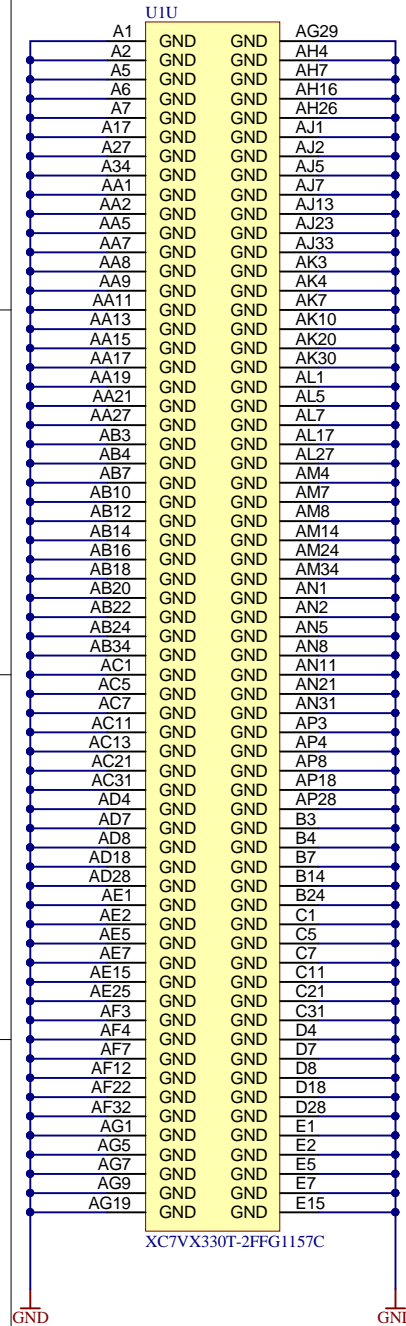
B

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Title: TEC0330 - FPGA POWER		
A4	Number: TEC0330 Default	Rev. 05
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U_PWR_4V_1V5
PWR_4V_1V5.SchDoc



U_PWR_3V3
PWR_3V3.SchDoc



U_PWR_1V
PWR_1V.SchDoc



U_PWR_MGT
PWR_MGT.SchDoc



U_PWR_1V8
PWR_1V8.SchDoc



U_PWR_5V
PWR_5V.SchDoc



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C

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D

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	Title: TEC0330 - POWER		
	A4	Number: TEC0330 Default	Rev. 05
	Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 32 of 39
	Filename: POWER.SchDoc		

A

A

B

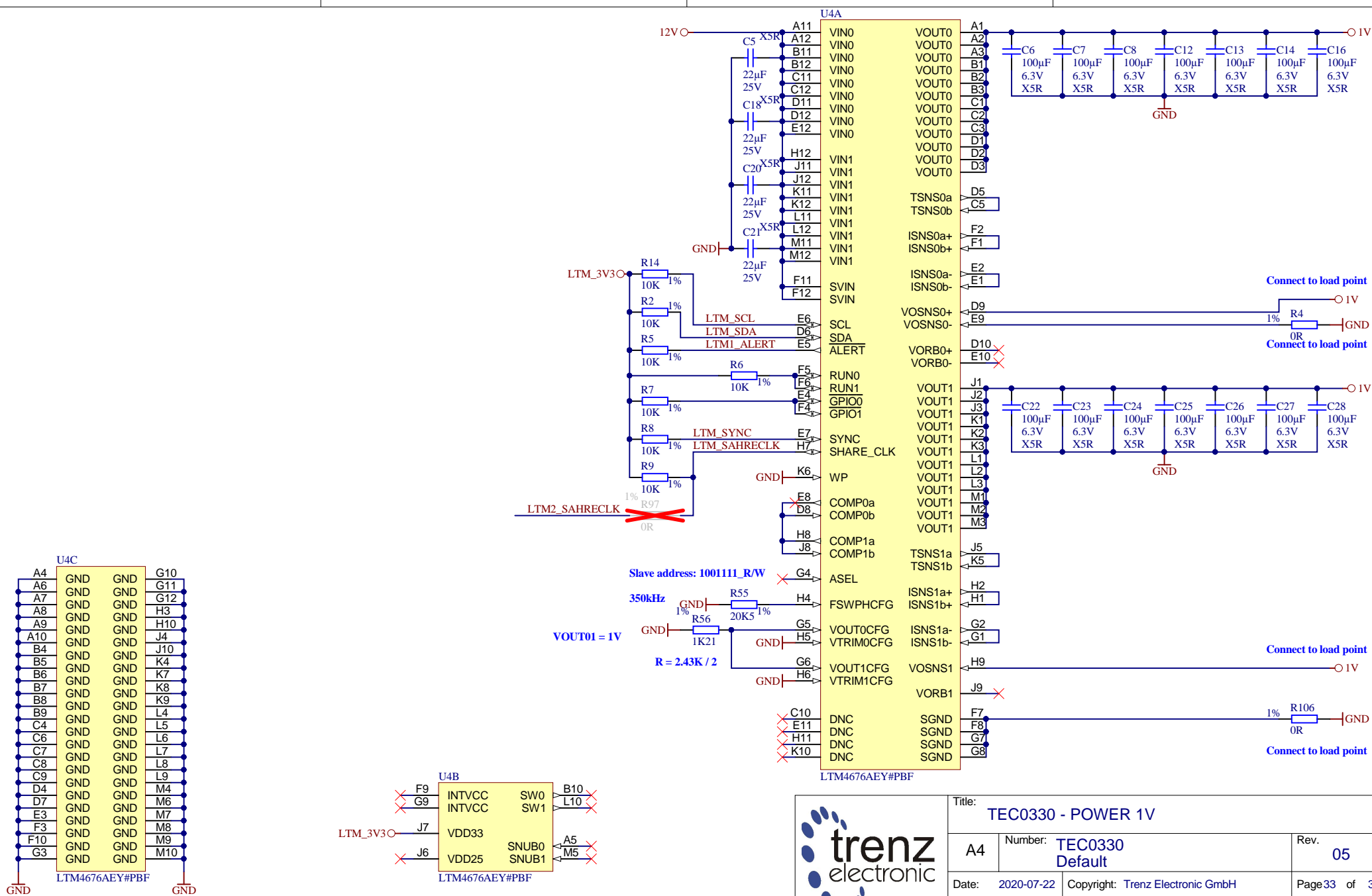
B

C

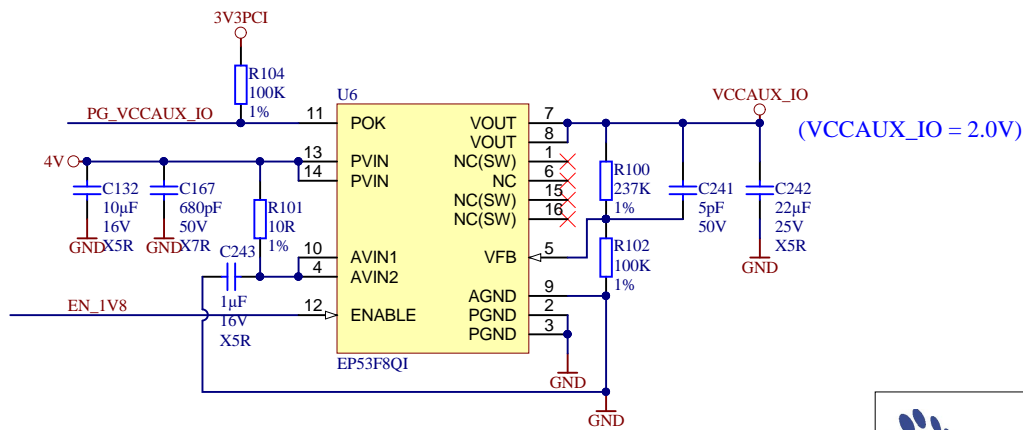
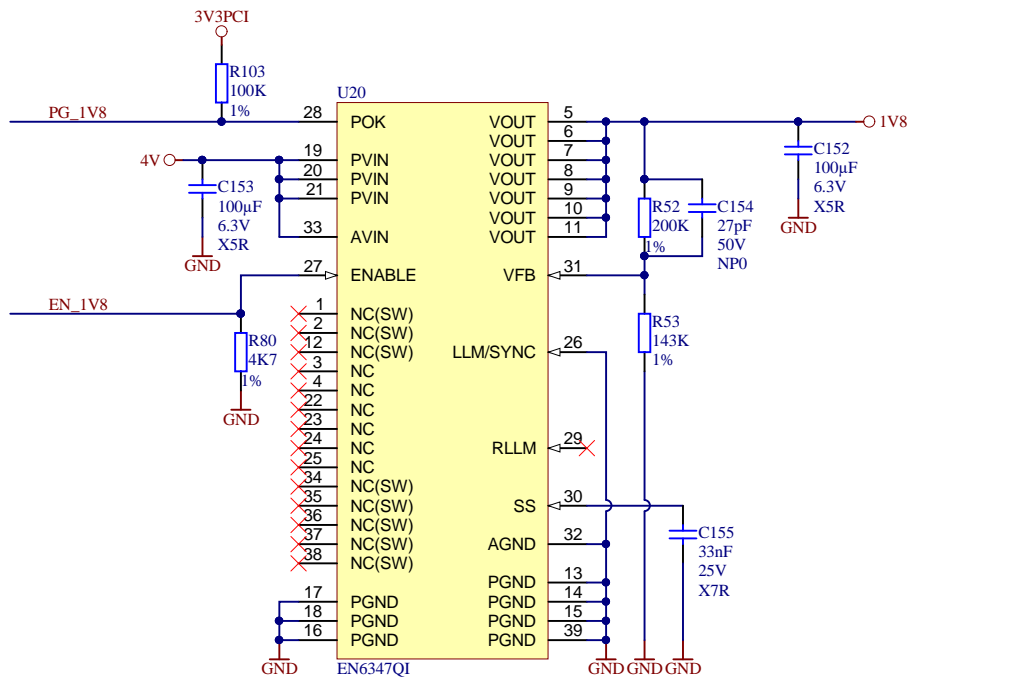
C


D

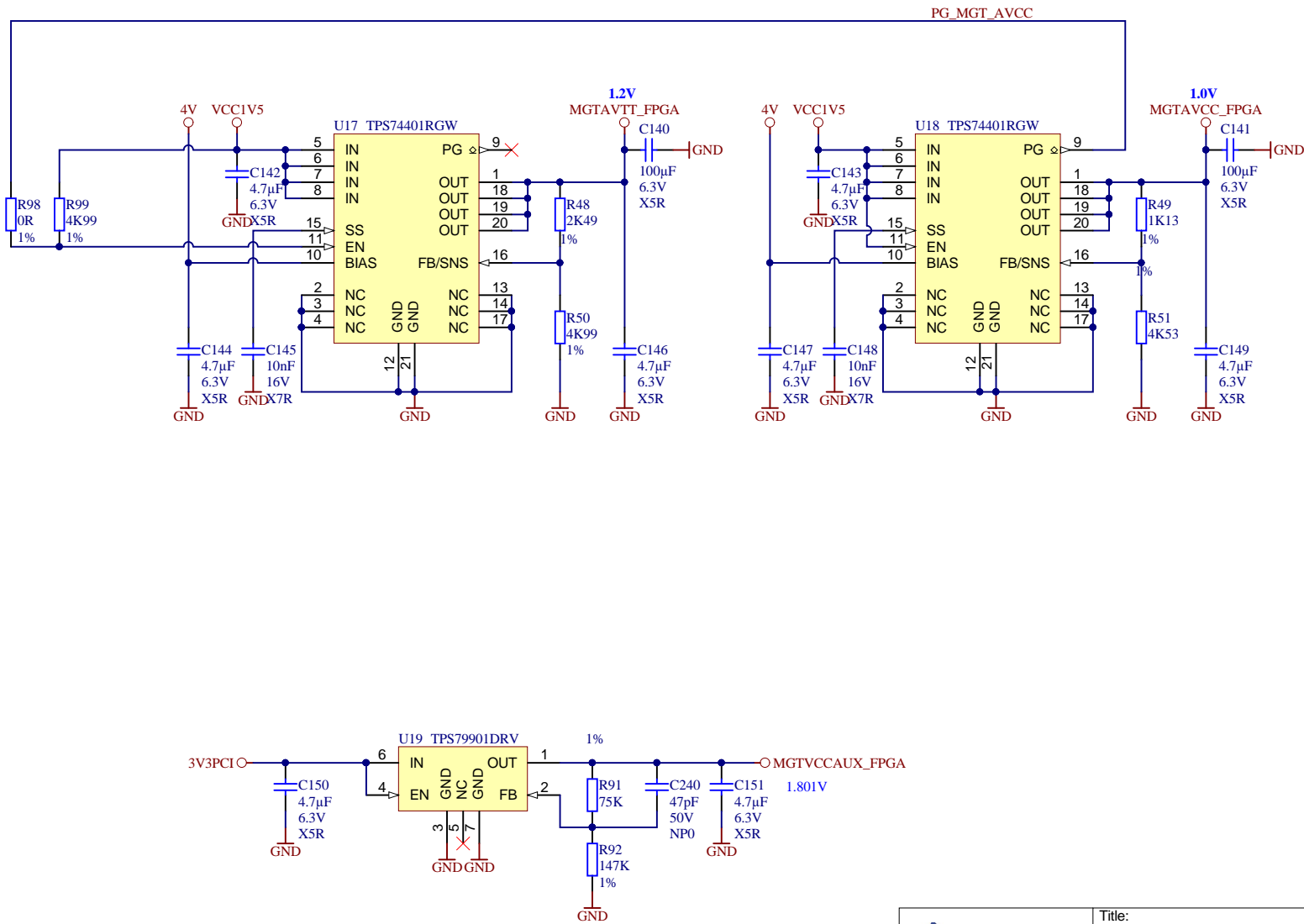
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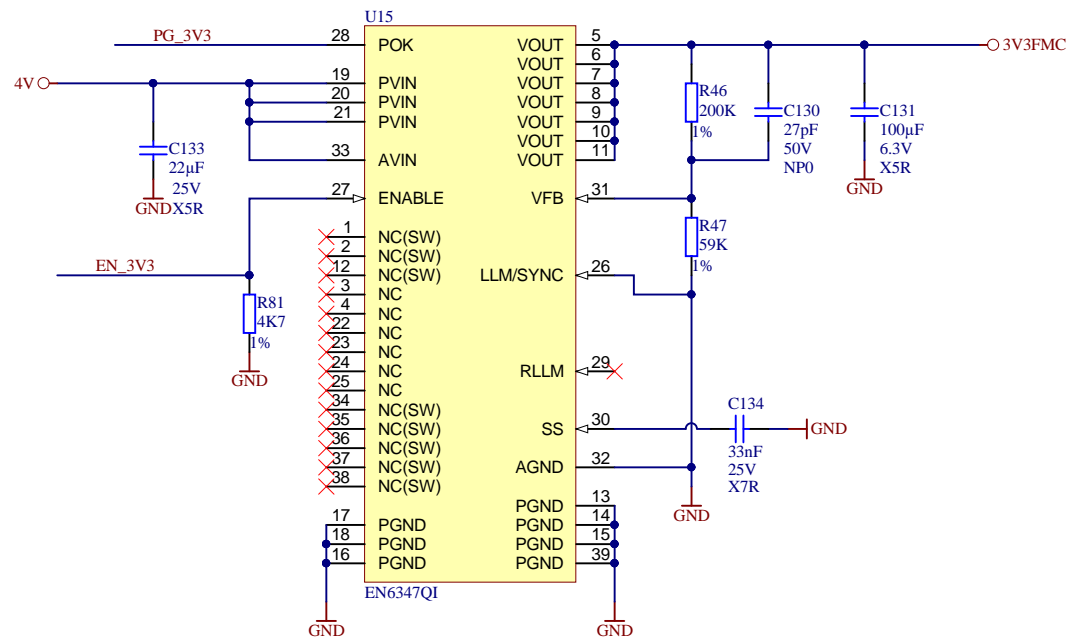
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A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 33 of 39
Filename: PWR_1V.SchDoc		




			Title: TEC0330 - POWER 1V8	
			A4	Number: TEC0330 Default
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Filename: PWR_1V8.SchDoc				



Title: TEC0330 - POWER MGT		
A4	Number: TEC0330 Default	Rev. 05
Date: 2020-07-22	Copyright: Trenz Electronic GmbH	Page 36 of 39
Filename: PWR_MGT.SchDoc		



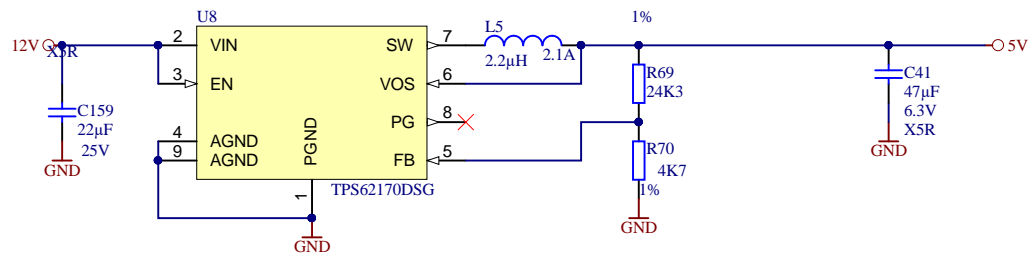
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		A4	Number: TEC0330 Default
Date: 2020-07-22		Copyright: Trenz Electronic GmbH	
Filename: PWR_3V3.SchDoc		Page 37 of 39	


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		Title: TEC0330 - POWER 5V	
		A4	Number: TEC0330 Default
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Filename: PWR_5V.SchDoc		Page 38 of 39	

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CHANGES REV04 to REV05

- 1) Replaced EOL component FMC Fan F455B-05MD -> F455B-05LD
- 2) Added AC coupling capacitors C244 .. C247
- 3) Updated hardware board revision bits (Pins AP25 .. AP27) for REV05
- 4) Full update LIB

A

A

B


B

C

C

D

D

	Title: TEC0330 - Revision Changes		
	A4	Number: TEC0330 Default	Rev. 05
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	Filename: Revision Changes.SchDoc		

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