U_FPGA
FPGA.SchDoc

U_SODIMM
SODIMM.SchDoc

U_CLOCK
CLOCK.SchDoc

U_POWER
POWER.SchDoc

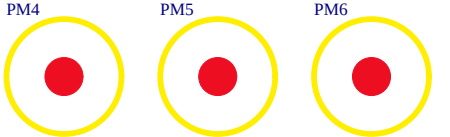
U_CONN
CONN.SchDoc

U_CPLD
CPLD.SchDoc

PM1 PM2 PM3

FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

PM4 PM5 PM6



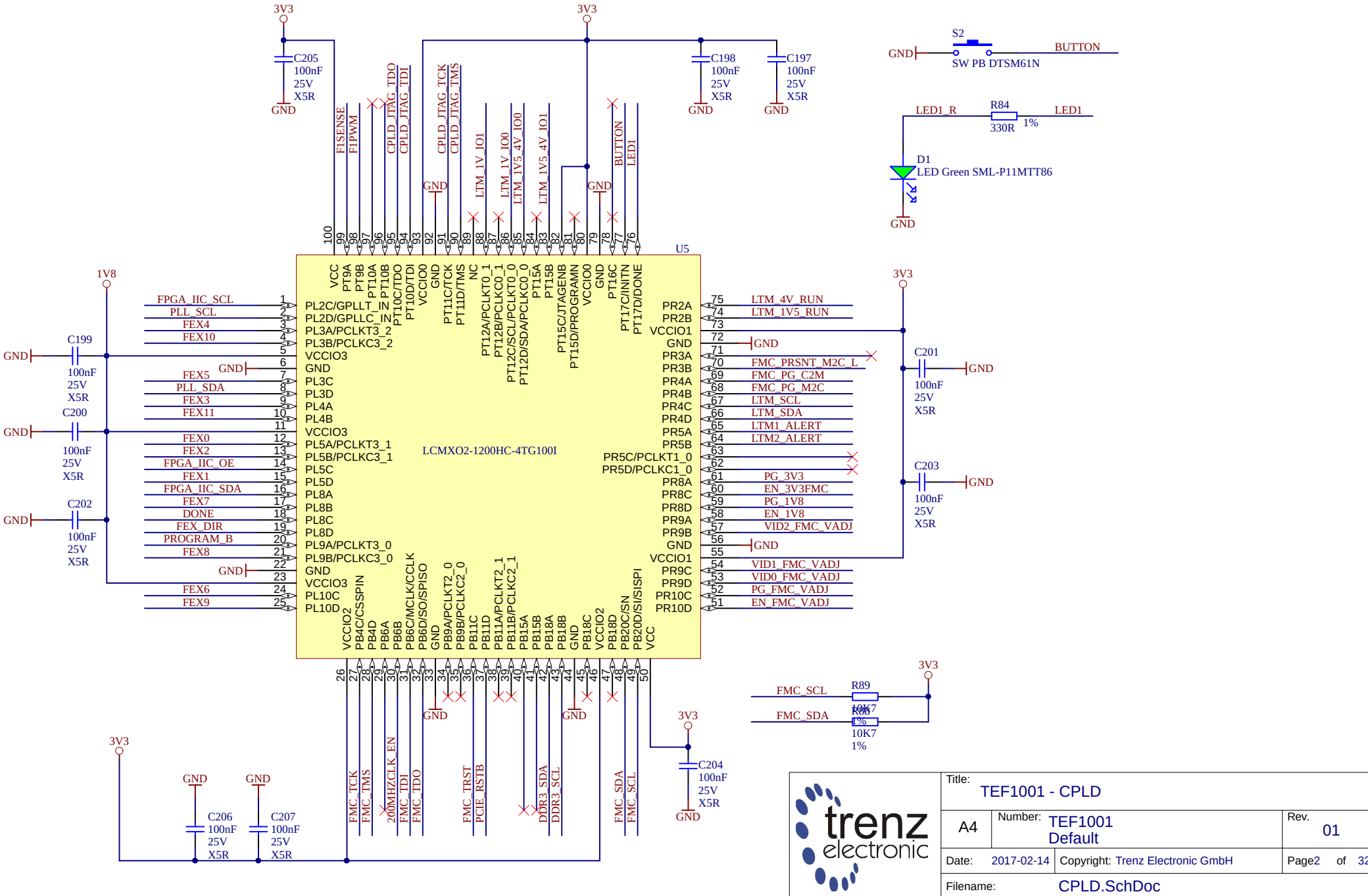
FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

Serial
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

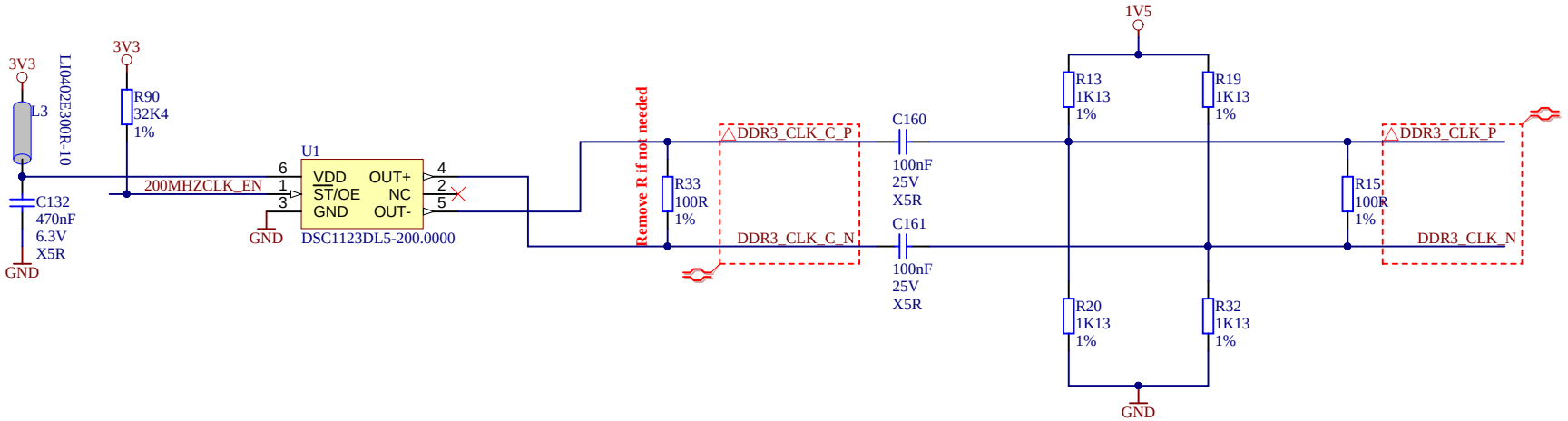
trenz electronic

Title: TEF1001 - MAIN			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page1 of 32
Filename: TEF1001.SchDoc			

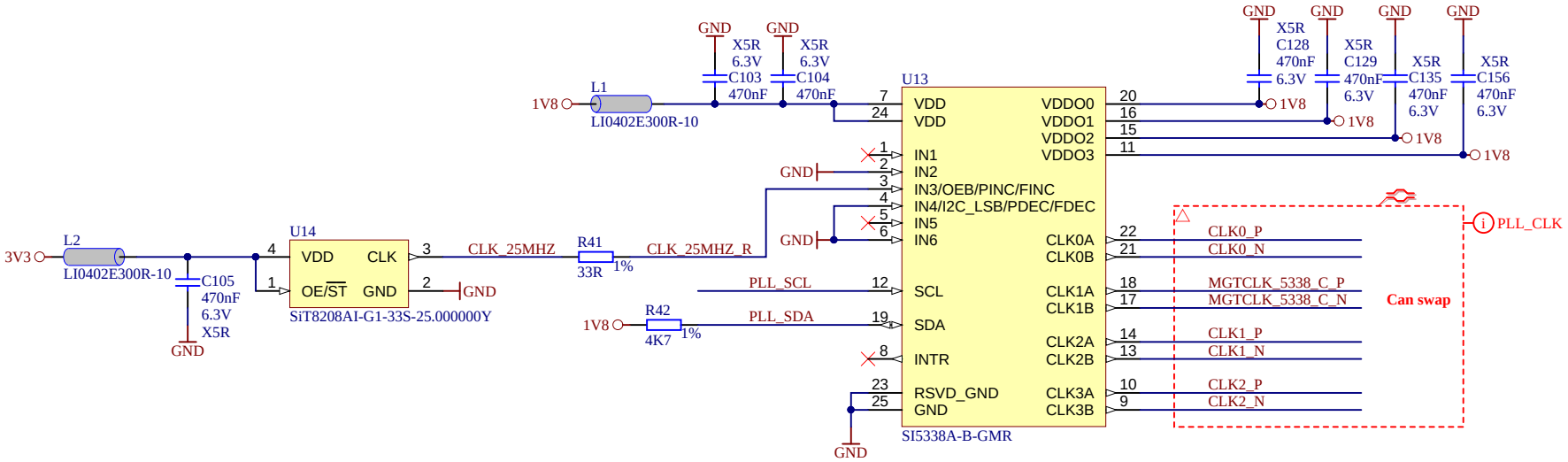


Title: TEF1001 - CPLD			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page2 of 32
Filename: CPLD.SchDoc			

U_CLK-SI5338
CLK-SI5338.SchDoc



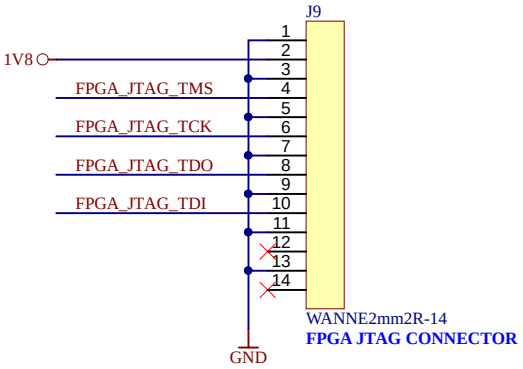
Title: TEF1001 - CLOCK			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page3 of 32
Filename: CLOCK.SchDoc			

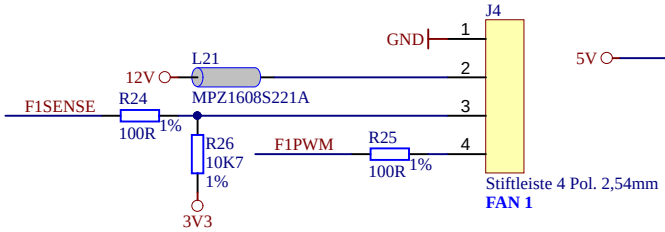


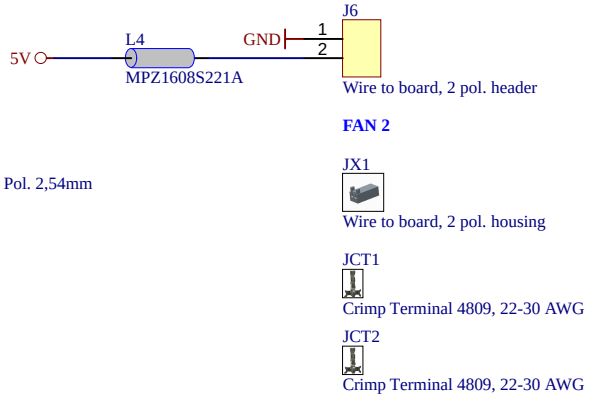
Title: TEF1001 - CLK-SI5338			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page4 of 32
Filename: CLK-SI5338.SchDoc			

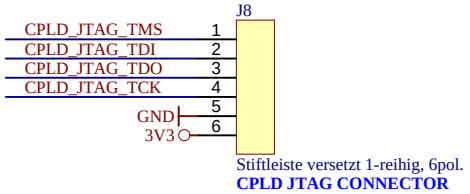
U_FMC
FMC.SchDoc

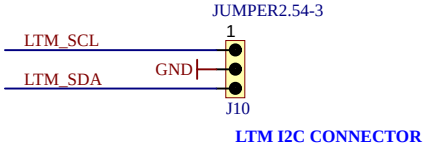
U_PCIE_CONN
PCIE_CONN.SchDoc



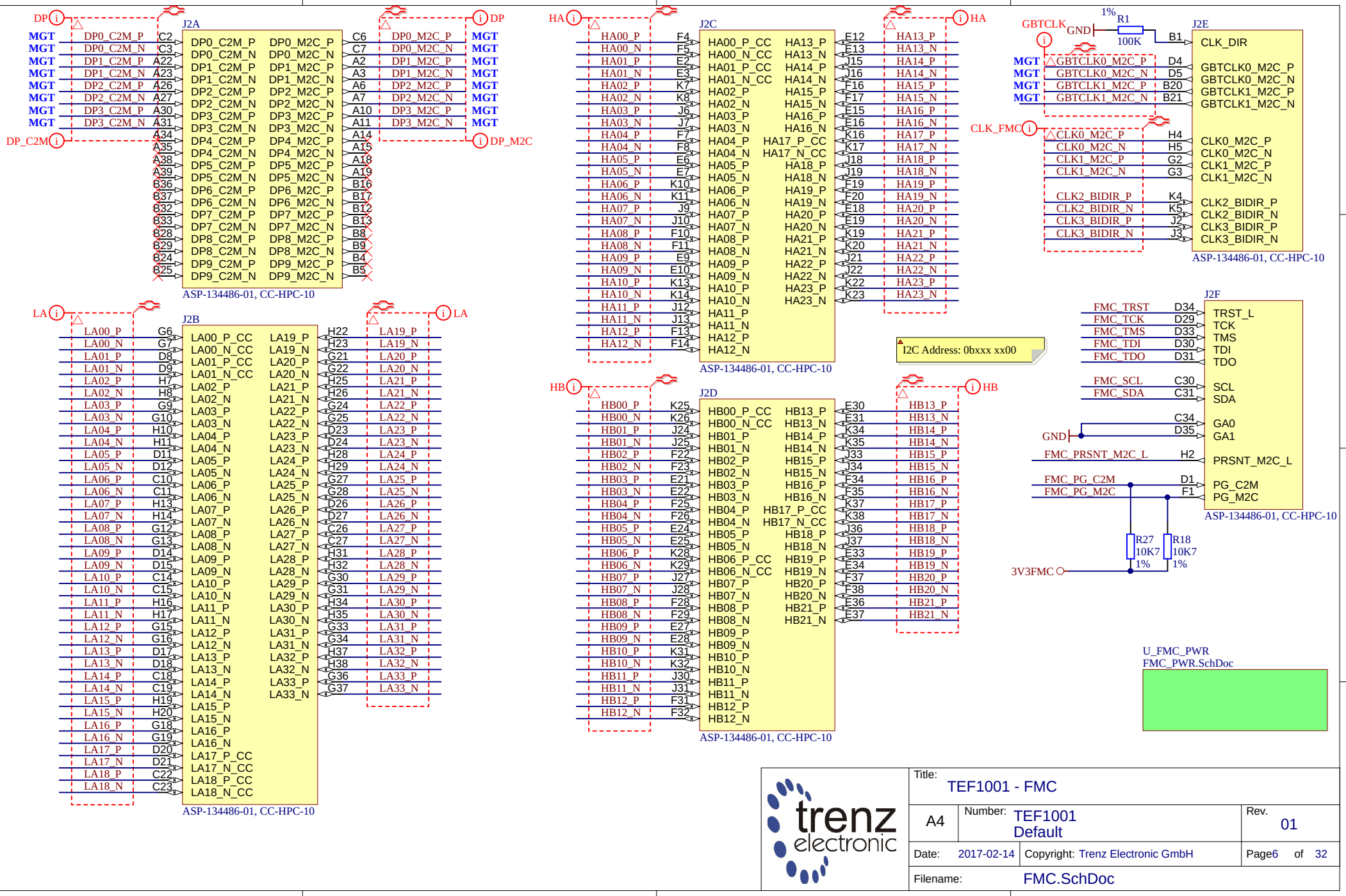


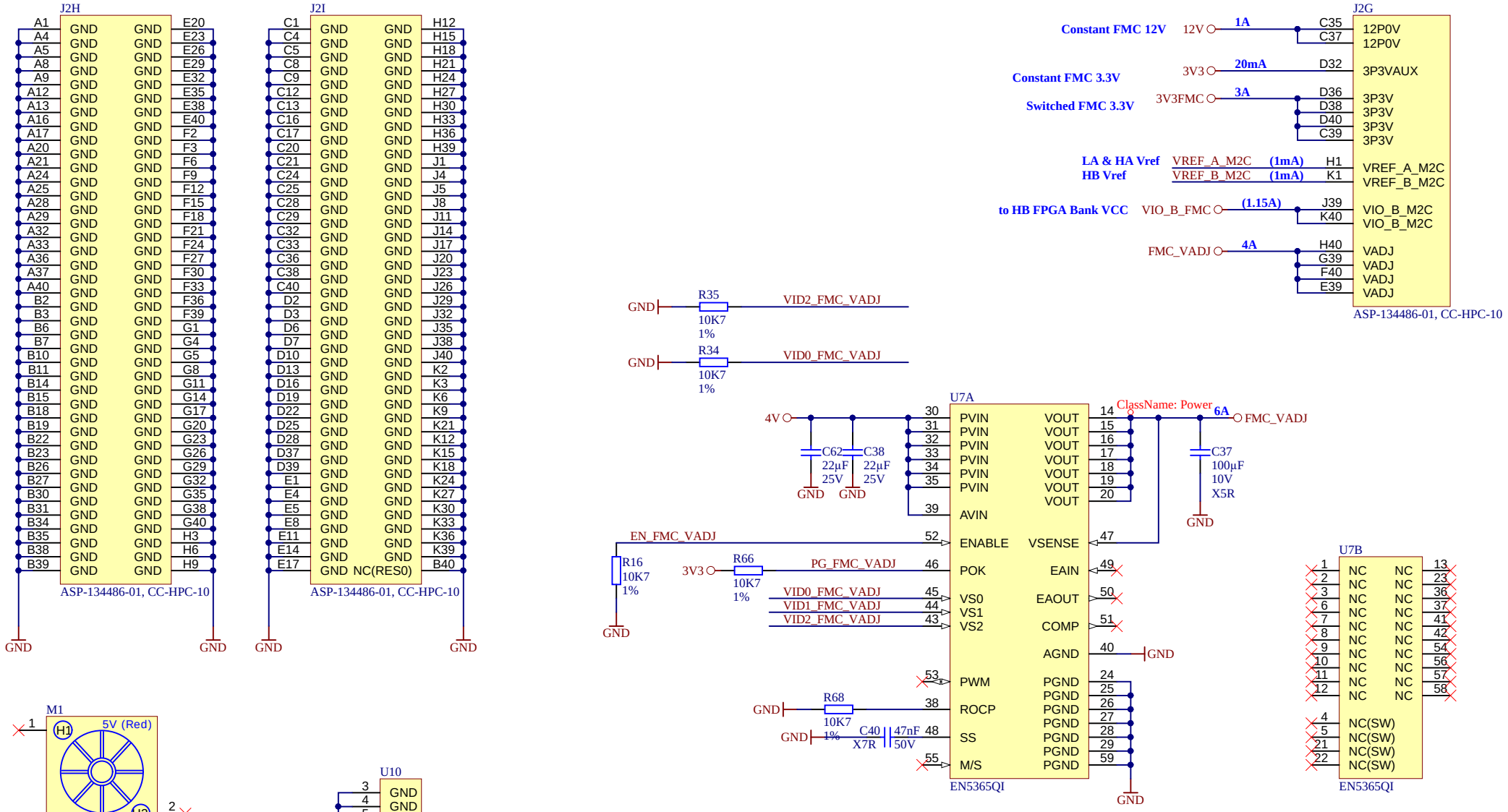


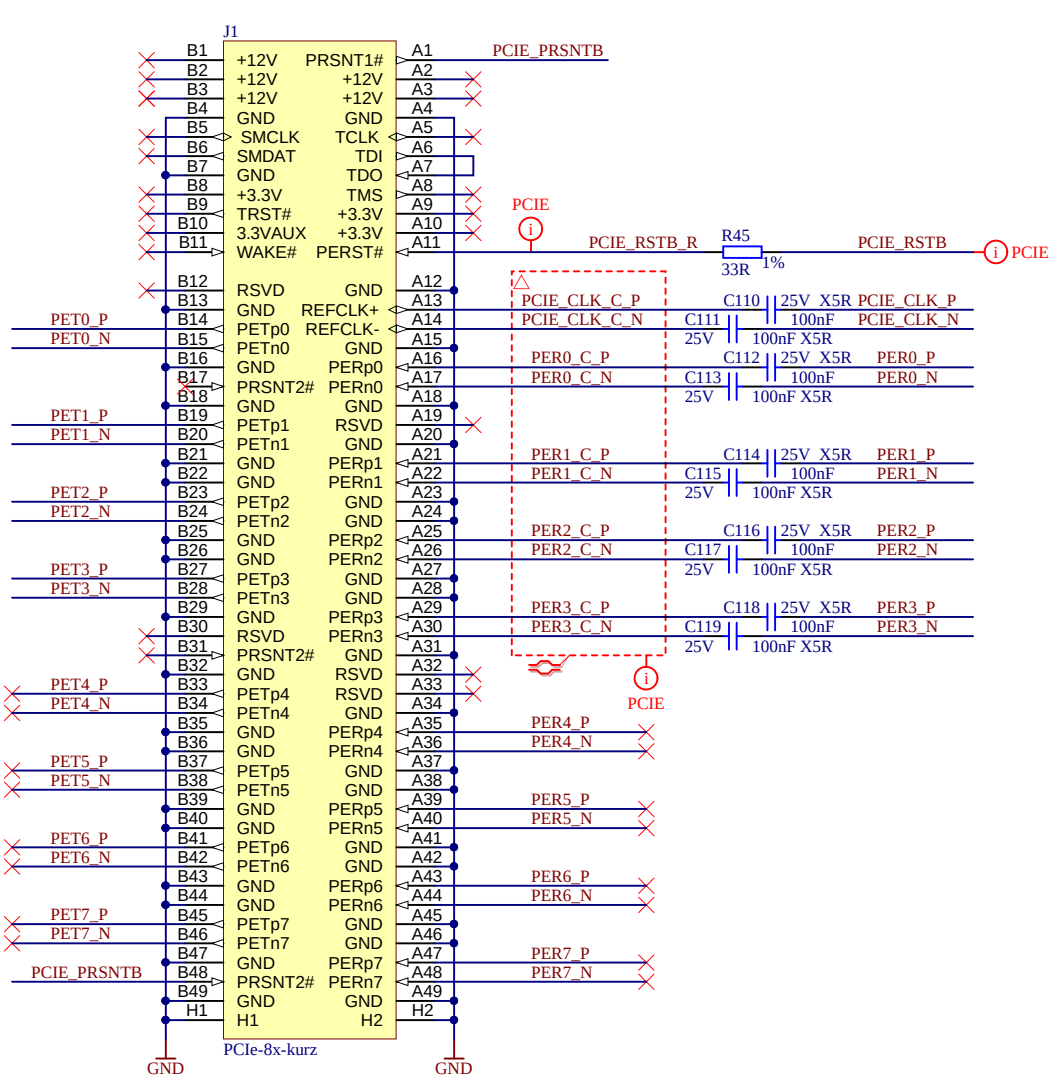


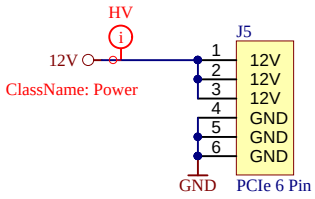


trenz electronic	Title: TEF1001 - CONN		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page5 of 32
Filename: CONN.SchDoc			


J2A
ASP-134486-01, CC-HPC-10
J2B
ASP-134486-01, CC-HPC-10
J2C
ASP-134486-01, CC-HPC-10
J2D
ASP-134486-01, CC-HPC-10
J2E
ASP-134486-01, CC-HPC-10
J2F
ASP-134486-01, CC-HPC-10
I2C Address: 0bxxx xx00
U_FMC_PWR
FMC_PWR.SchDoc
trenz electronic
Title: TEF1001 - FMC
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
Copyright: Trenz Electronic GmbH
Page6 of 32
Filename: FMC.SchDoc


J2H
J2I
J2G
ASP-134486-01, CC-HPC-10
Constant FMC 12V
Constant FMC 3.3V
Switched FMC 3.3V
LA & HA Vref
HB Vref
to HB FPGA Bank VCC
VREF_A_M2C
VREF_B_M2C
VIO_B_M2C
VADJ
R35
R34
10K7
1%
VID2_FMC_VADJ
VID0_FMC_VADJ
U7A
EN5365QI
ClassName: Power
FMC_VADJ
C62
C38
22µF
25V
C37
100µF
10V
X5R
EN_FMC_VADJ
R16
R66
PG_FMC_VADJ
VID1_FMC_VADJ
R68
C40
47nF
50V
X7R
U7B
NC(SW)
M1
5V (Red)
GND (Black)
FAN 5VDC 45X5MM .7W 1.06CFM
U10
Single FMC Con. Cooled BB Snap
VS2 | VS1 | VS0 | Output Voltage
0 | 0 | 0 | 3.3V
0 | 0 | 1 | 2.5V
0 | 1 | 0 | 1.8V
0 | 1 | 1 | 1.5V
1 | 0 | 0 | 1.25V
1 | 0 | 1 | 1.2V
trenz electronic
Title: TEF1001 - FMC_PWR
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
Copyright: Trenz Electronic GmbH
Page7 of 32
Filename: FMC_PWR.SchDoc





Title: TEF1001 - PCIE CONNECTOR			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page 8 of 32
Filename: PCIE_CONN.SchDoc			

U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

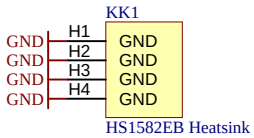
U_FPGA_BANK_16
FPGA_BANK_16.SchDoc

U_DDR_Banks
DDR_Banks.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

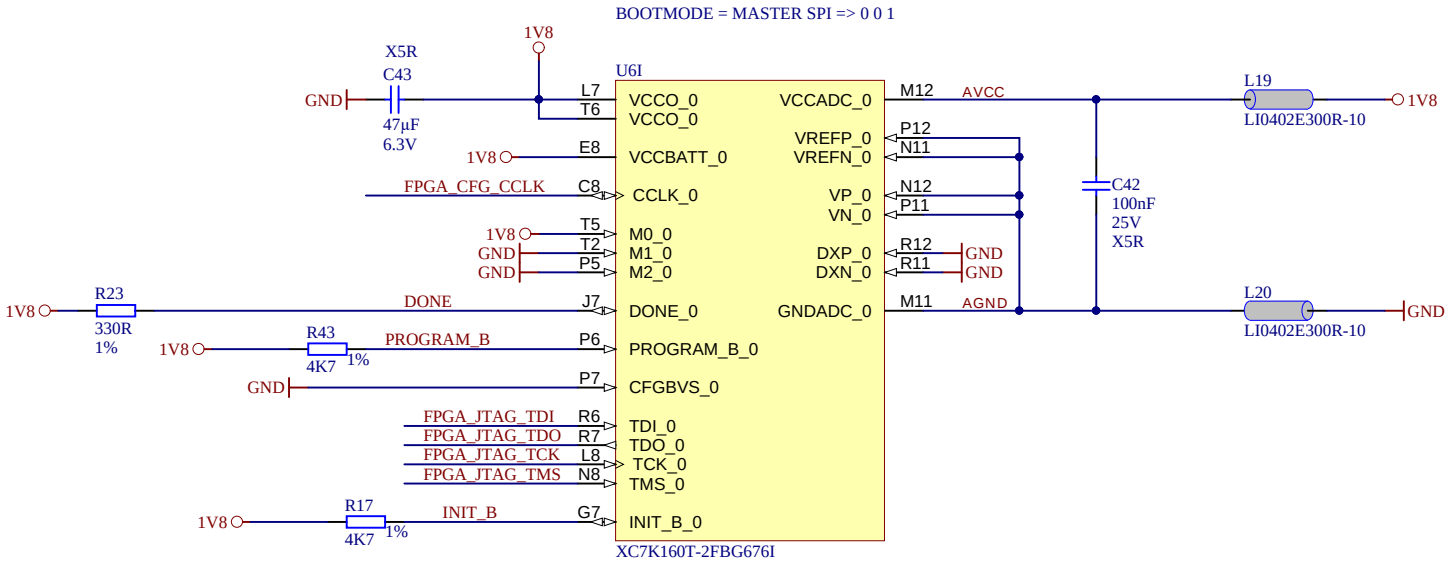
U_FPGA_CFG
FPGA_CFG.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

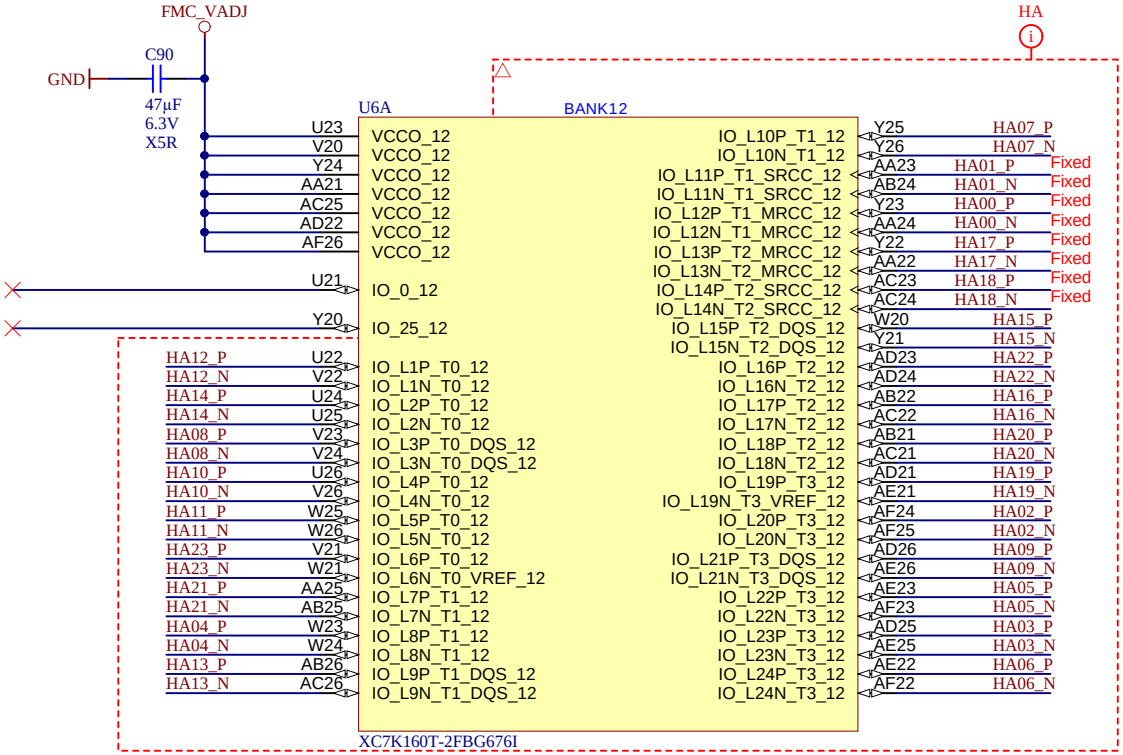


HS1582EB Heatsink

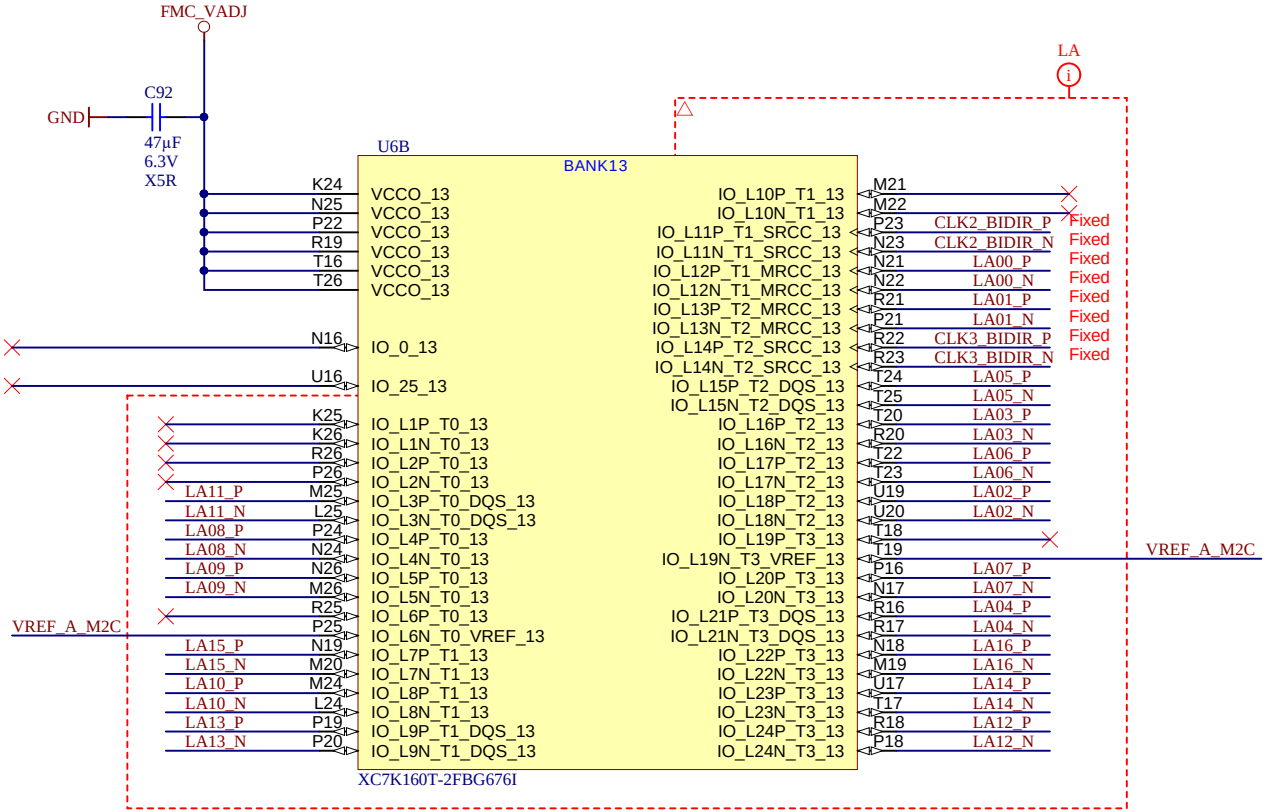
trenz electronic	Title: TEF1001 - FPGA		
	A4	Number: TEF1001 Default	Rev. 01
	Date: 2017-02-14	Copyright: Trenz Electronic GmbH	Page9 of 32
	Filename: FPGA.SchDoc		



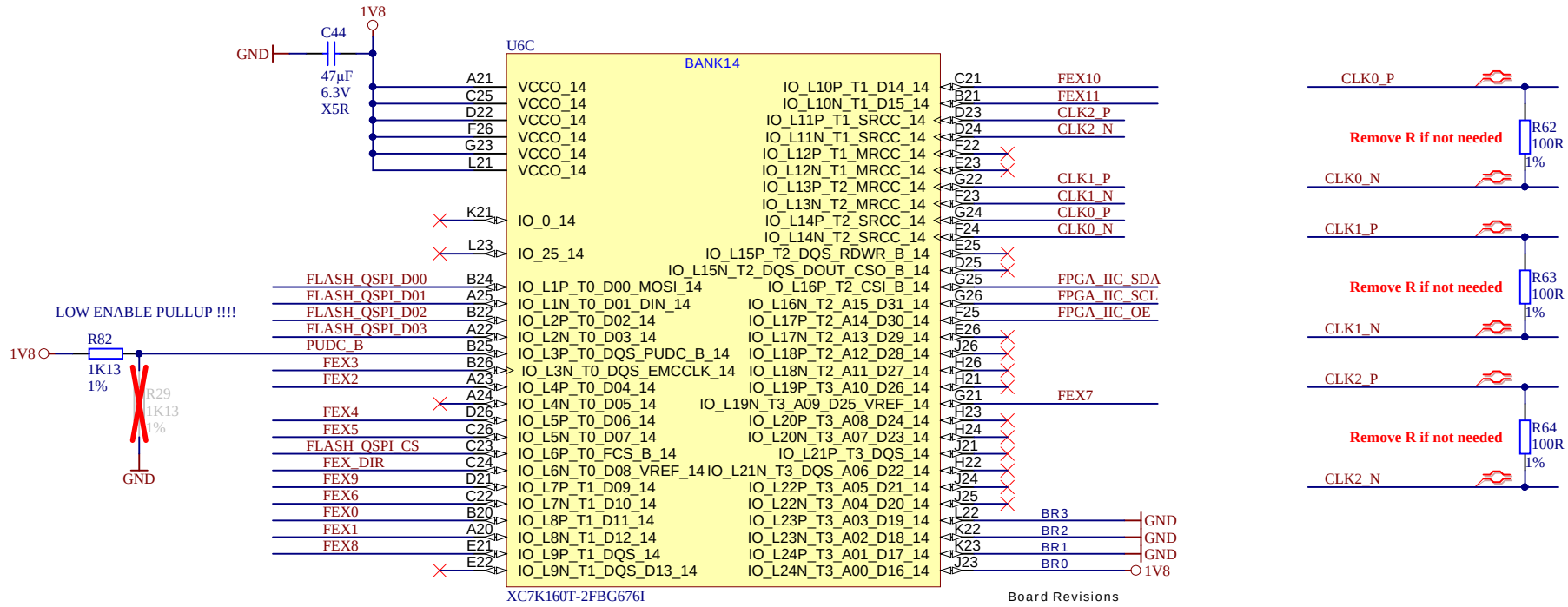
Title: TEF1001 - FPGA_CFG			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page10 of 32
Filename: FPGA_CFG.SchDoc			



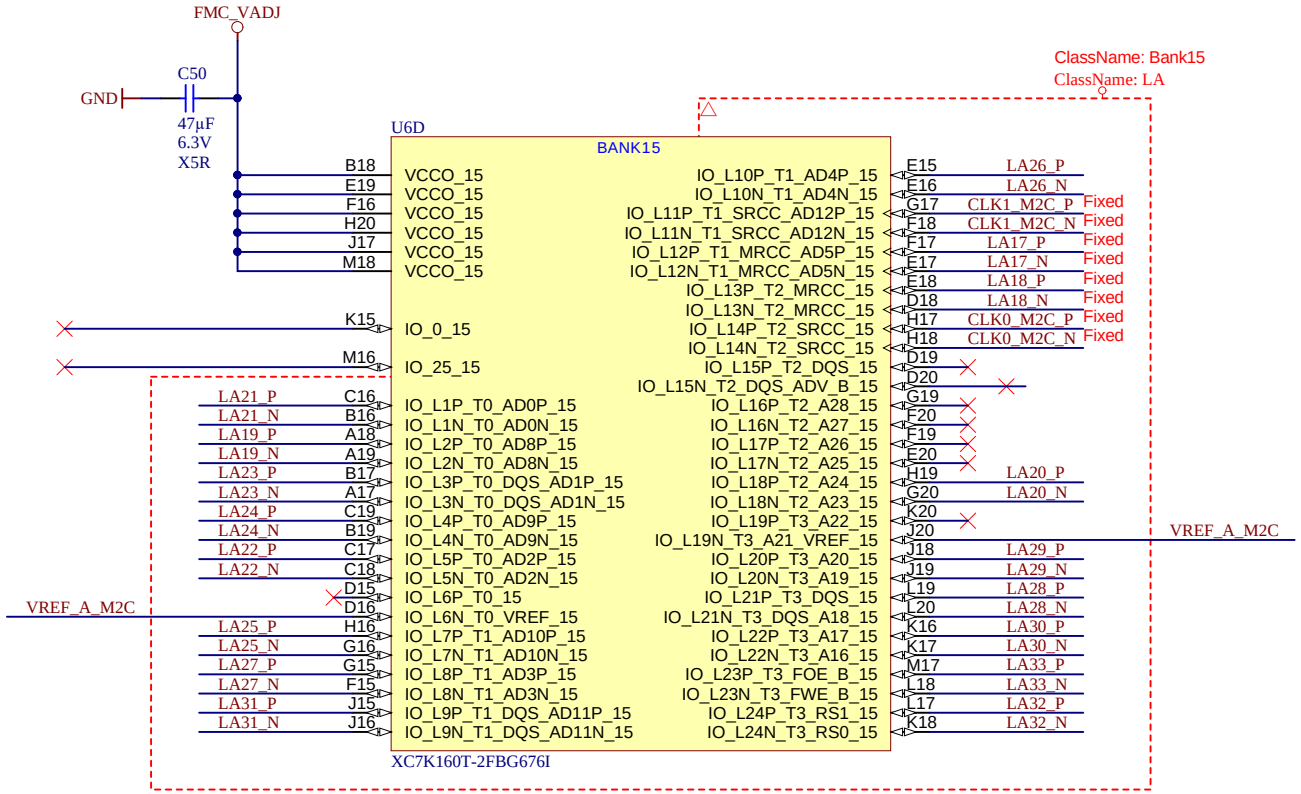
trenz electronic	Title: TEF1001 - FPGA_BANK_12		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page11 of 32
Filename: FPGA_BANK_12.SchDoc			



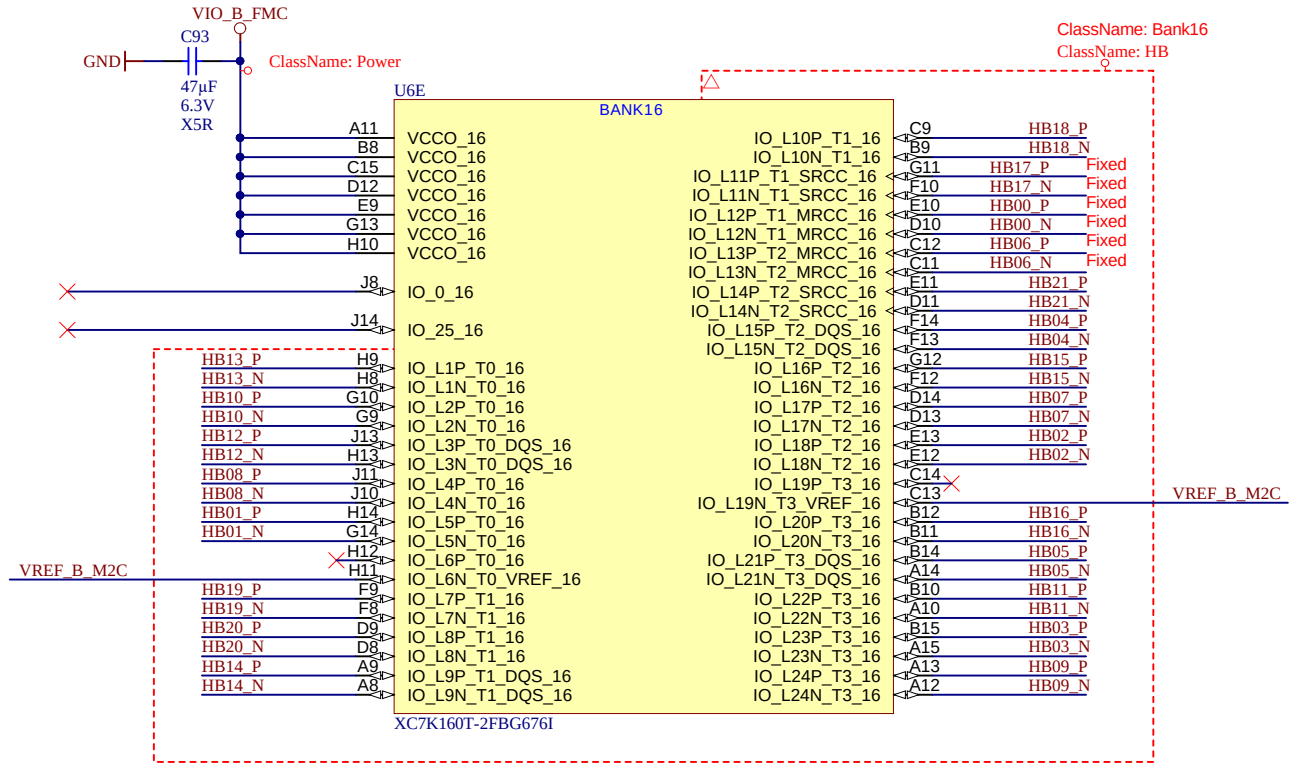
Title: TEF1001 - FPGA_BANK_13			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page12 of 32
Filename: FPGA_BANK_13.SchDoc			



trenz electronic	Title: TEF1001 - FPGA_BANK_14		
	A4	Number: TEF1001 Default	Rev. 01
	Date: 2017-02-14	Copyright: Trenz Electronic GmbH	Page13 of 32
	Filename: FPGA_BANK_14.SchDoc		

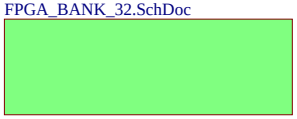


Title: TEF1001 - FPGA_BANK_15			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page14 of 32
Filename: FPGA_BANK_15.SchDoc			

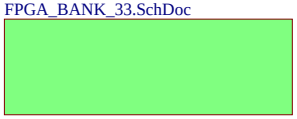


Title: TEF1001 - FPGA_BANK_16			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page15 of 32
Filename: FPGA_BANK_16.SchDoc			

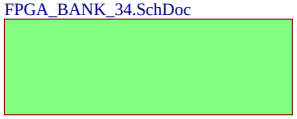
U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



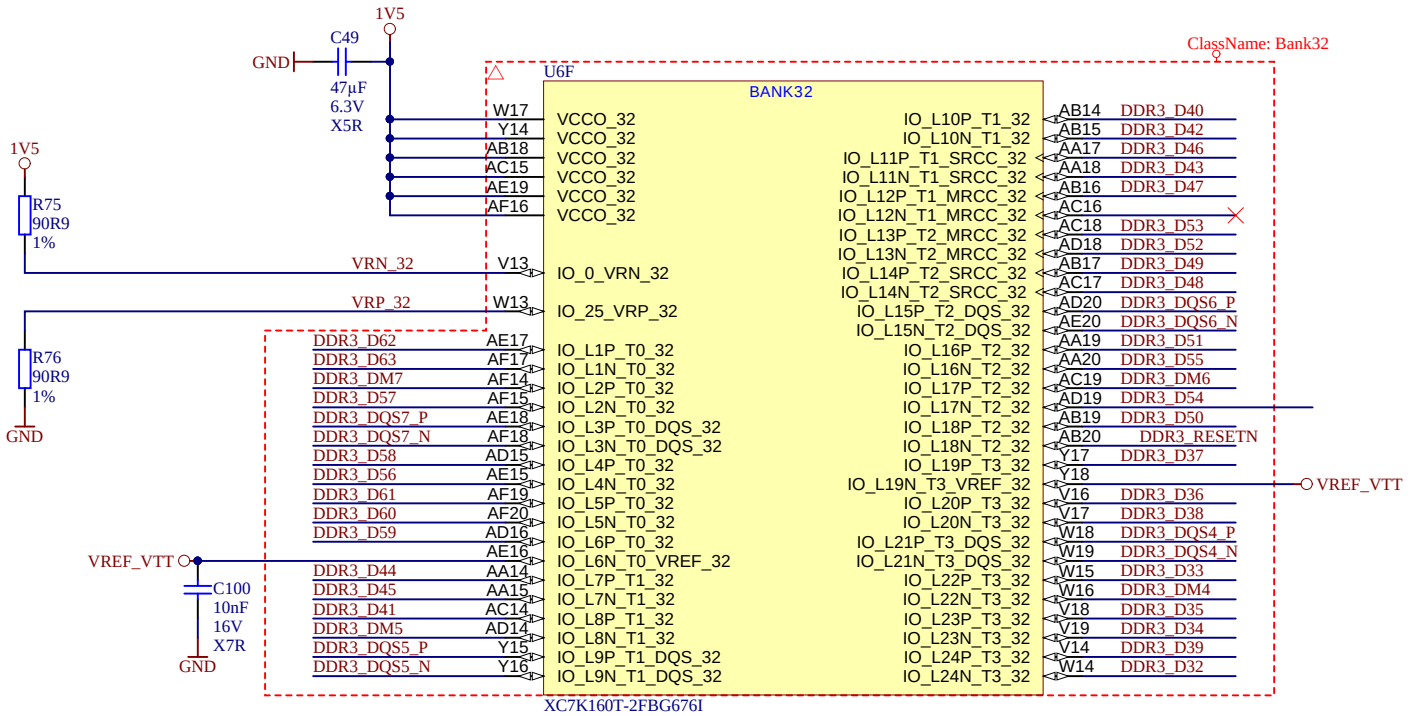
U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



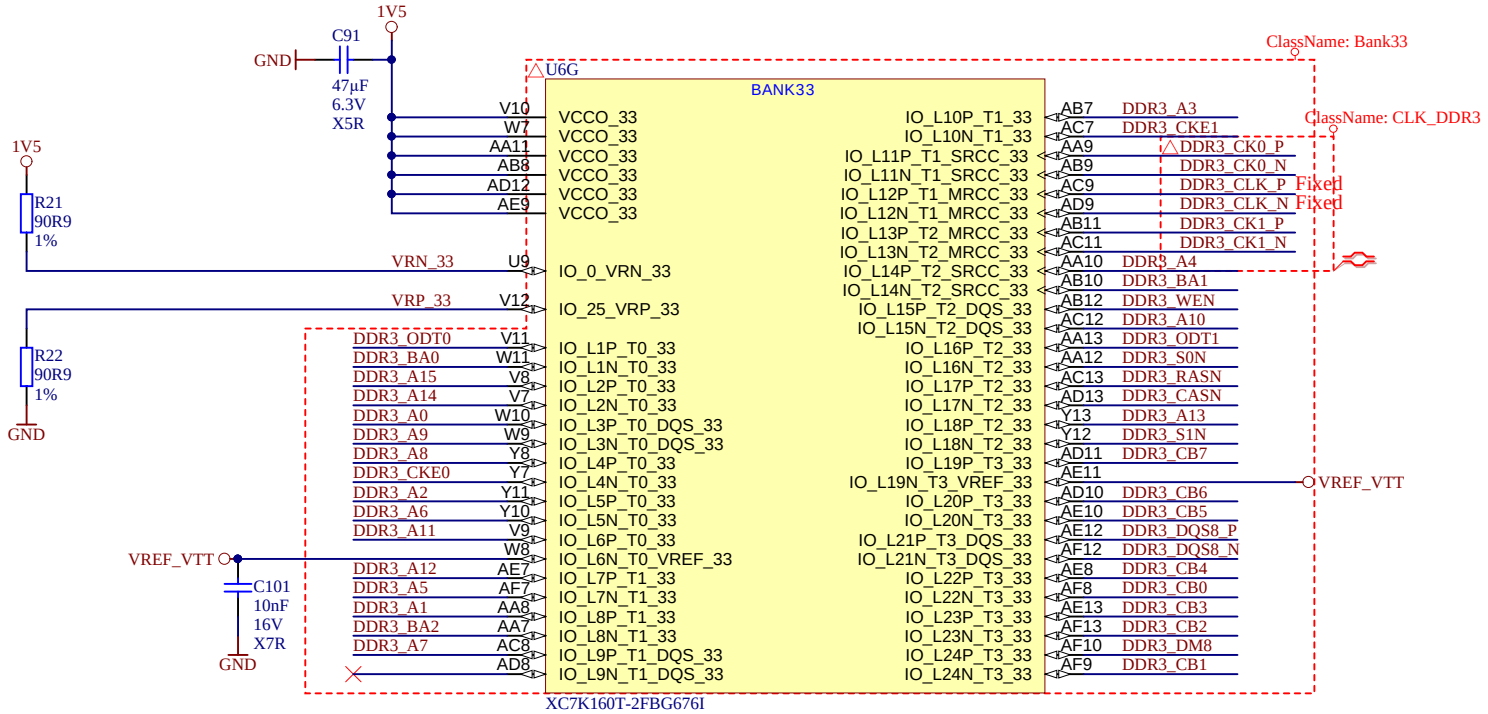
U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



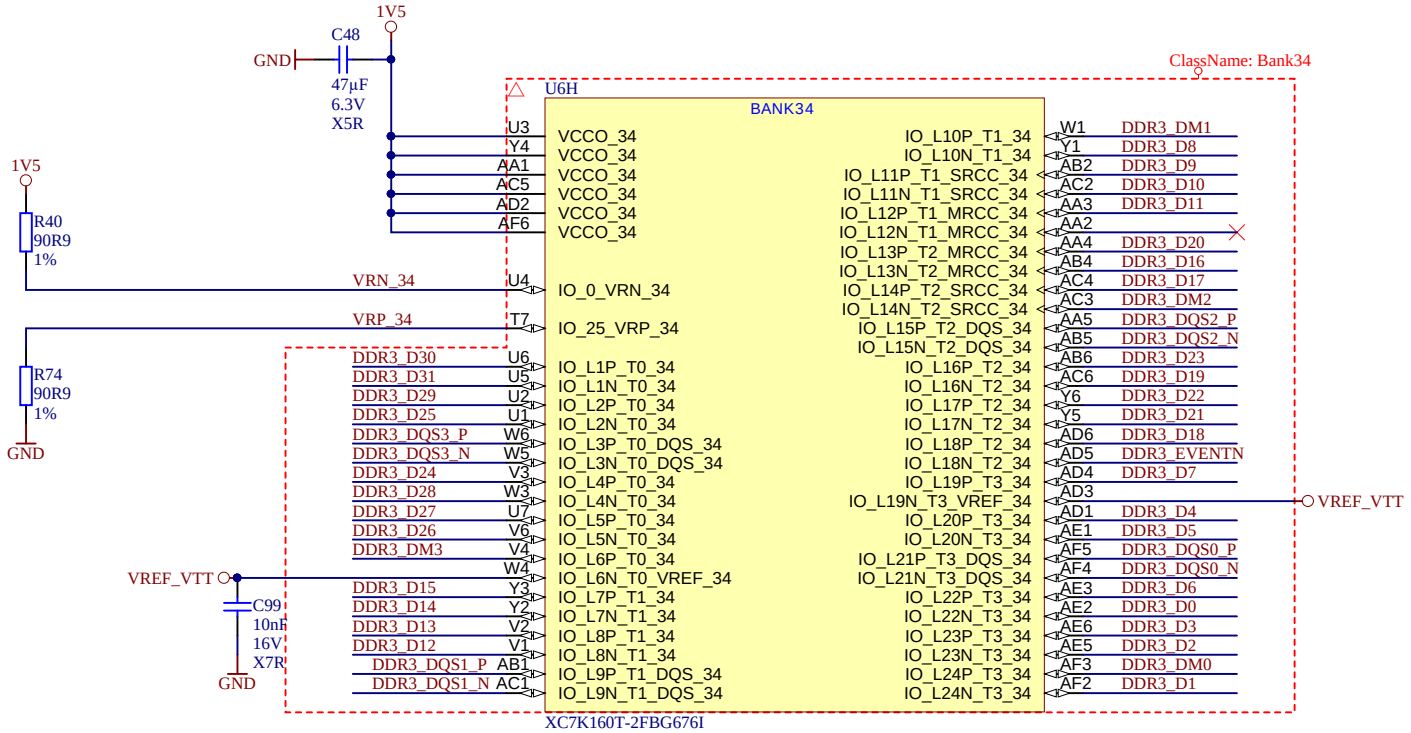
trenz electronic	Title: TEF1001 - DDR_BANKS		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page16 of 32
Filename: DDR_Banks.SchDoc			



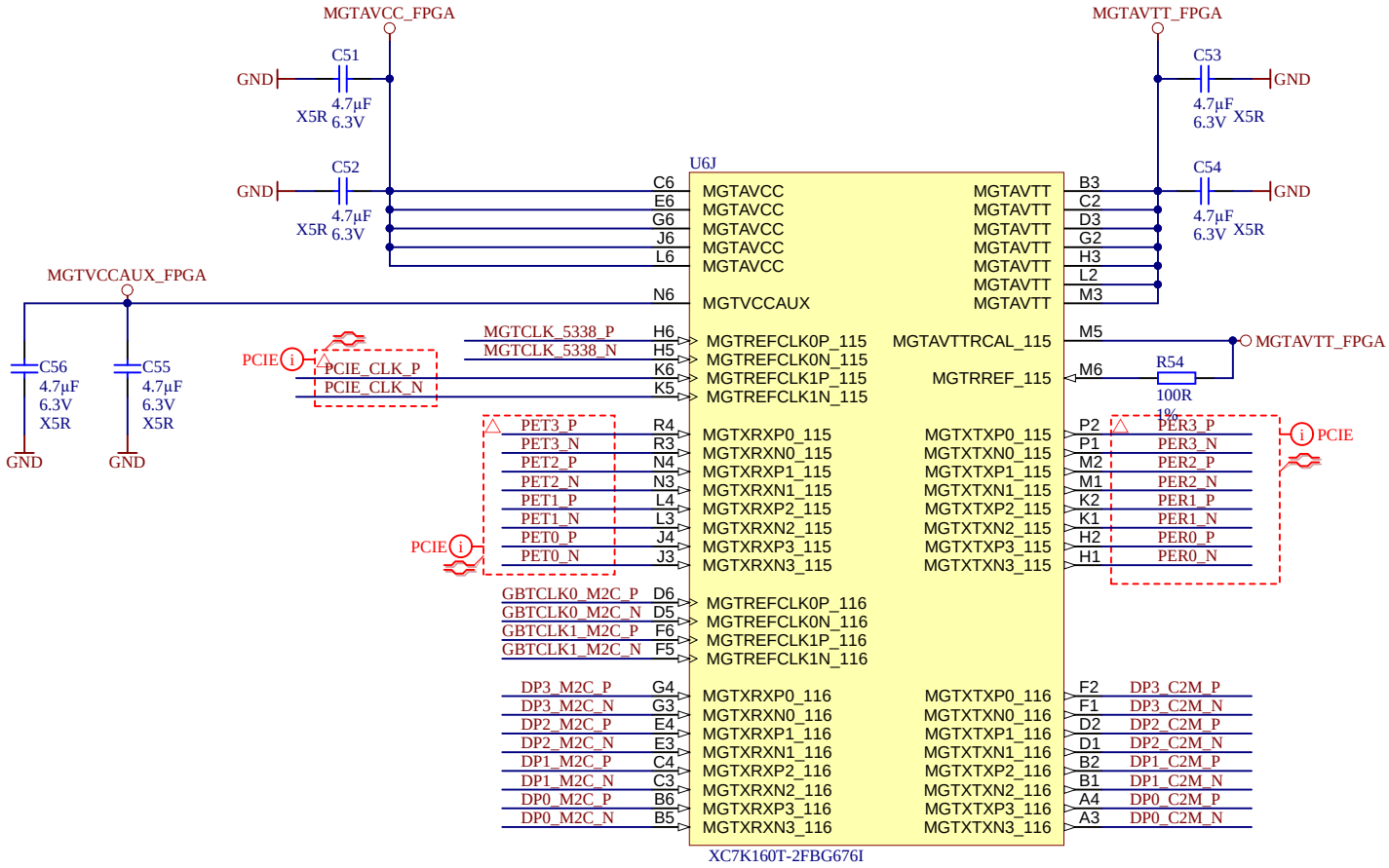
trenz electronic	Title: TEF1001 - FPGA_BANK_32		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page17 of 32
Filename: FPGA_BANK_32.SchDoc			



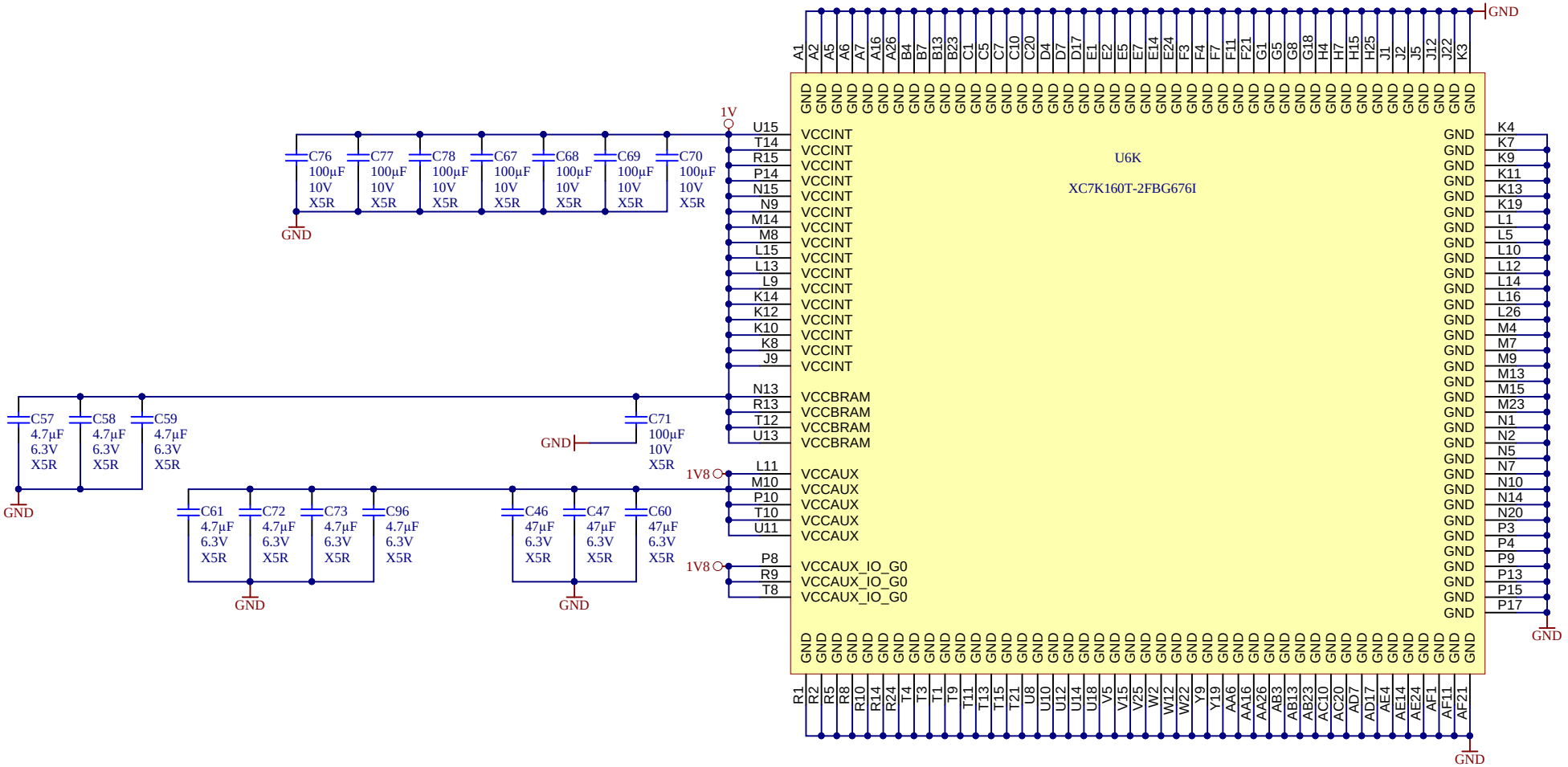
trenz electronic	Title: TEF1001 - FPGA_BANK_33		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page18 of 32
Filename: FPGA_BANK_33.SchDoc			



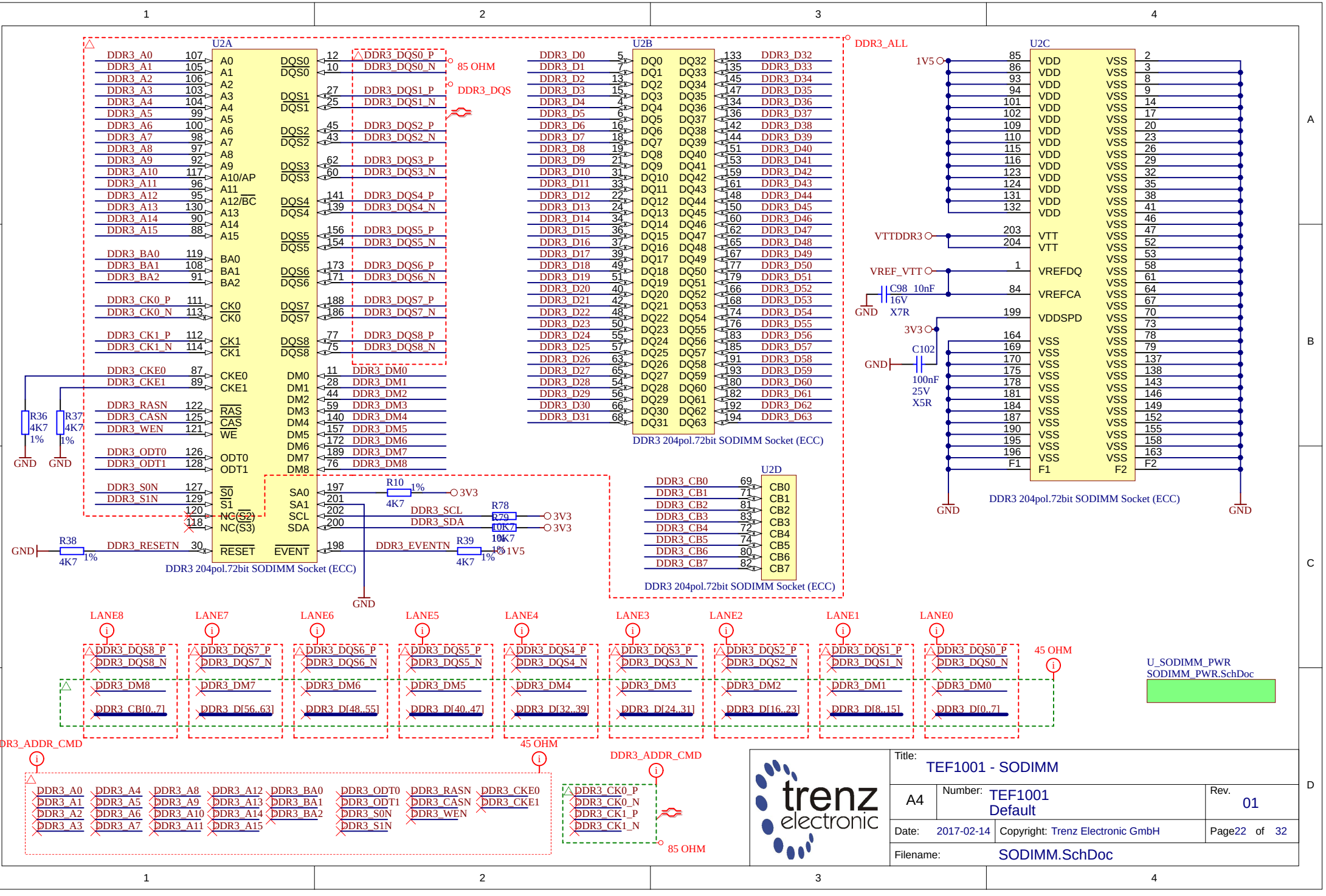
trenz electronic	Title: TEF1001 - FPGA_BANK_34		
	A4	Number: TEF1001 Default	Rev. 01
	Date: 2017-02-14	Copyright: Trenz Electronic GmbH	Page19 of 32
	Filename: FPGA_BANK_34.SchDoc		

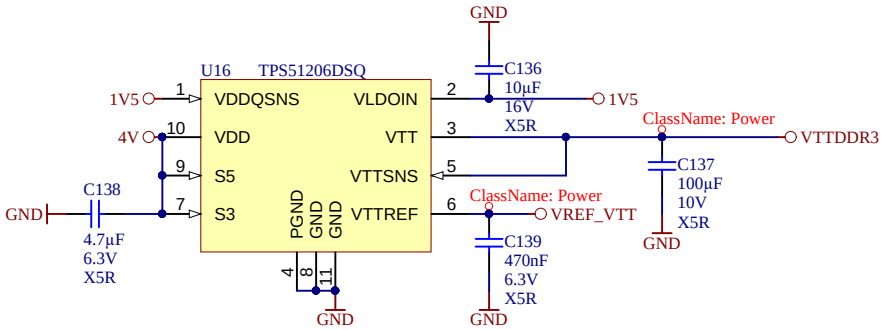


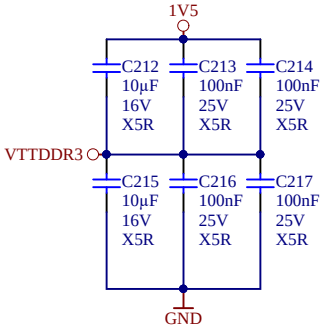
trenz electronic	Title: TEF1001_FPGA_MGT_BANKS		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page20 of 32
Filename: FPGA_MGT_BANKS.SchDoc			

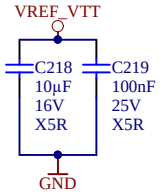


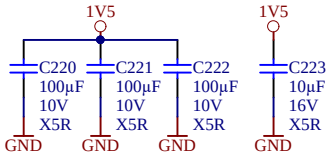
Title: TEF1001 - FPGA_POWER			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page21 of 32
Filename: FPGA_POWER.SchDoc			

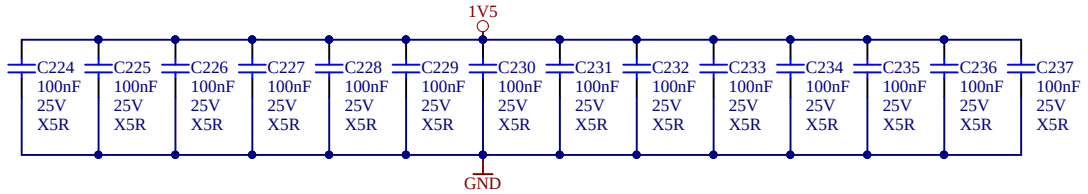

U2A
U2B
U2C
U2D
DDR3_ALL
85 OHM
DDR3_DQS
DDR3 204pol.72bit SODIMM Socket (ECC)
R36 4K7 1%
R37 4K7 1%
R38 4K7 1%
R10 4K7 1%
R39 4K7 1%
R78 10K7 1%
R79 10K7 1%
C98 10nF 16V X7R
C102 100nF 25V X5R
3V3
1V5
GND
VTTDDR3
VREF_VTT
LANE8
LANE7
LANE6
LANE5
LANE4
LANE3
LANE2
LANE1
LANE0
45 OHM
U_SODIMM_PWR
SODIMM_PWR.SchDoc
DDR3_ADDR_CMD
Title: TEF1001 - SODIMM
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
Copyright: Trenz Electronic GmbH
Page22 of 32
Filename: SODIMM.SchDoc





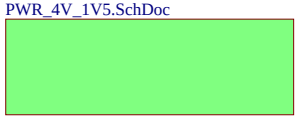




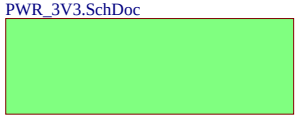


trenz electronic	Title: TEF1001 - SODIMM_PWR		
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page23 of 32
Filename: SODIMM_PWR.SchDoc			

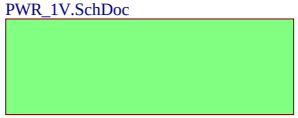
U_PWR_4V_1V5
PWR_4V_1V5.SchDoc



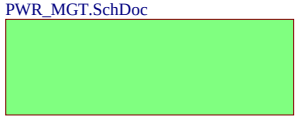
U_PWR_3V3
PWR_3V3.SchDoc



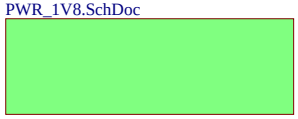
U_PWR_1V
PWR_1V.SchDoc



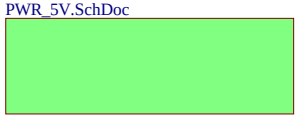
U_PWR_MGT
PWR_MGT.SchDoc



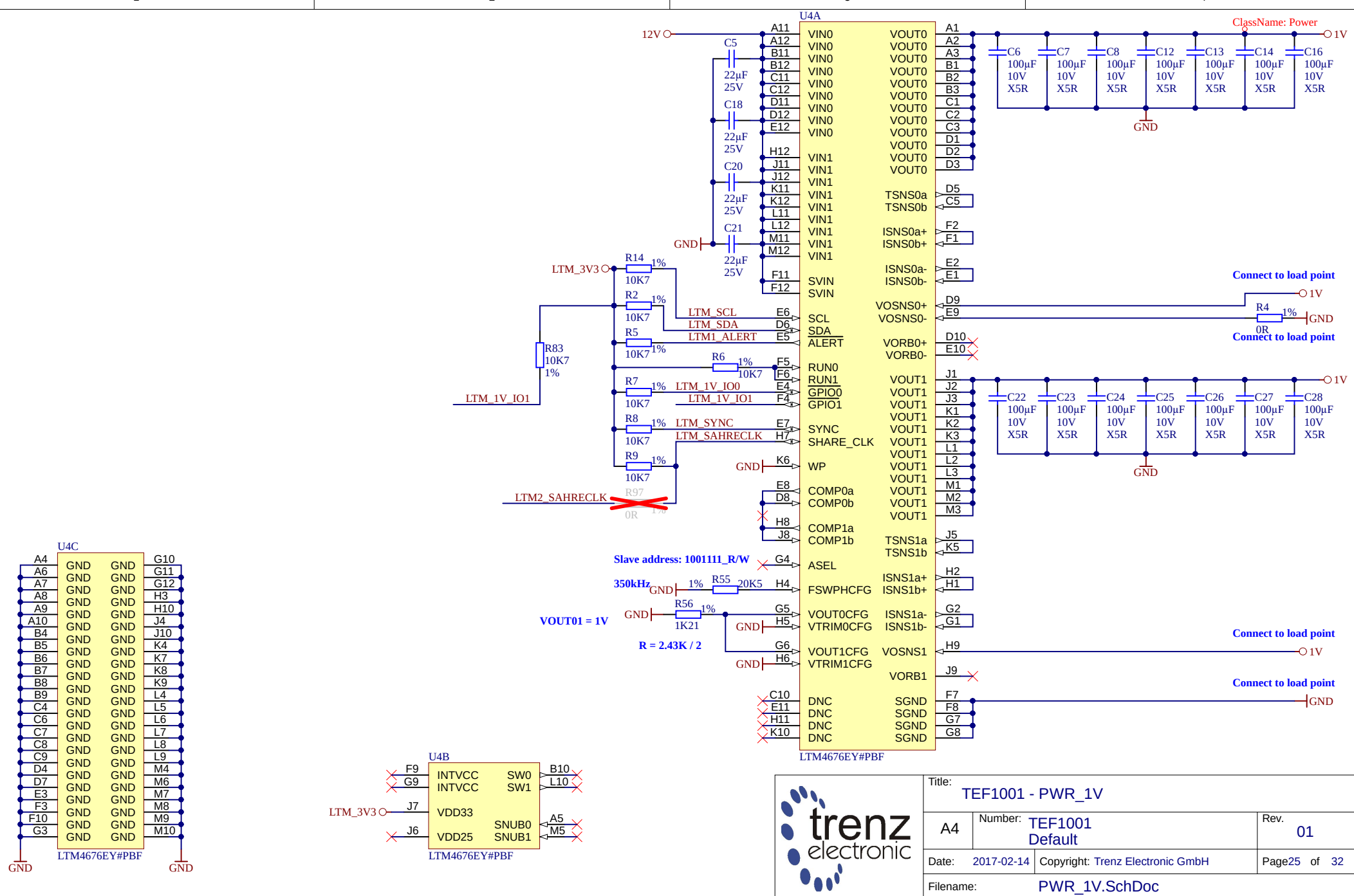
U_PWR_1V8
PWR_1V8.SchDoc

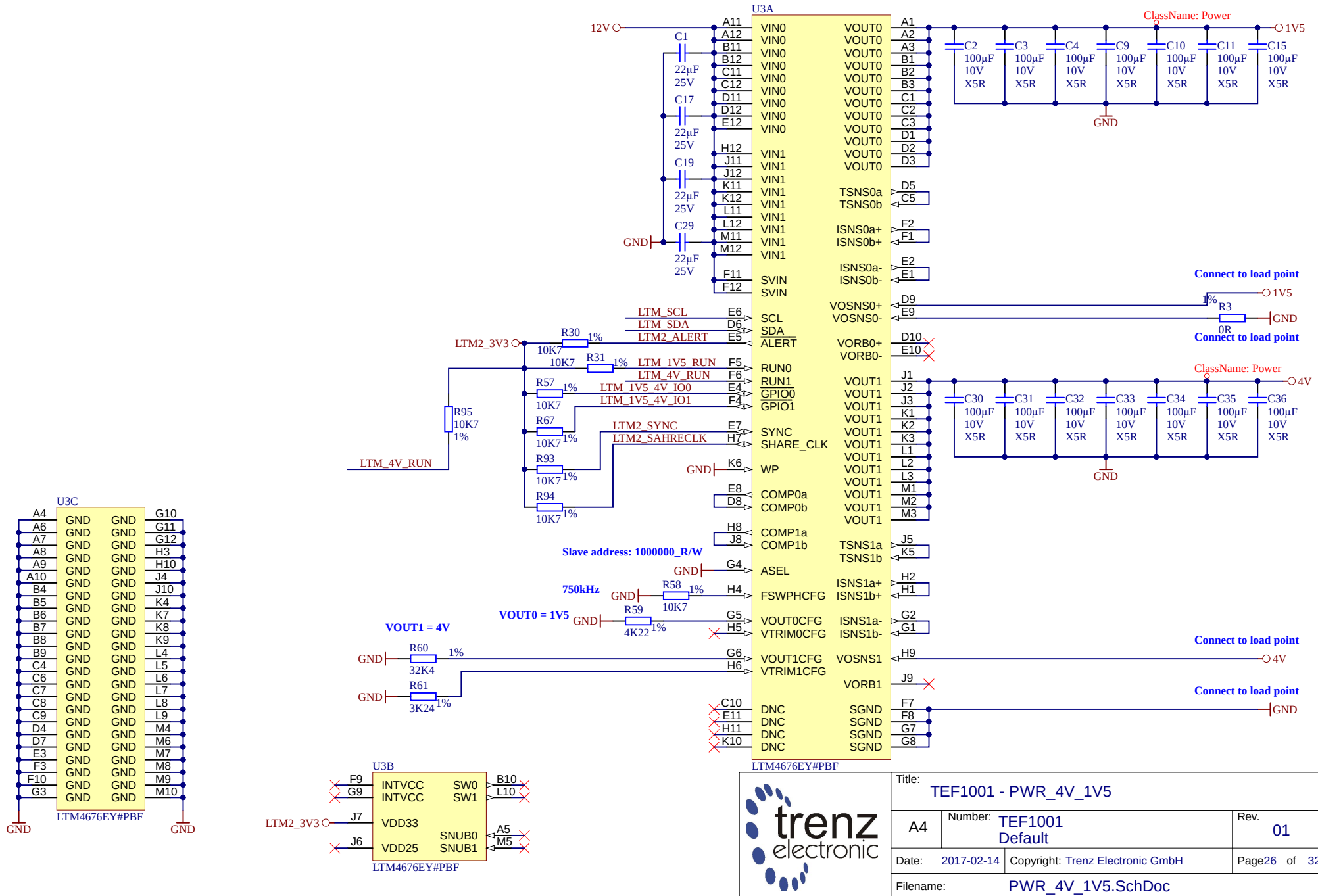


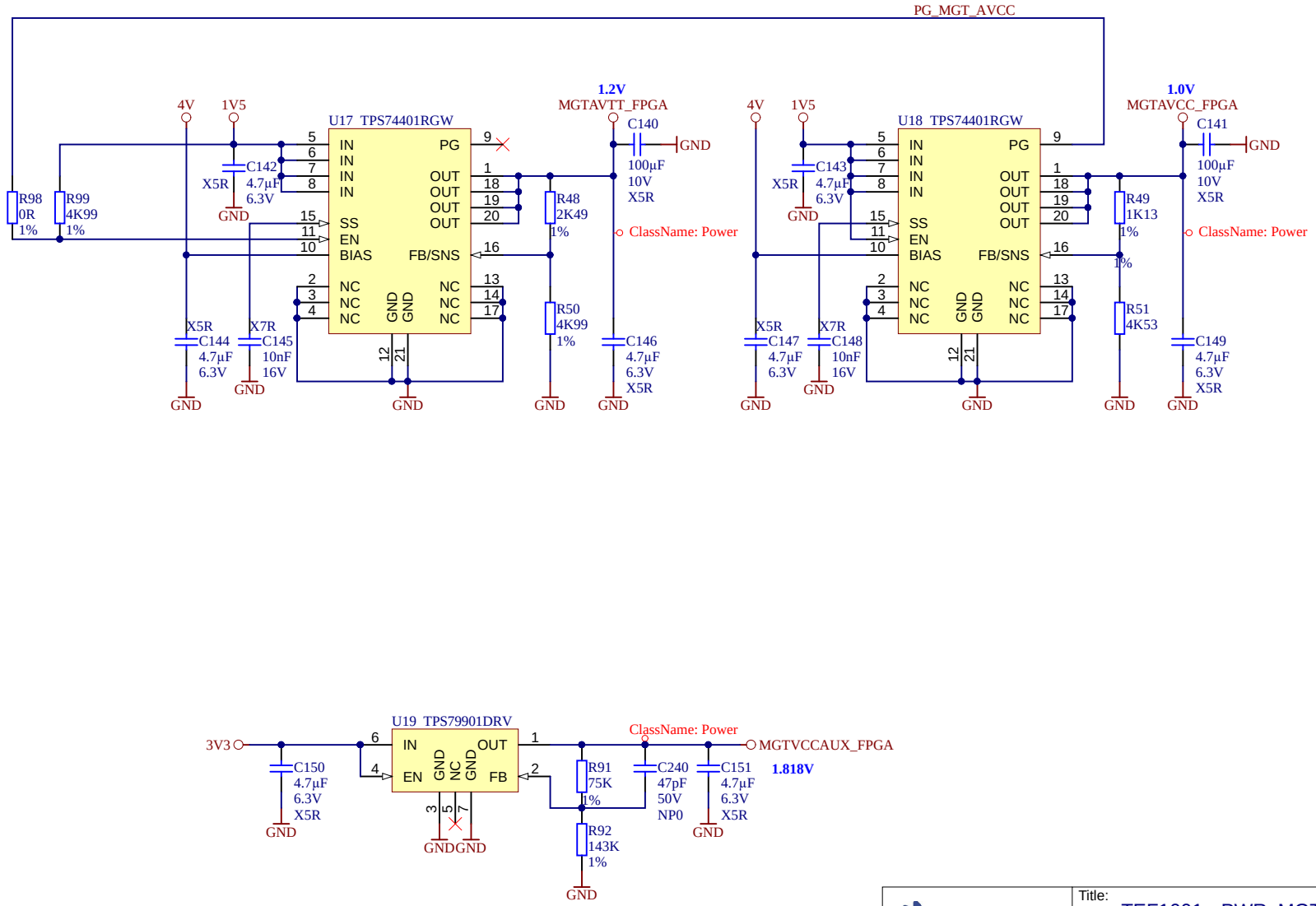
U_PWR_5V
PWR_5V.SchDoc



Title: TEF1001 - POWER			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page 24 of 32
Filename: POWER.SchDoc			


U4A
LTM4676EY#PBF
U4C
LTM4676EY#PBF
U4B
LTM4676EY#PBF
12V
1V
GND
LTM_3V3
LTM_SCL
LTM_SDA
LTM1_ALERT
LTM_1V_IO1
LTM_1V_IO0
LTM_SYNC
LTM_SAHRECLK
LTM2_SAHRECLK
Slave address: 1001111_R/W
350kHz
VOUT01 = 1V
R = 2.43K / 2
ClassName: Power
Connect to load point
Title: TEF1001 - PWR_1V
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
Copyright: Trenz Electronic GmbH
Page25 of 32
Filename: PWR_1V.SchDoc


U3A
LTM4676EY#PBF
U3C
LTM4676EY#PBF
U3B
LTM4676EY#PBF
12V
GND
LTM2_3V3
LTM_4V_RUN
LTM_SCL
LTM_SDA
LTM2_ALERT
LTM_1V5_RUN
LTM_4V_RUN
LTM_1V5_4V_IO0
LTM_1V5_4V_IO1
LTM2_SYNC
LTM2_SAHRECLK
Slave address: 1000000_R/W
750kHz
VOUT0 = 1V5
VOUT1 = 4V
ClassName: Power
1V5
4V
Connect to load point
Title: TEF1001 - PWR_4V_1V5
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
Copyright: Trenz Electronic GmbH
Page26 of 32
Filename: PWR_4V_1V5.SchDoc



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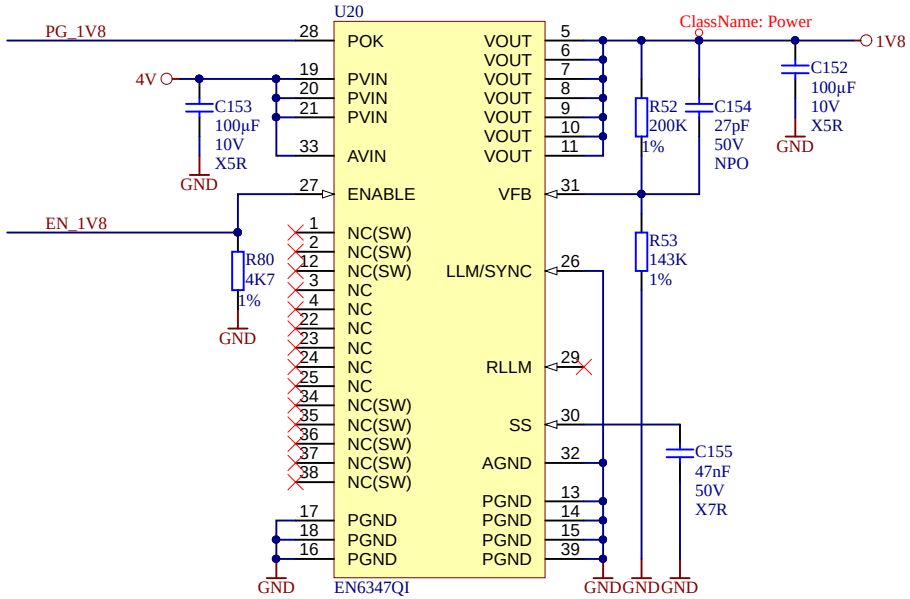
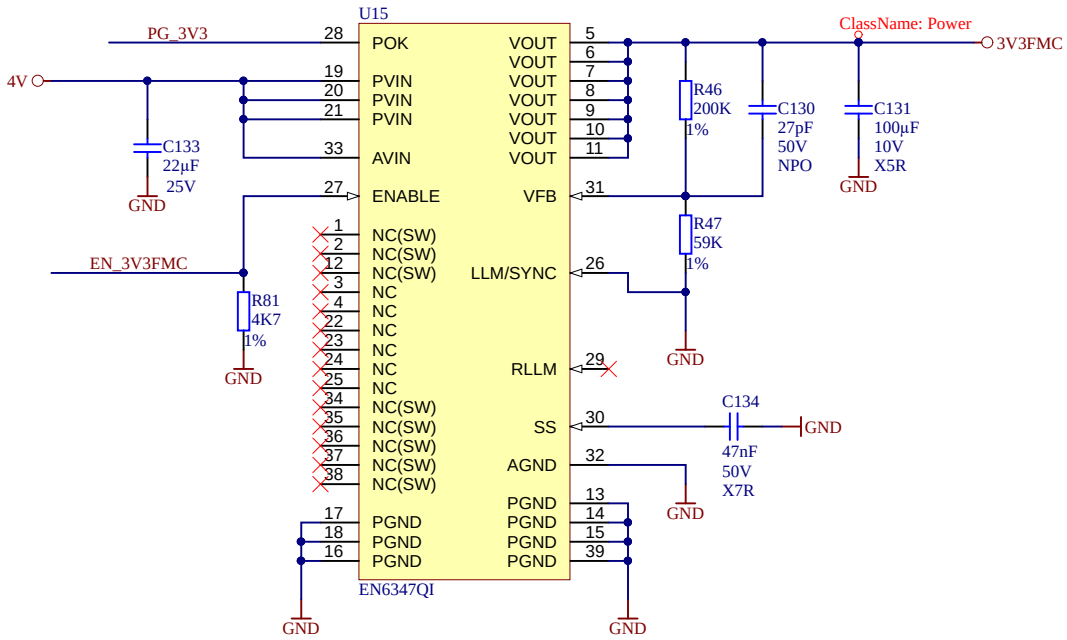
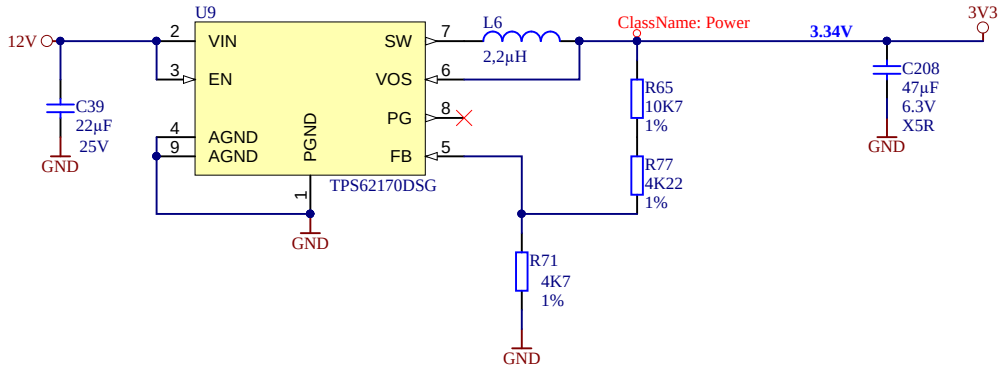
Title: TEF1001 - PWR_MGT			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page27 of 32
Filename: PWR_MGT.SchDoc			

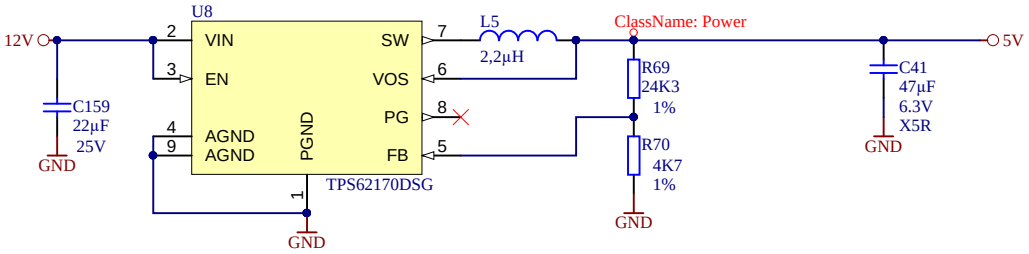


trenz electronic	Title: TEF1001 - PWR_1V8		
	A4	Number: TEF1001 Default	Rev. 01
	Date: 2017-02-14	Copyright: Trenz Electronic GmbH	Page28 of 32
	Filename: PWR_1V8.SchDoc		

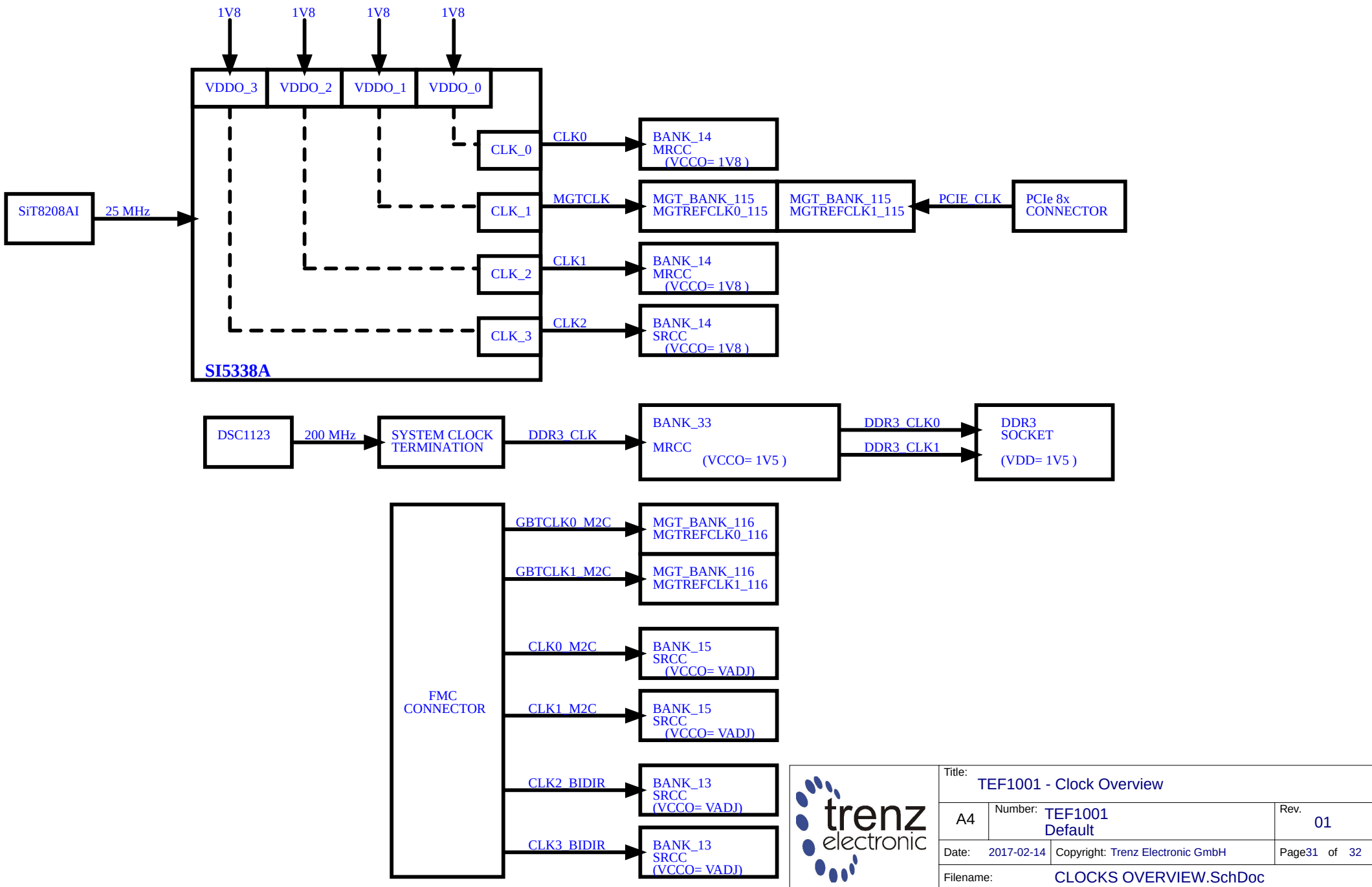




trenz electronic	Title: TEF1001 - PWR_3V3		
	A4	Number: TEF1001 Default	Rev. 01
	Date: 2017-02-14	Copyright: Trenz Electronic GmbH	Page29 of 32
	Filename: PWR_3V3.SchDoc		



Title: TEF1001 - PWR_5V			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page30 of 32
Filename: PWR_5V.SchDoc			



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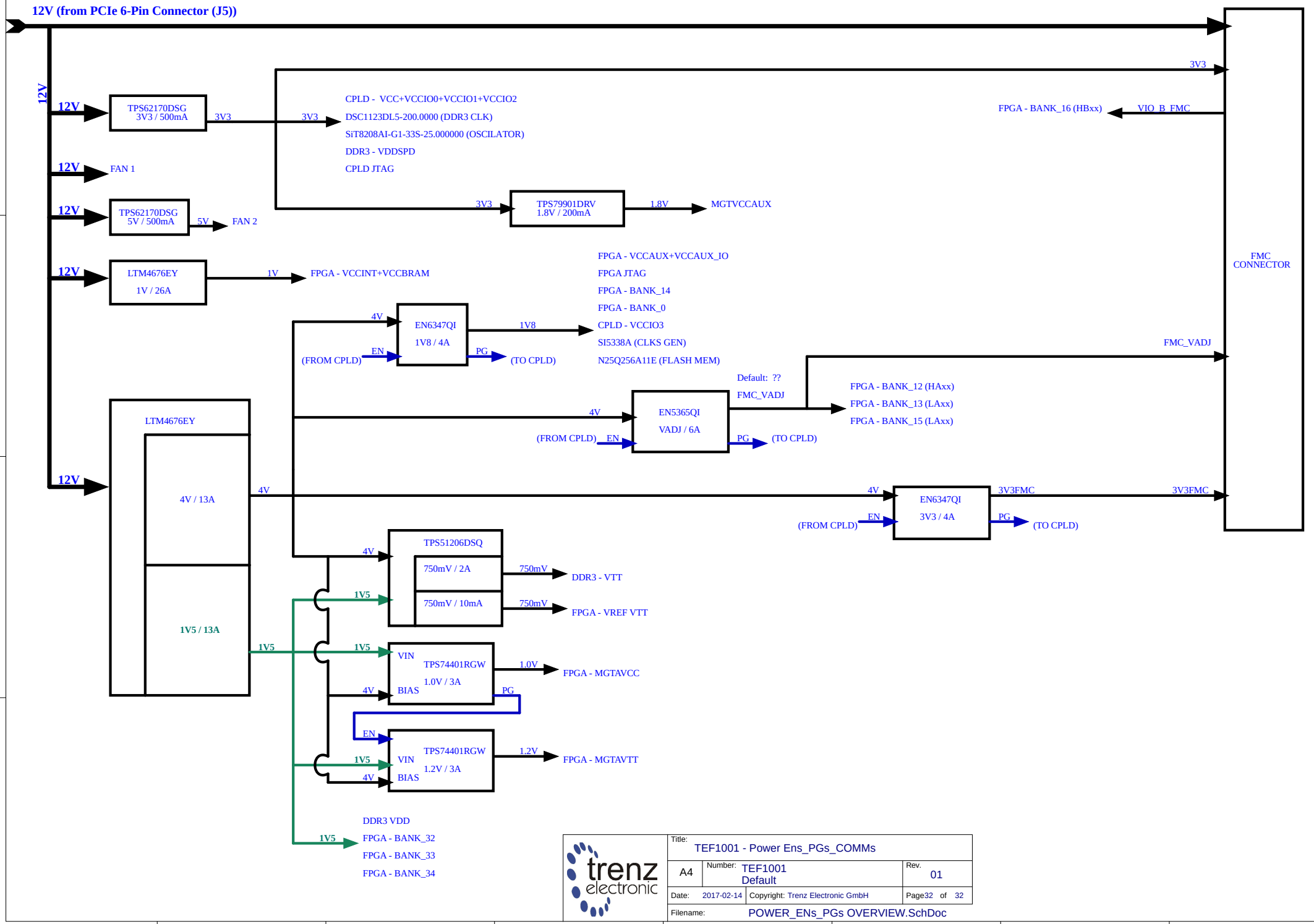
Title: TEF1001 - Clock Overview			
A4	Number: TEF1001 Default		Rev. 01
Date: 2017-02-14	Copyright: Trenz Electronic GmbH		Page31 of 32
Filename: CLOCKS OVERVIEW.SchDoc			


12V (from PCIe 6-Pin Connector (J5))
12V
TPS62170DSG
3V3 / 500mA
3V3
CPLD - VCC+VCCIO0+VCCIO1+VCCIO2
DSC1123DL5-200.0000 (DDR3 CLK)
SiT8208AI-G1-33S-25.000000 (OSCILATOR)
DDR3 - VDDSPD
CPLD JTAG
FAN 1
TPS62170DSG
5V / 500mA
5V
FAN 2
TPS79901DRV
1.8V / 200mA
1.8V
MGTVCCAUX
LTM4676EY
1V / 26A
1V
FPGA - VCCINT+VCCBRAM
FPGA - VCCAUX+VCCAUX_IO
FPGA JTAG
FPGA - BANK_14
FPGA - BANK_0
CPLD - VCC03
SI5338A (CLKS GEN)
N25Q256A11E (FLASH MEM)
EN6347QI
1V8 / 4A
4V
EN
PG
1V8
(FROM CPLD)
(TO CPLD)
LTM4676EY
4V / 13A
1V5 / 13A
EN5365QI
VADJ / 6A
Default: ??
FMC_VADJ
FPGA - BANK_12 (HAxx)
FPGA - BANK_13 (LAxx)
FPGA - BANK_15 (LAxx)
EN6347QI
3V3 / 4A
3V3FMC
TPS51206DSQ
750mV / 2A
750mV / 10mA
750mV
DDR3 - VTT
FPGA - VREF VTT
TPS74401RGW
1.0V / 3A
VIN
BIAS
1.0V
FPGA - MGTAVCC
TPS74401RGW
1.2V / 3A
1.2V
FPGA - MGTAVTT
DDR3 VDD
FPGA - BANK_32
FPGA - BANK_33
FPGA - BANK_34
3V3
FPGA - BANK_16 (HBxx)
VIO_B_FMC
FMC_VADJ
FMC CONNECTOR
3V3FMC
trenz electronic
Title: TEF1001 - Power Ens_PGs_COMMs
A4
Number: TEF1001 Default
Rev. 01
Date: 2017-02-14
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Page32 of 32
Filename: POWER_ENs_PGs OVERVIEW.SchDoc