Special notes:

U_FPGA
FPGA.SchDoc

U_SODIMM
SODIMM.SchDoc

U_CLOCK
CLOCK.SchDoc

U_POWER
POWER.SchDoc

U_CONN
CONN.SchDoc

U_CPLD
CPLD.SchDoc

PM1 FIDU-DOT - small

PM2 FIDU-DOT - small

PM3 FIDU-DOT - small

PM4 FIDU-DOT - small

PM5 FIDU-DOT - small

PM6 FIDU-DOT - small

Serial
Serial
Serialnumber 6,3 x 6.3mm

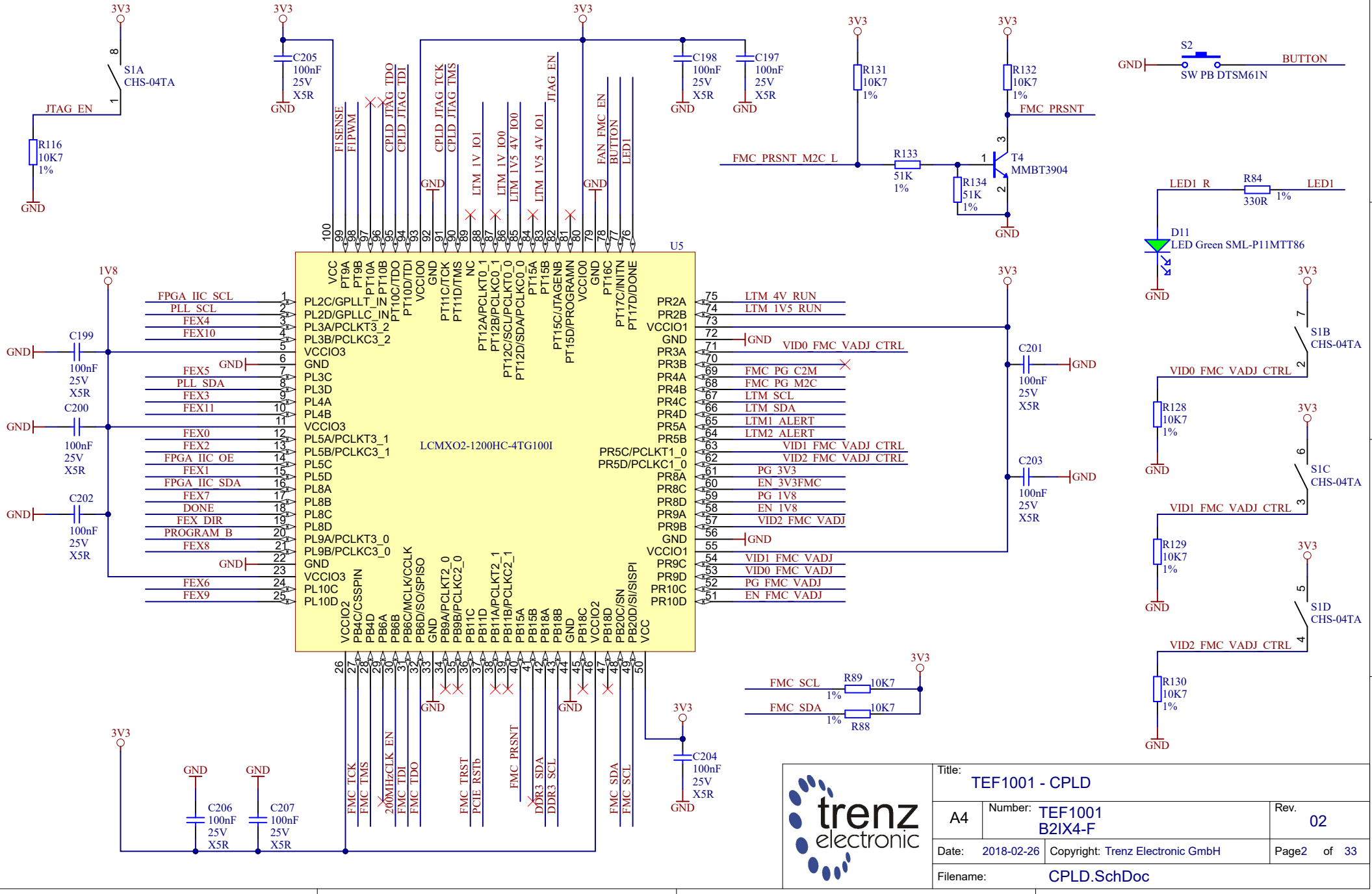
LOGO1
TE Logo PRINT Layer
LOGO PRINT

Front Bracket screw head on Top
MECH1
Slotblende Ndigo xTDC4 Lemo

Front Bracket screw head on Bottom
MECH2
TEF1001 PCIe Frontplate

trenz electronic

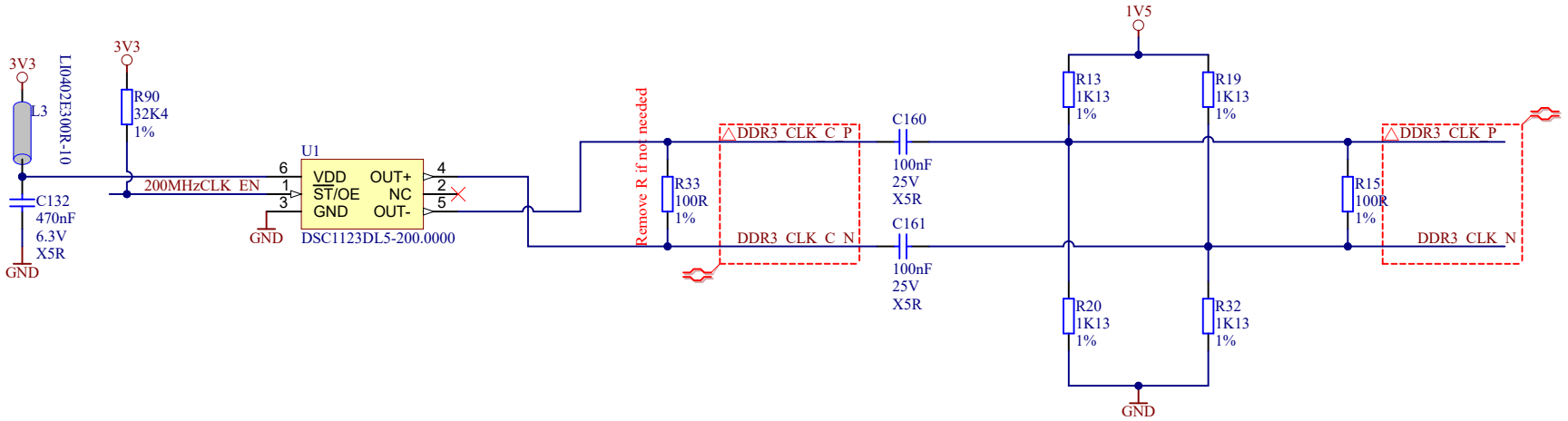
Title: TEF1001 - MAIN			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page1 of 33
Filename: TEF1001.SchDoc			



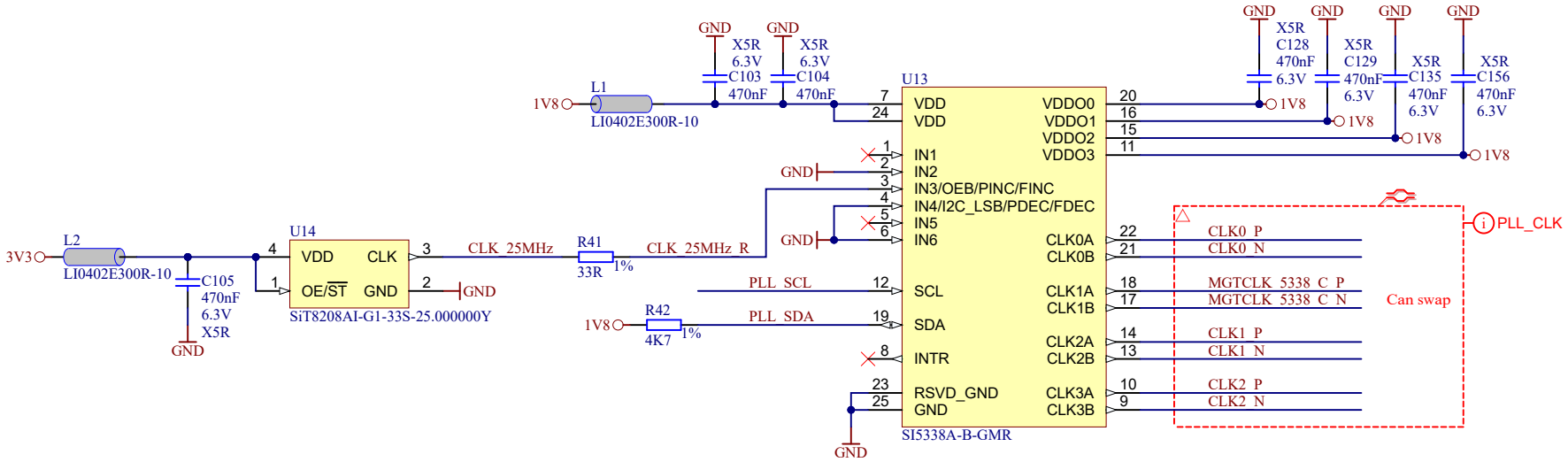
trenz electronic

Title: TEF1001 - CPLD			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page2 of 33
Filename: CPLD.SchDoc			

U_CLK-SI5338
CLK-SI5338.SchDoc



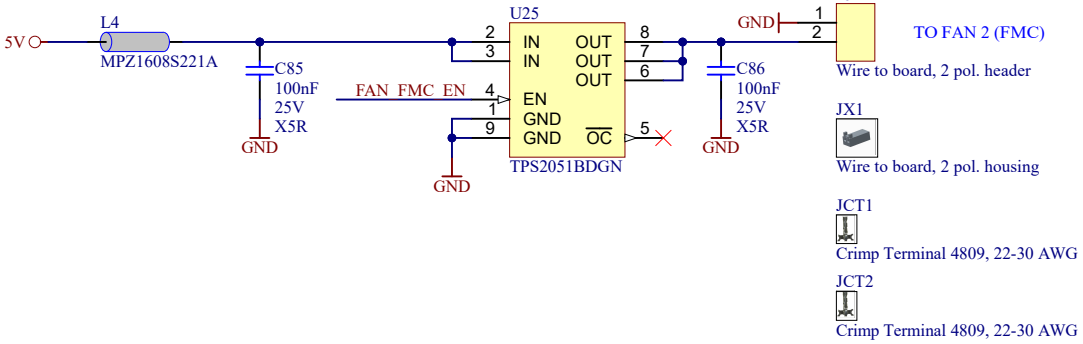
Title: TEF1001 - CLOCK			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page3 of 33
Filename: CLOCK.SchDoc			

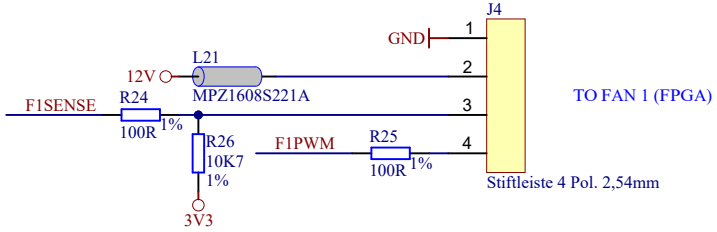


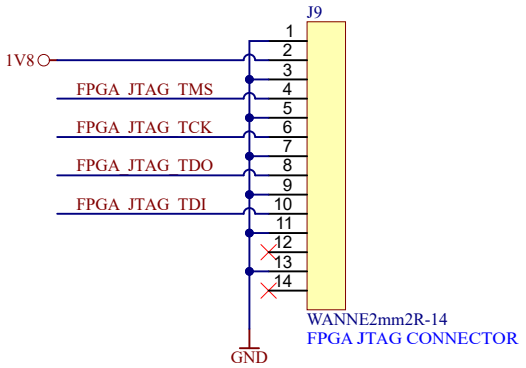
Title: TEF1001 - CLK-SI5338			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page4 of 33
Filename: CLK-SI5338.SchDoc			

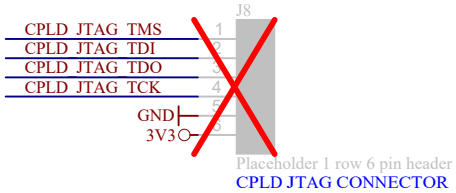
U_FMC
FMC.SchDoc

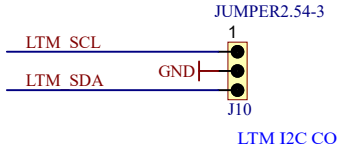
U_PCIE_CONN
PCIE_CONN.SchDoc





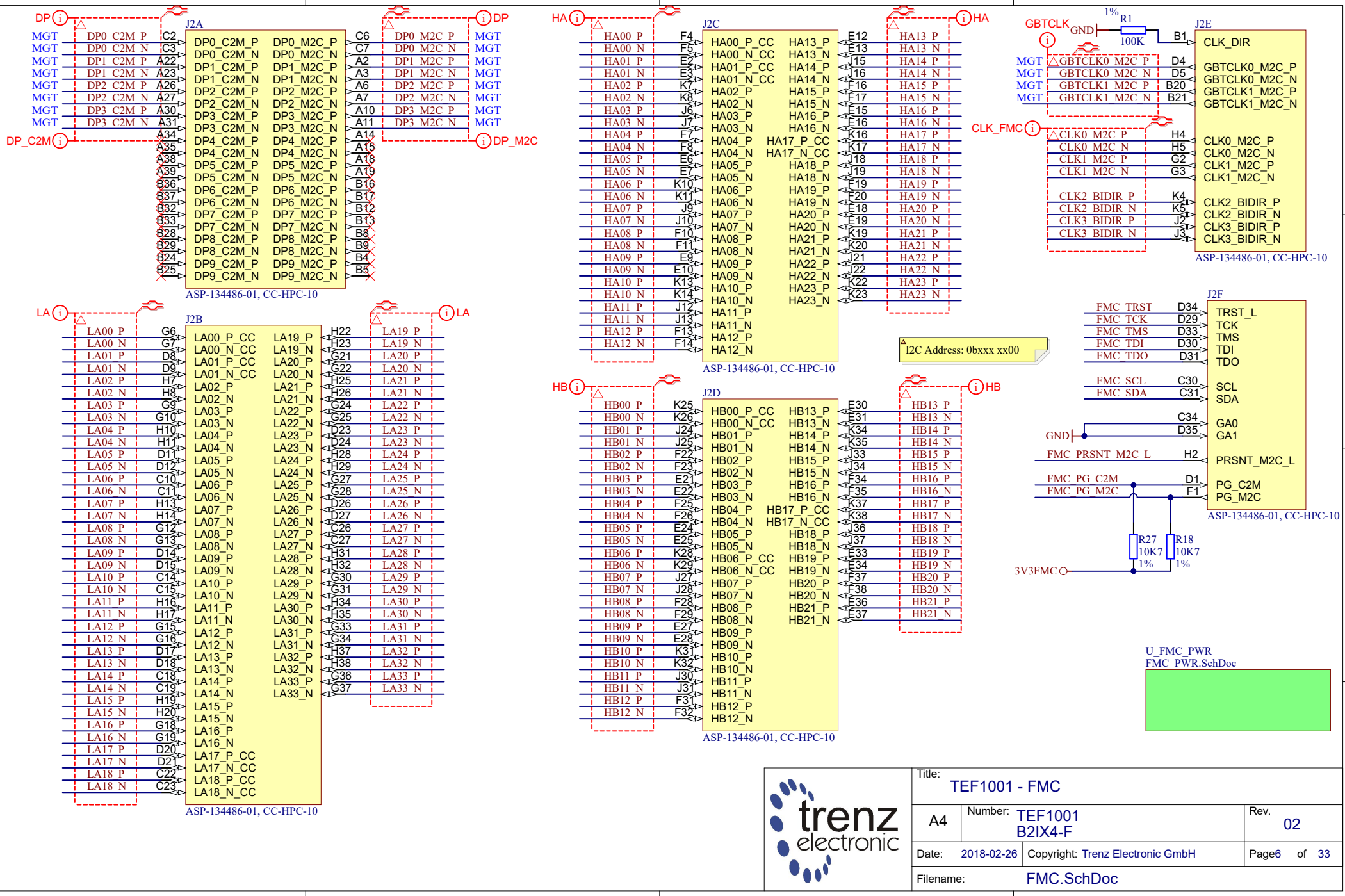






trenz electronic

Title: TEF1001 - CONN			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page5 of 33
Filename: CONN.SchDoc			



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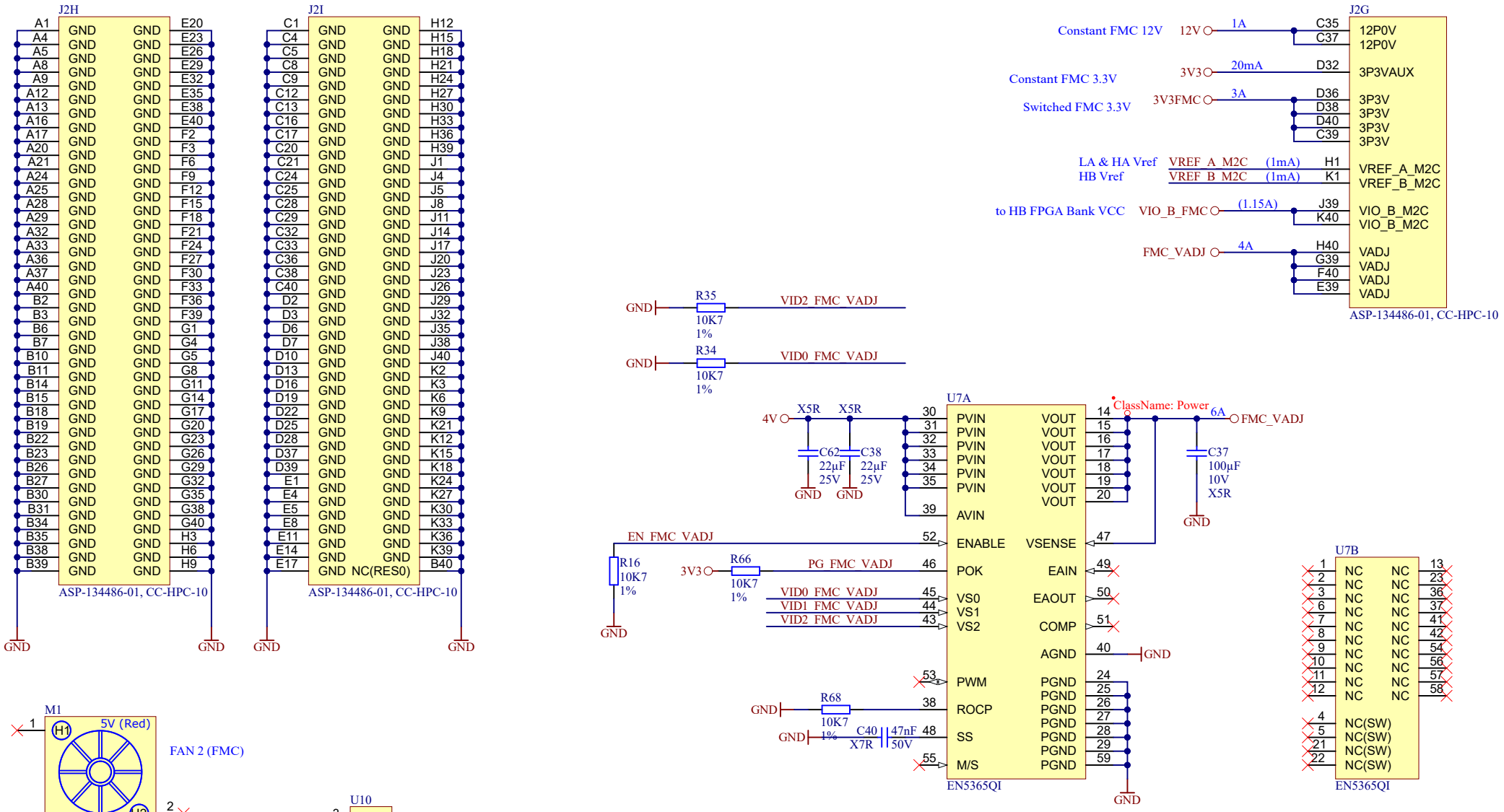
Title: TEF1001 - FMC			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page6 of 33
Filename: FMC.SchDoc			


J2H
J2I
J2G
ASP-134486-01, CC-HPC-10
Constant FMC 12V
Constant FMC 3.3V
Switched FMC 3.3V
LA & HA Vref
HB Vref
to HB FPGA Bank VCC
FMC_VADJ
U7A
EN5365QI
U7B
R35
R34
R16
R66
R68
C62
C38
C37
C40
VID2_FMC_VADJ
VID0_FMC_VADJ
VID1_FMC_VADJ
PG_FMC_VADJ
EN_FMC_VADJ
M1
FAN 2 (FMC)
FAN 5VDC 45X5MM .7W 1.06CFM
U10
Single FMC Con. Cooled BB Snap
Type: Set as Standard (No BOM)
VS2 | VS1 | VS0 | Output Voltage
0 | 0 | 0 | 3.3V
0 | 0 | 1 | 2.5V
0 | 1 | 0 | 1.8V
0 | 1 | 1 | 1.5V
1 | 0 | 0 | 1.25V
1 | 0 | 1 | 1.2V
trenz electronic
Title: TEF1001 - FMC_PWR
A4
Number: TEF1001 B2IX4-F
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
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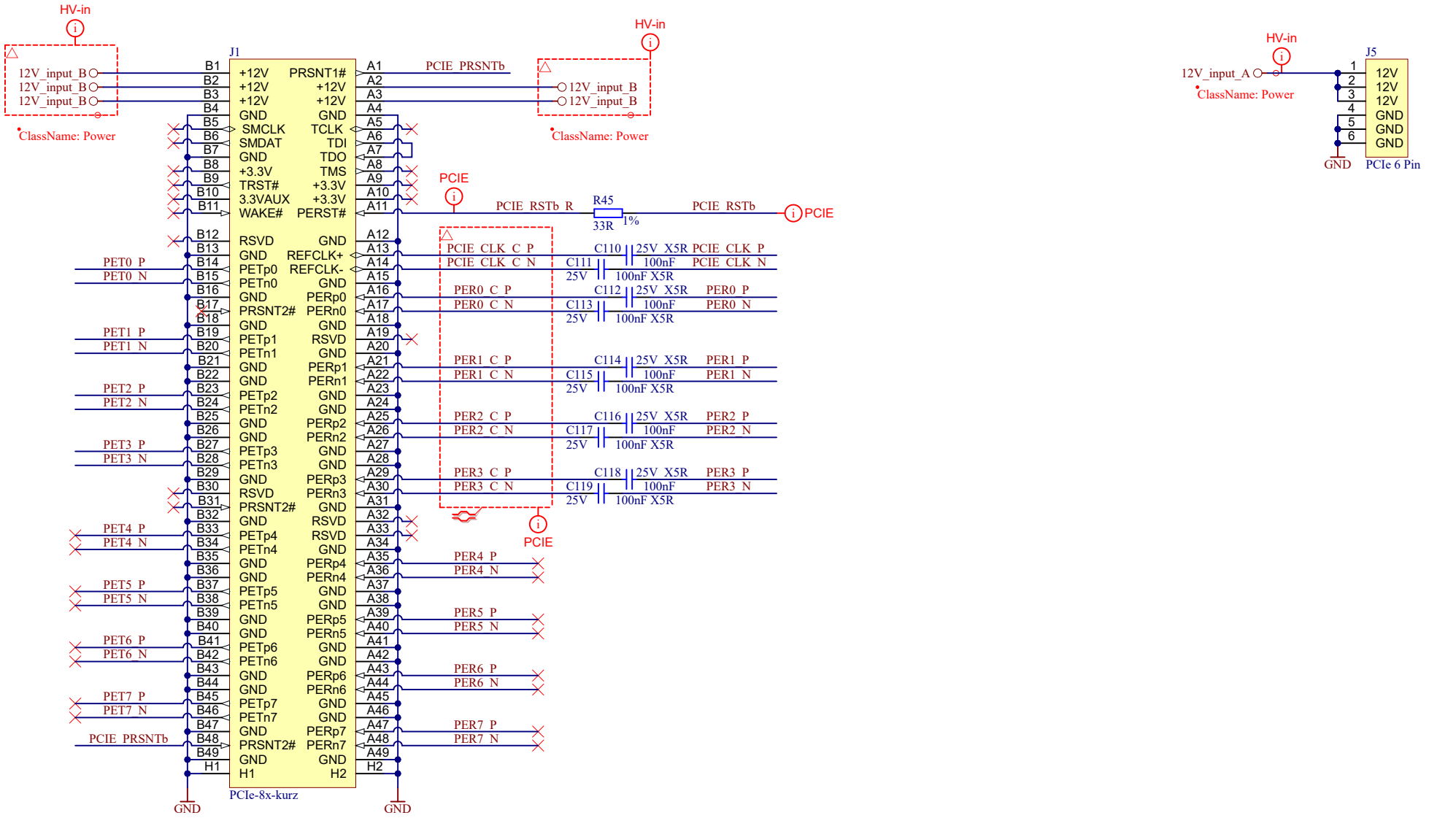
Filename: FMC_PWR.SchDoc



trenz electronic	Title: TEF1001 - PCIE CONNECTOR		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page8 of 33
Filename: PCIE_CONN.SchDoc			

U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

U_FPGA_BANK_16
FPGA_BANK_16.SchDoc

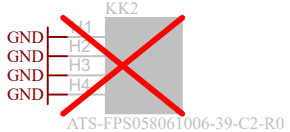
U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

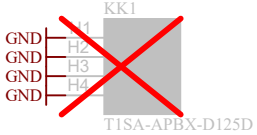
U_DDR_Banks
DDR_Banks.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

HEATSINK TYPE 2 (FPGA)



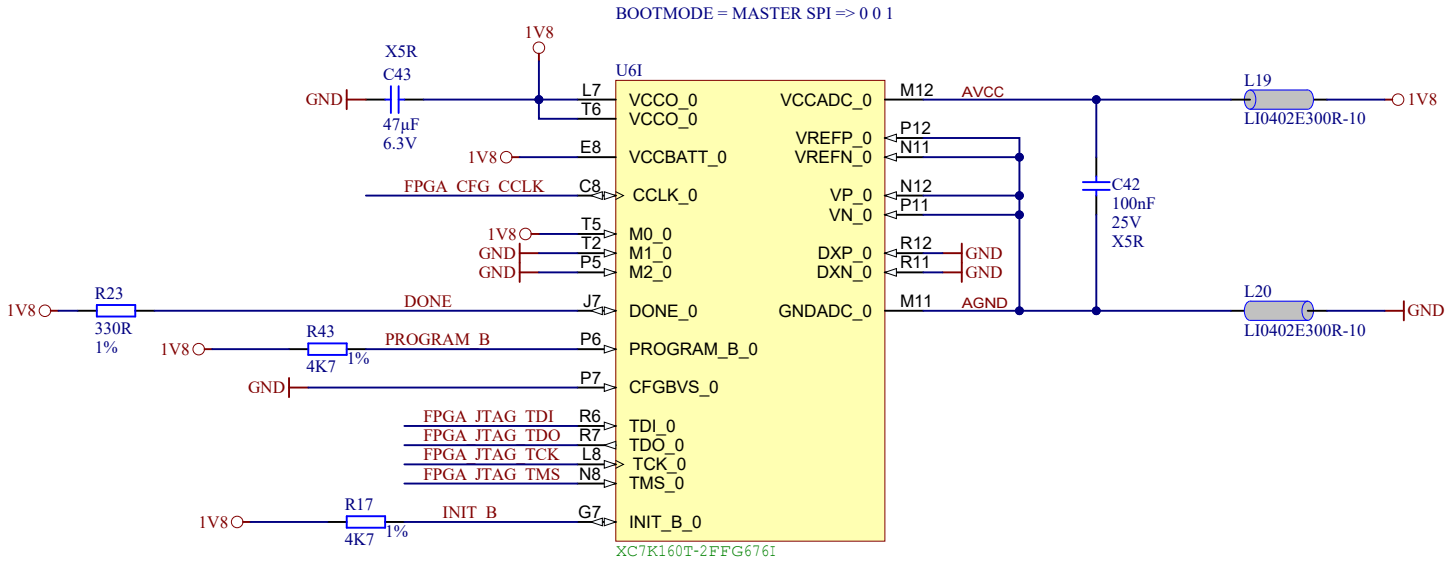
HEATSINK TYPE 1 (FPGA)



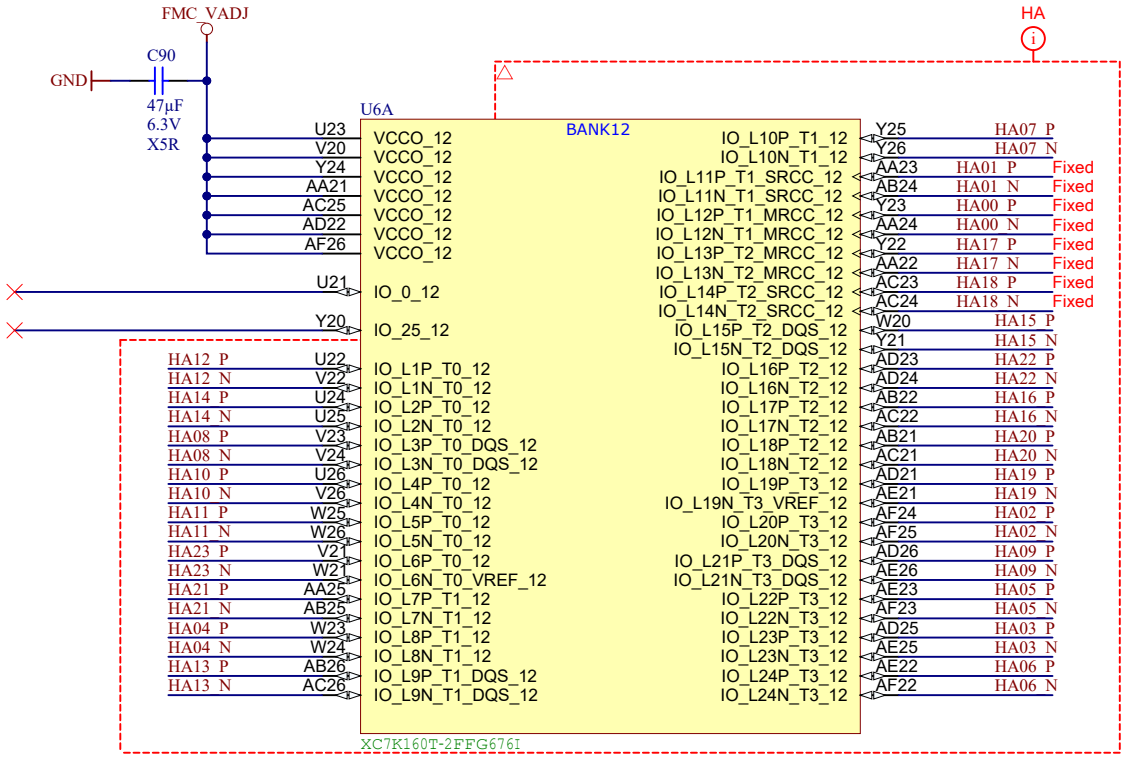
Hardware for HEATSINK TYPE 2 (FPGA)

trenz electronic

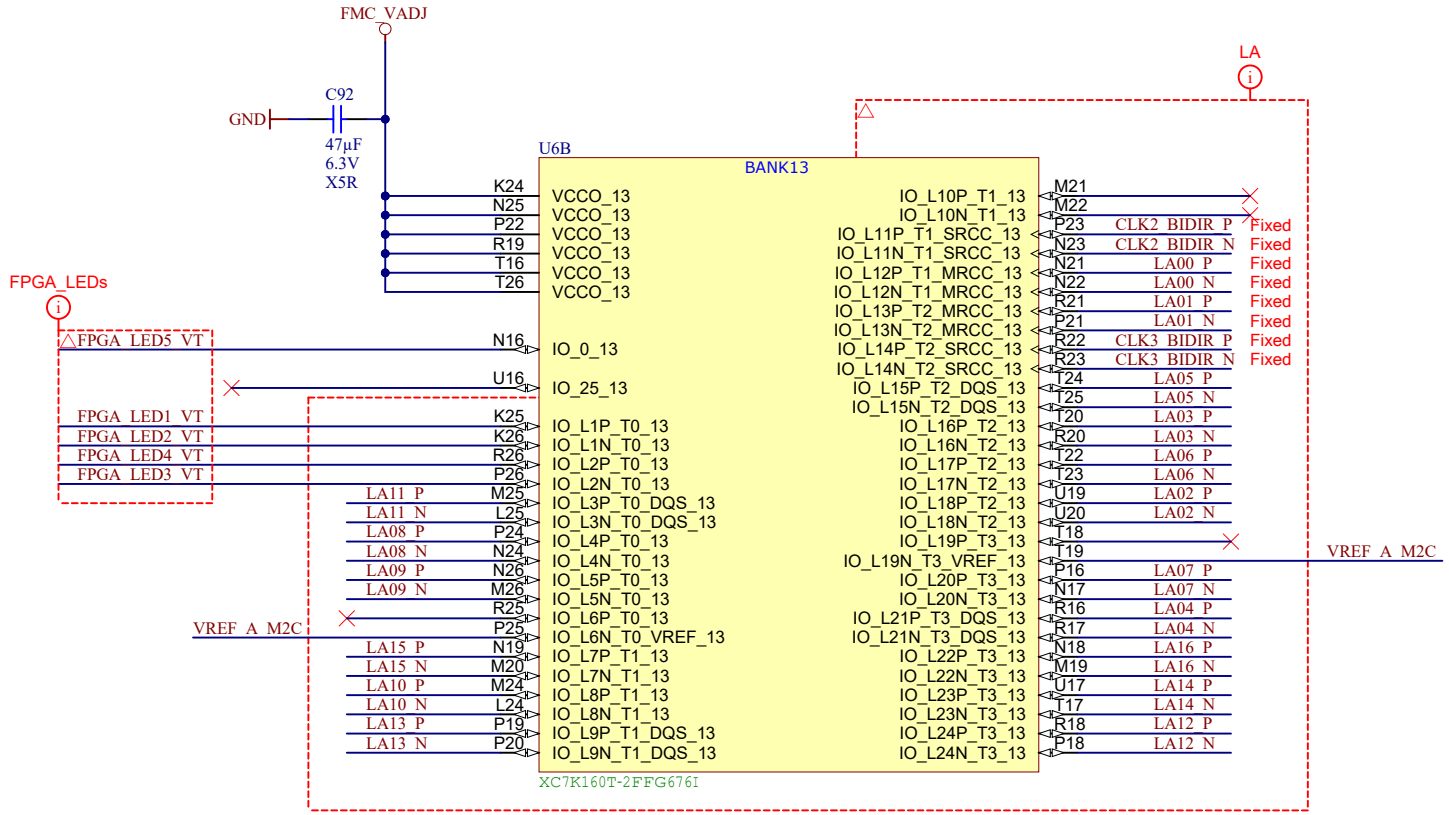
Title: TEF1001 - FPGA			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page9 of 33
Filename: FPGA.SchDoc			



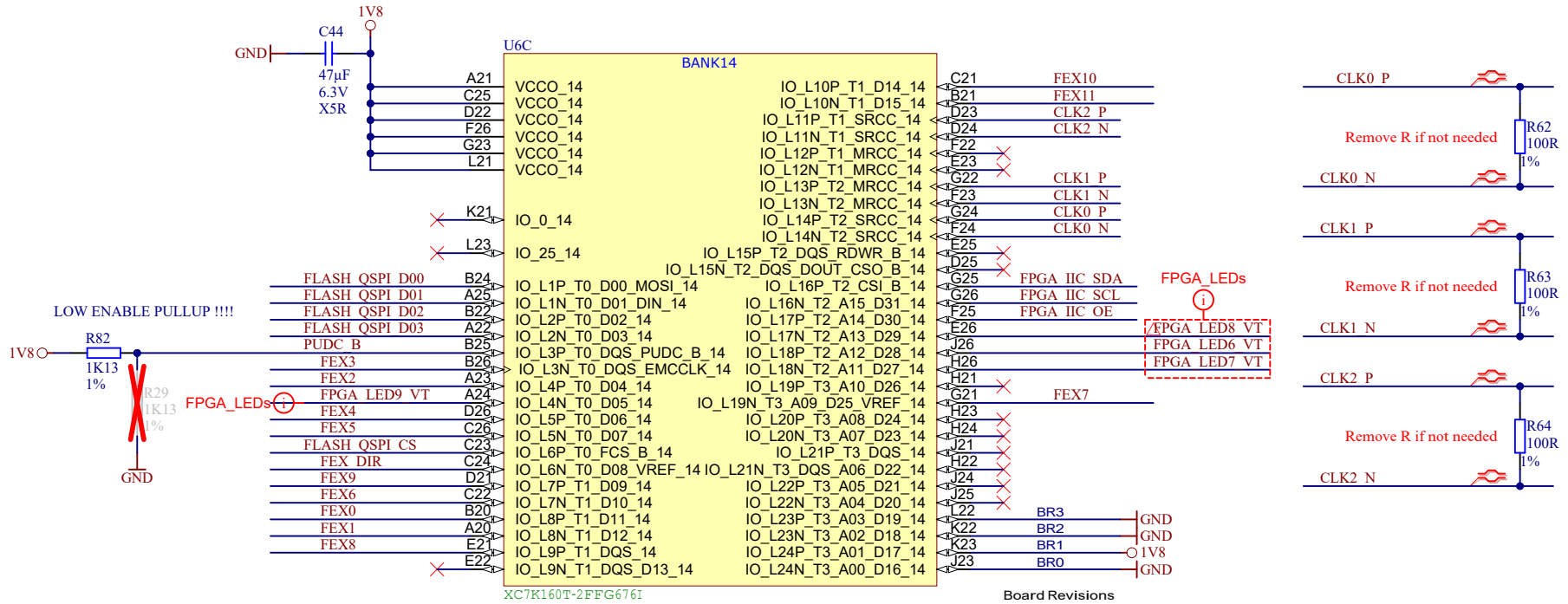
trenz electronic	Title: TEF1001 - FPGA_CFG		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page10 of 33
Filename: FPGA_CFG.SchDoc			



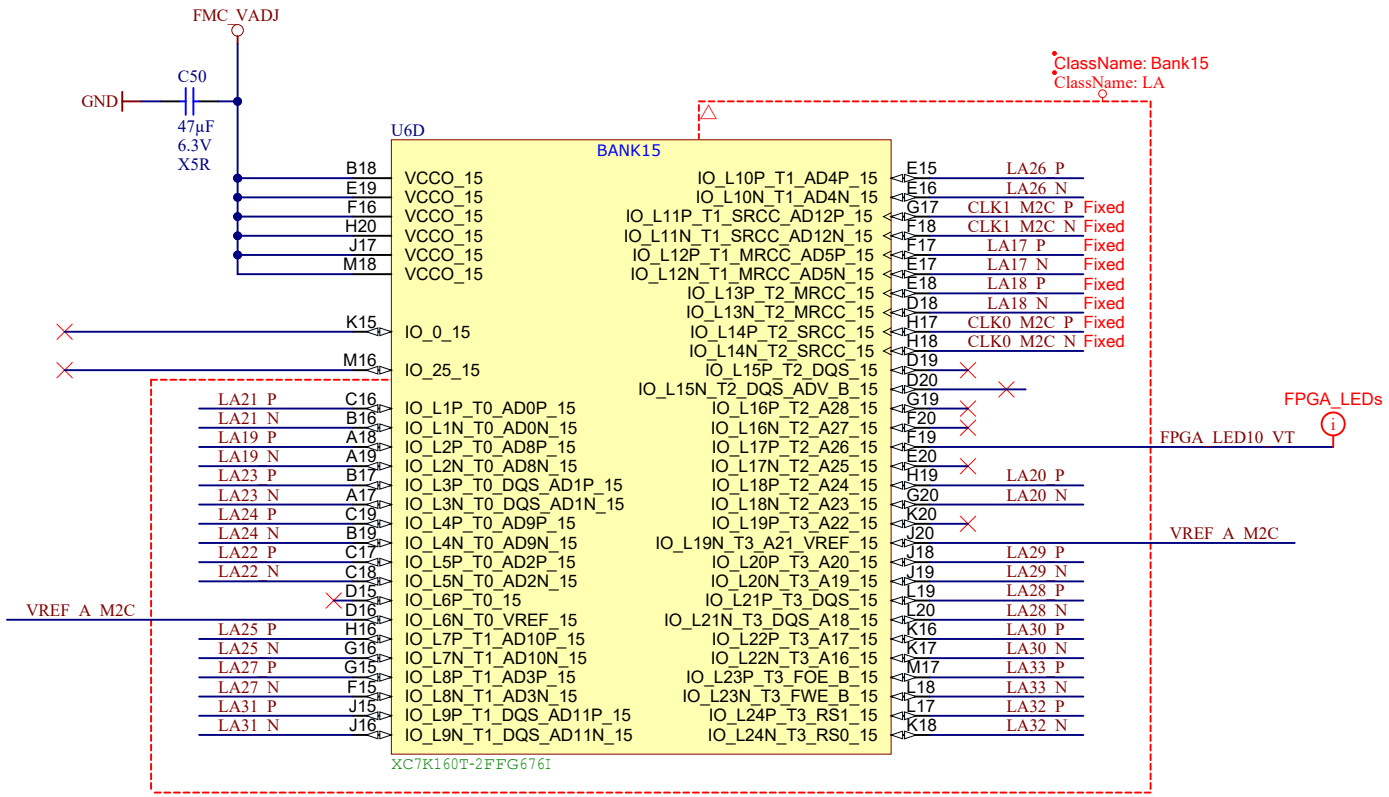
trenz electronic	Title: TEF1001 - FPGA_BANK_12		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page 11 of 33
Filename: FPGA_BANK_12.SchDoc			



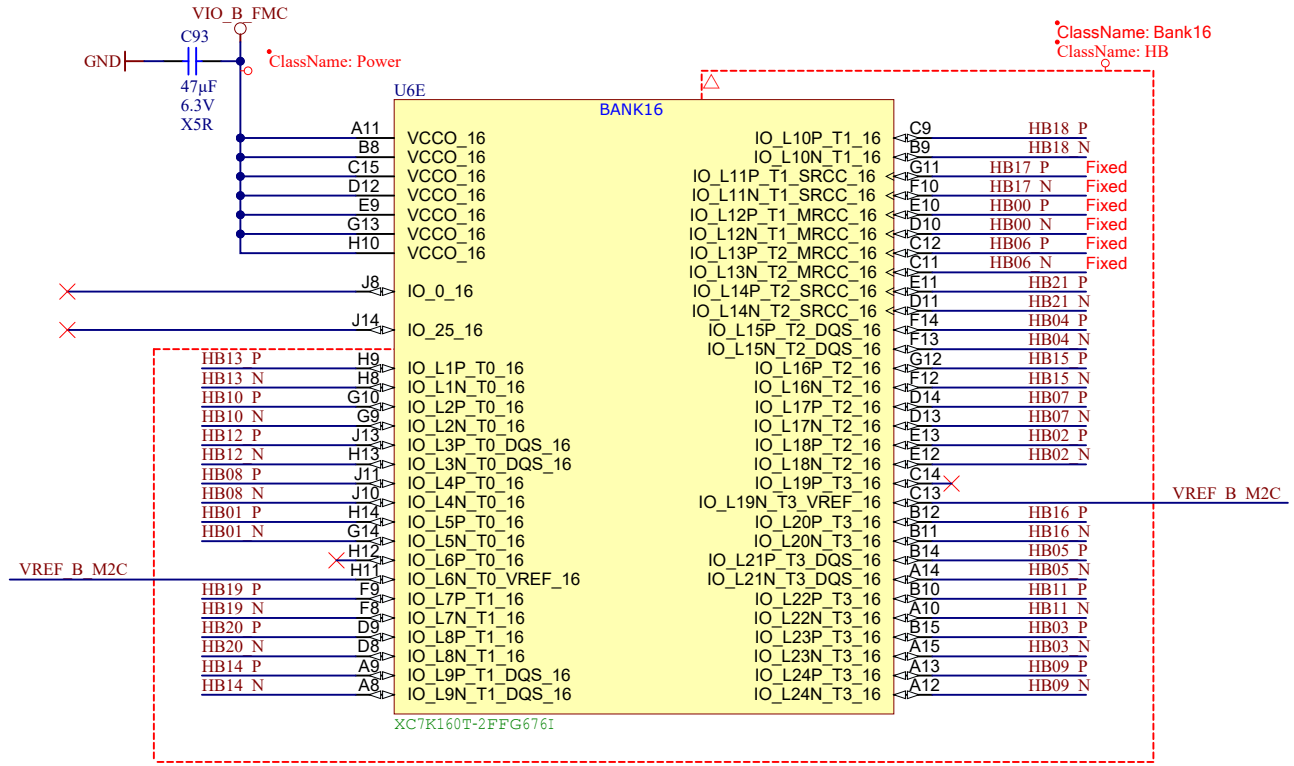
Title: TEF1001 - FPGA_BANK_13			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page12 of 33
Filename: FPGA_BANK_13.SchDoc			



trenz electronic	Title: TEF1001 - FPGA_BANK_14		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page13 of 33
Filename: FPGA_BANK_14.SchDoc			



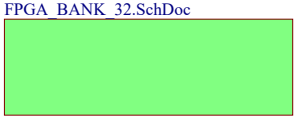
Title: TEF1001 - FPGA_BANK_15			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page14 of 33
Filename: FPGA_BANK_15.SchDoc			



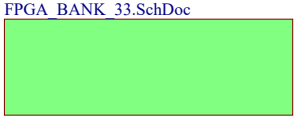
trenz electronic

Title: TEF1001 - FPGA_BANK_16		
A4	Number: TEF1001 B2IX4-F	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page15 of 33
Filename: FPGA_BANK_16.SchDoc		

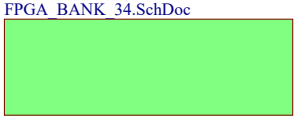
U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



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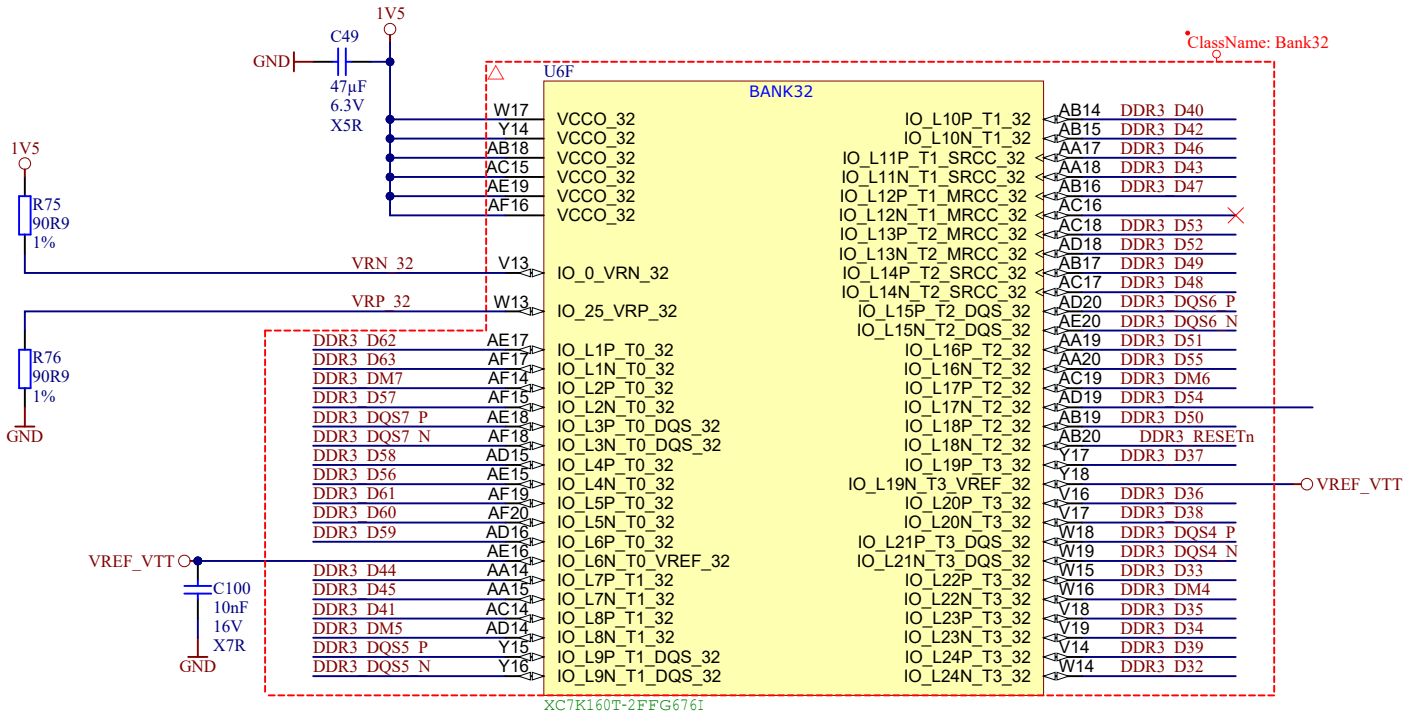
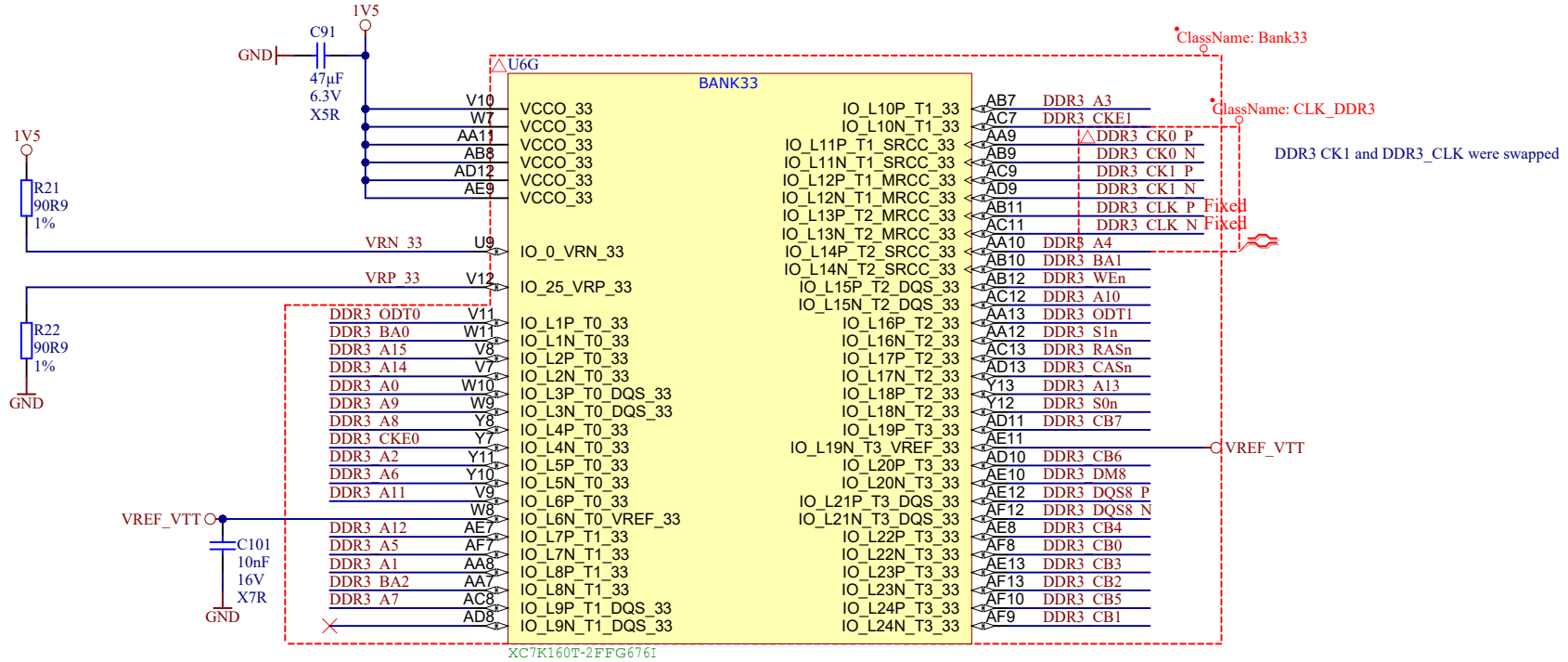
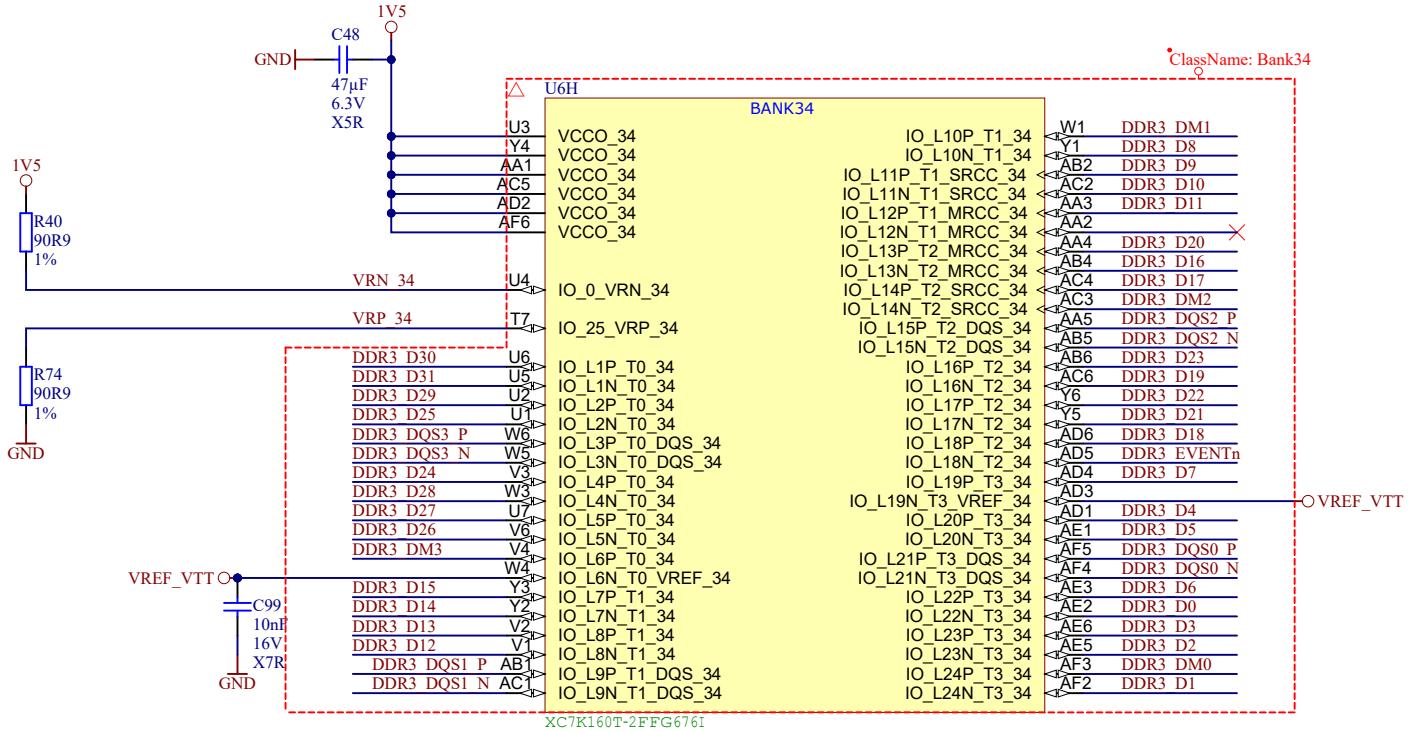
Title: TEF1001 - DDR_BANKS		
A4	Number: TEF1001 B2IX4-F	Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page16 of 33
Filename: DDR_Banks.SchDoc		



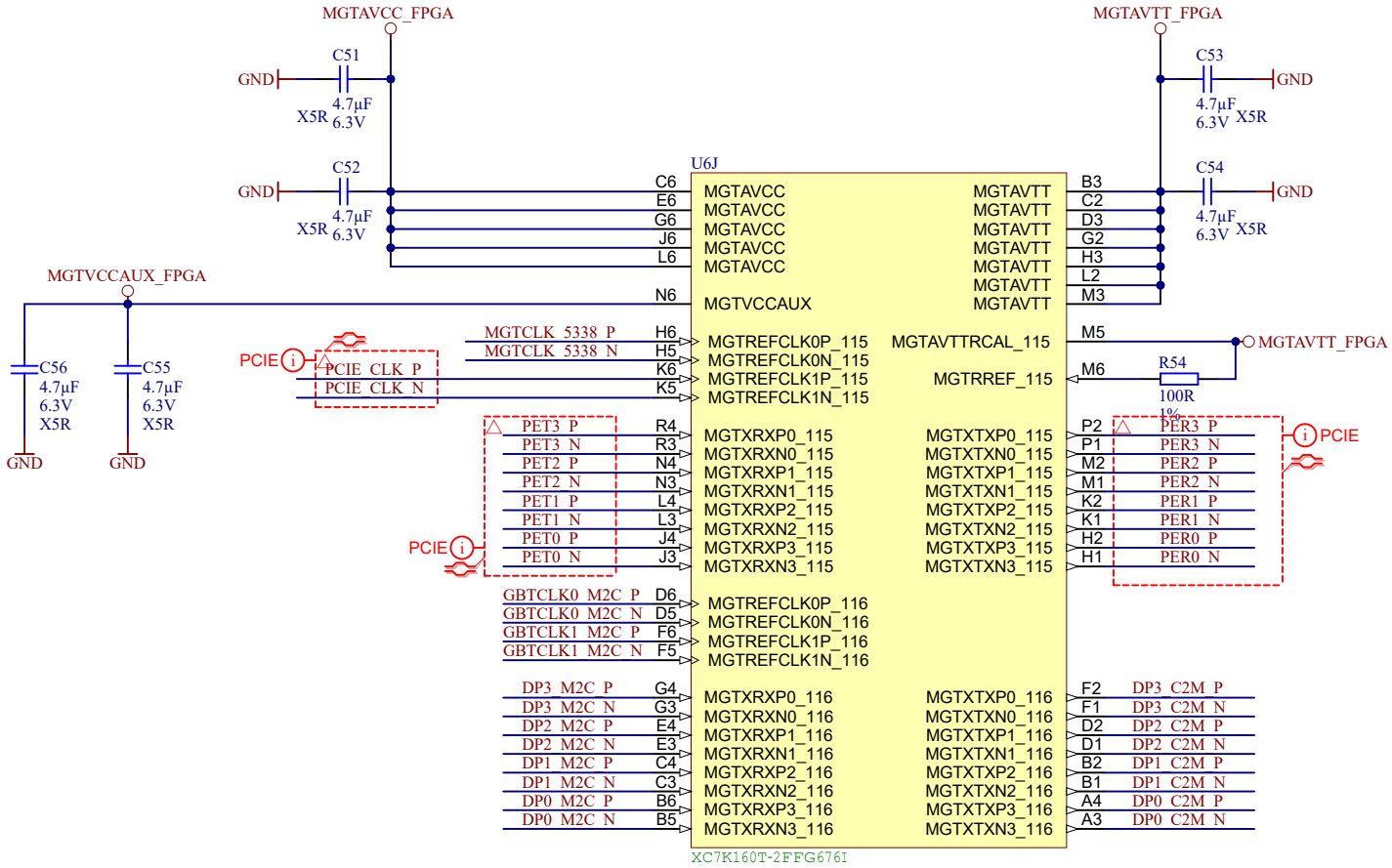
trenz electronic	Title: TEF1001 - FPGA_BANK_32		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page17 of 33
Filename: FPGA_BANK_32.SchDoc			



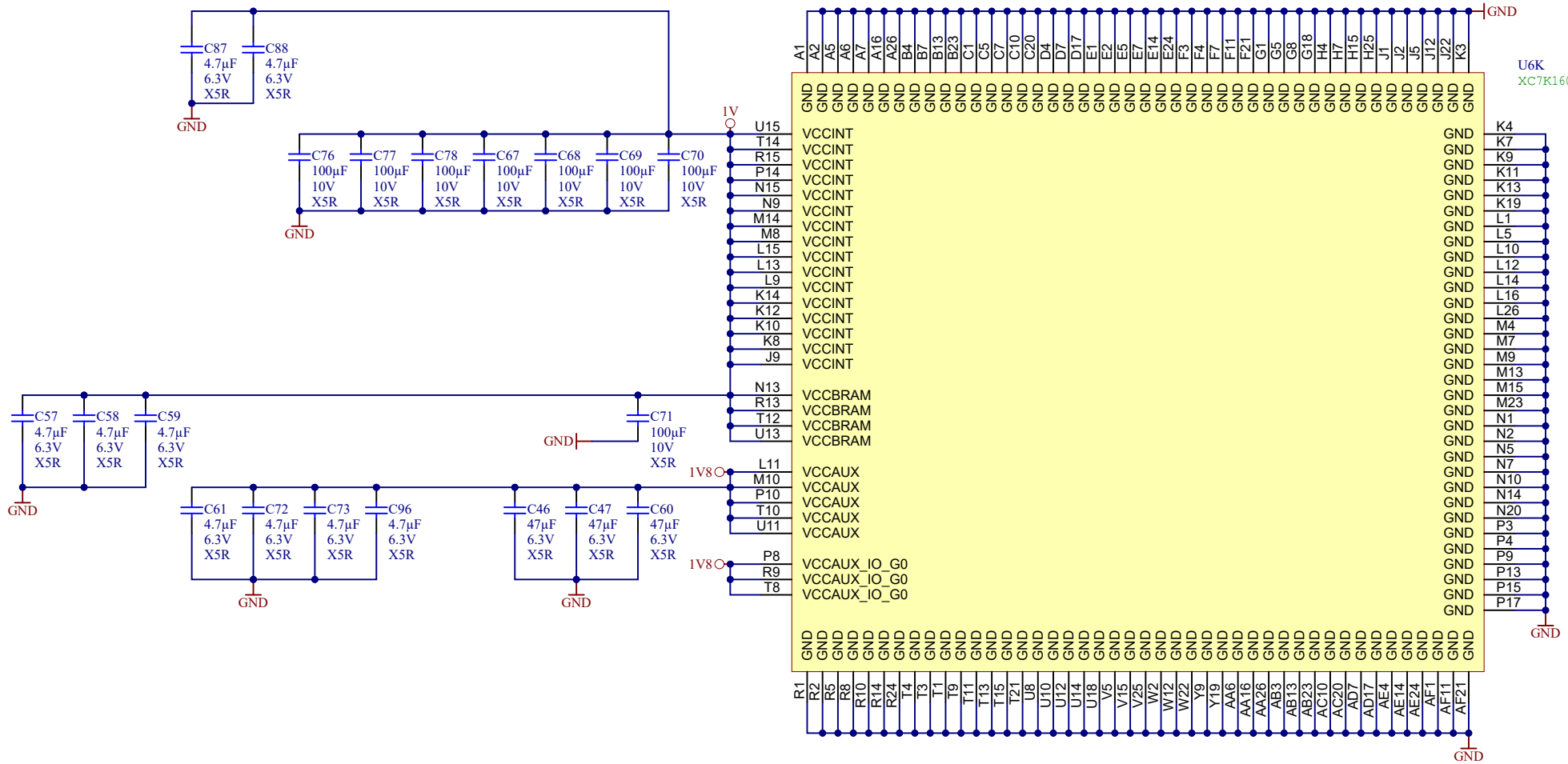
trenz electronic	Title: TEF1001 - FPGA_BANK_33		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page 18 of 33
Filename: FPGA_BANK_33.SchDoc			



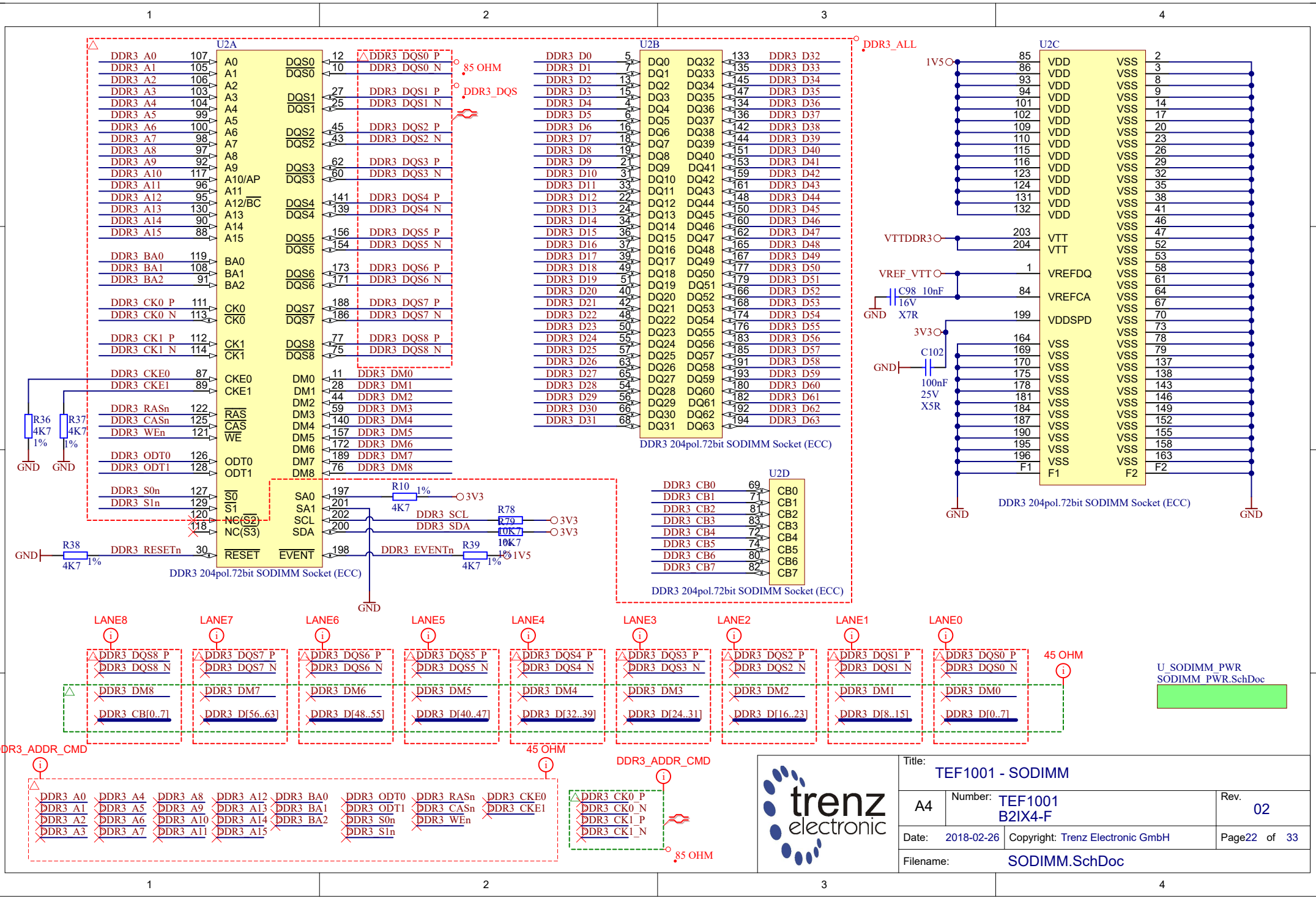
trenz electronic	Title: TEF1001 - FPGA_BANK_34		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page19 of 33
Filename: FPGA_BANK_34.SchDoc			



trenz electronic	Title: TEF1001_FPGA_MGT_BANKS		
	A4	Number: TEF1001 B2IX4-F	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page20 of 33
	Filename: FPGA_MGT_BANKS.SchDoc		



Title: TEF1001 - FPGA_POWER			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page21 of 33
Filename: FPGA_POWER.SchDoc			


U2A
DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14 DDR3_A15
DDR3_BA0 DDR3_BA1 DDR3_BA2
DDR3_CK0_P DDR3_CK0_N DDR3_CK1_P DDR3_CK1_N
DDR3_CKE0 DDR3_CKE1
DDR3_RASn DDR3_CASn DDR3_WEn
DDR3_ODT0 DDR3_ODT1
DDR3_S0n DDR3_S1n
DDR3_RESETn
DDR3_DQS0_P DDR3_DQS0_N DDR3_DQS1_P DDR3_DQS1_N DDR3_DQS2_P DDR3_DQS2_N DDR3_DQS3_P DDR3_DQS3_N DDR3_DQS4_P DDR3_DQS4_N DDR3_DQS5_P DDR3_DQS5_N DDR3_DQS6_P DDR3_DQS6_N DDR3_DQS7_P DDR3_DQS7_N DDR3_DQS8_P DDR3_DQS8_N
DDR3_DM0 DDR3_DM1 DDR3_DM2 DDR3_DM3 DDR3_DM4 DDR3_DM5 DDR3_DM6 DDR3_DM7 DDR3_DM8
DDR3 204pol.72bit SODIMM Socket (ECC)
85 OHM
DDR3_DQS
R36 4K7 1%
R37 4K7 1%
GND
R38 4K7 1%
R10 4K7 1%
3V3
DDR3_SCL
DDR3_SDA
R78 10K7
R79 10K7
R39 4K7 1%
1V5
DDR3_EVENTn
U2B
DDR3_D0 DDR3_D1 DDR3_D2 DDR3_D3 DDR3_D4 DDR3_D5 DDR3_D6 DDR3_D7 DDR3_D8 DDR3_D9 DDR3_D10 DDR3_D11 DDR3_D12 DDR3_D13 DDR3_D14 DDR3_D15 DDR3_D16 DDR3_D17 DDR3_D18 DDR3_D19 DDR3_D20 DDR3_D21 DDR3_D22 DDR3_D23 DDR3_D24 DDR3_D25 DDR3_D26 DDR3_D27 DDR3_D28 DDR3_D29 DDR3_D30 DDR3_D31
DDR3_D32 DDR3_D33 DDR3_D34 DDR3_D35 DDR3_D36 DDR3_D37 DDR3_D38 DDR3_D39 DDR3_D40 DDR3_D41 DDR3_D42 DDR3_D43 DDR3_D44 DDR3_D45 DDR3_D46 DDR3_D47 DDR3_D48 DDR3_D49 DDR3_D50 DDR3_D51 DDR3_D52 DDR3_D53 DDR3_D54 DDR3_D55 DDR3_D56 DDR3_D57 DDR3_D58 DDR3_D59 DDR3_D60 DDR3_D61 DDR3_D62 DDR3_D63
DDR3 204pol.72bit SODIMM Socket (ECC)
U2D
DDR3_CB0 DDR3_CB1 DDR3_CB2 DDR3_CB3 DDR3_CB4 DDR3_CB5 DDR3_CB6 DDR3_CB7
DDR3 204pol.72bit SODIMM Socket (ECC)
DDR3_ALL
U2C
1V5
VTTDDR3
VREF_VTT
C98 10nF 16V X7R
3V3
C102 100nF 25V X5R
VDD VSS VTT VREFDQ VREFCA VDDSPD F1 F2
DDR3 204pol.72bit SODIMM Socket (ECC)
LANE8 LANE7 LANE6 LANE5 LANE4 LANE3 LANE2 LANE1 LANE0
45 OHM
U_SODIMM_PWR
SODIMM_PWR.SchDoc
DDR3_ADDR_CMD
DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14 DDR3_A15 DDR3_BA0 DDR3_BA1 DDR3_BA2 DDR3_ODT0 DDR3_ODT1 DDR3_S0n DDR3_S1n DDR3_RASn DDR3_CASn DDR3_WEn DDR3_CKE0 DDR3_CKE1
45 OHM
DDR3_ADDR_CMD
DDR3_CK0_P DDR3_CK0_N DDR3_CK1_P DDR3_CK1_N
85 OHM
trenz electronic
Title: TEF1001 - SODIMM
A4
Number: TEF1001 B2IX4-F
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
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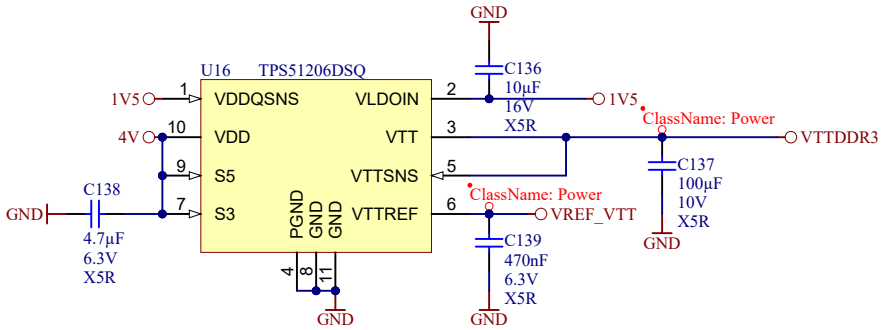
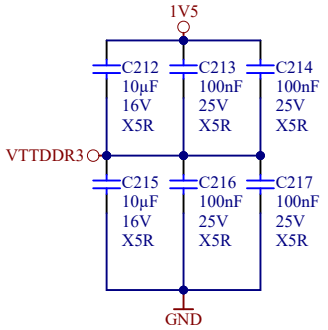
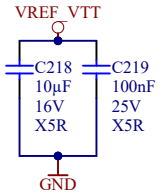
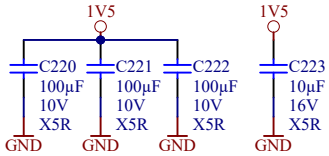
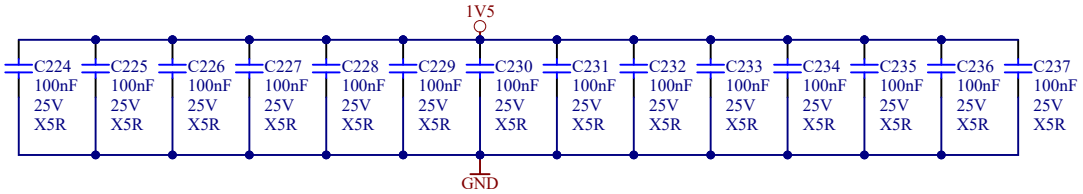
Filename: SODIMM.SchDoc











Title: TEF1001 - SODIMM_PWR			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page23 of 33
Filename: SODIMM_PWR.SchDoc			

U_PWR_4V_1V5
PWR_4V_1V5.SchDoc

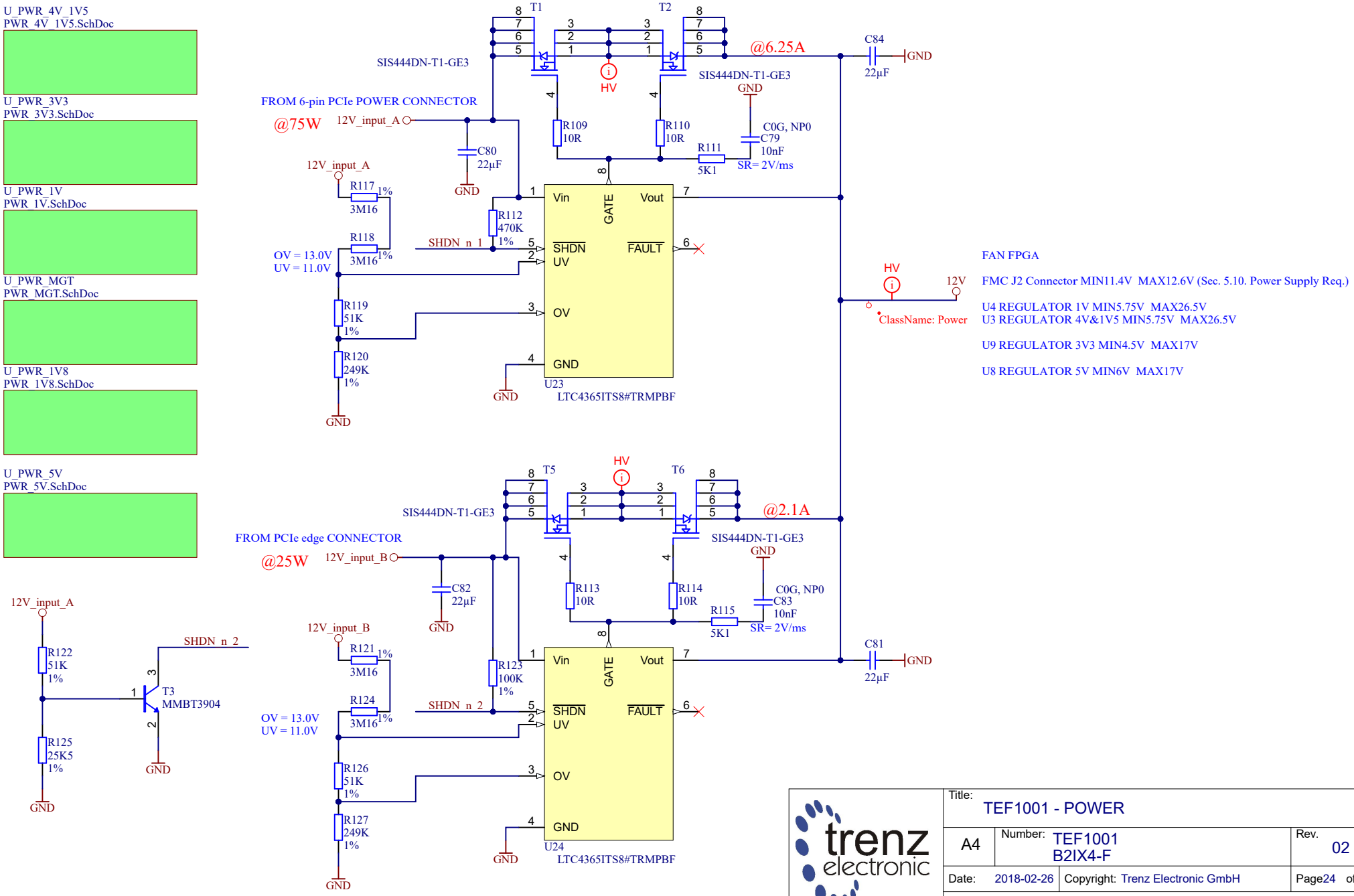
U_PWR_3V3
PWR_3V3.SchDoc

U_PWR_1V
PWR_1V.SchDoc

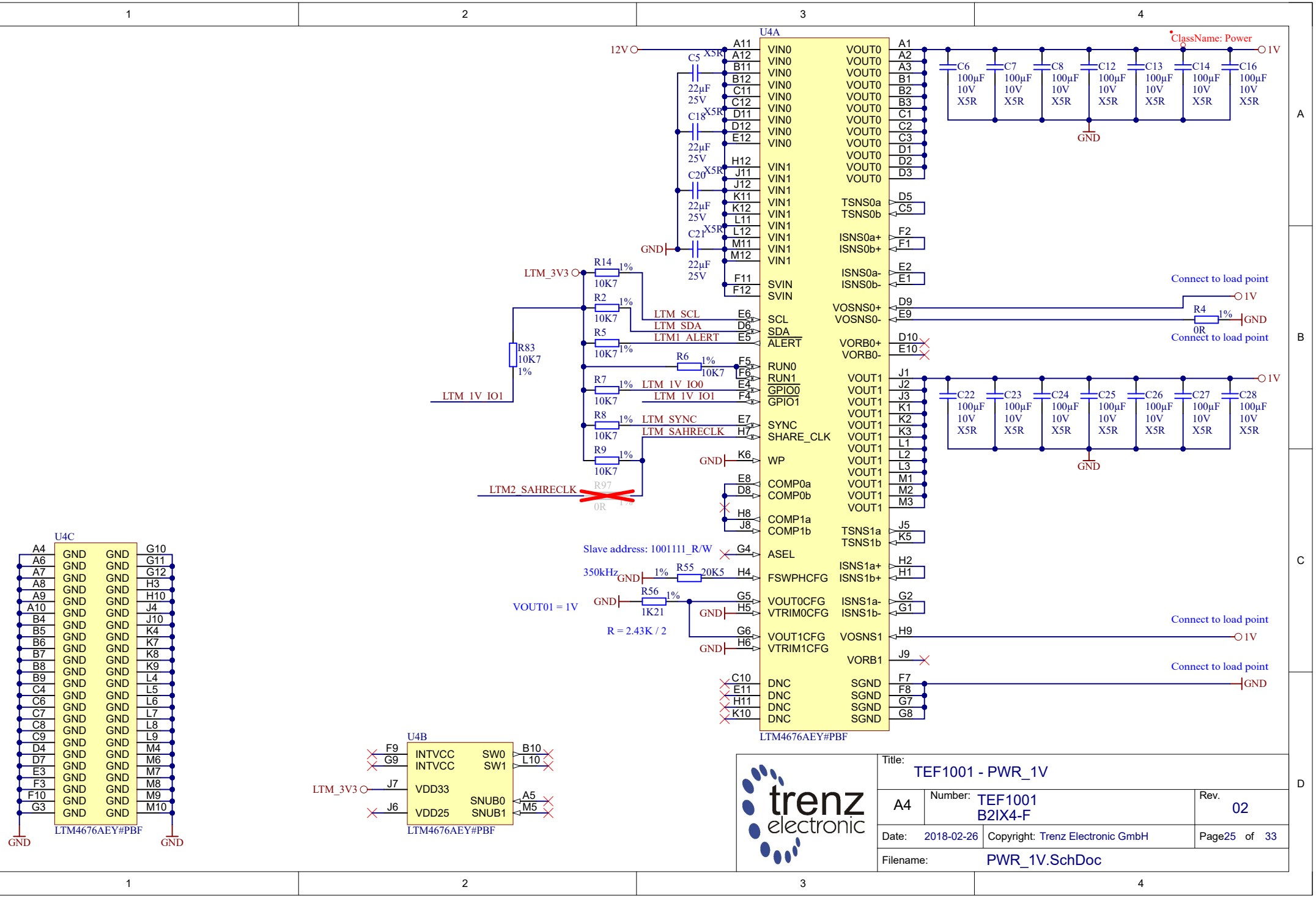
U_PWR_MGT
PWR_MGT.SchDoc

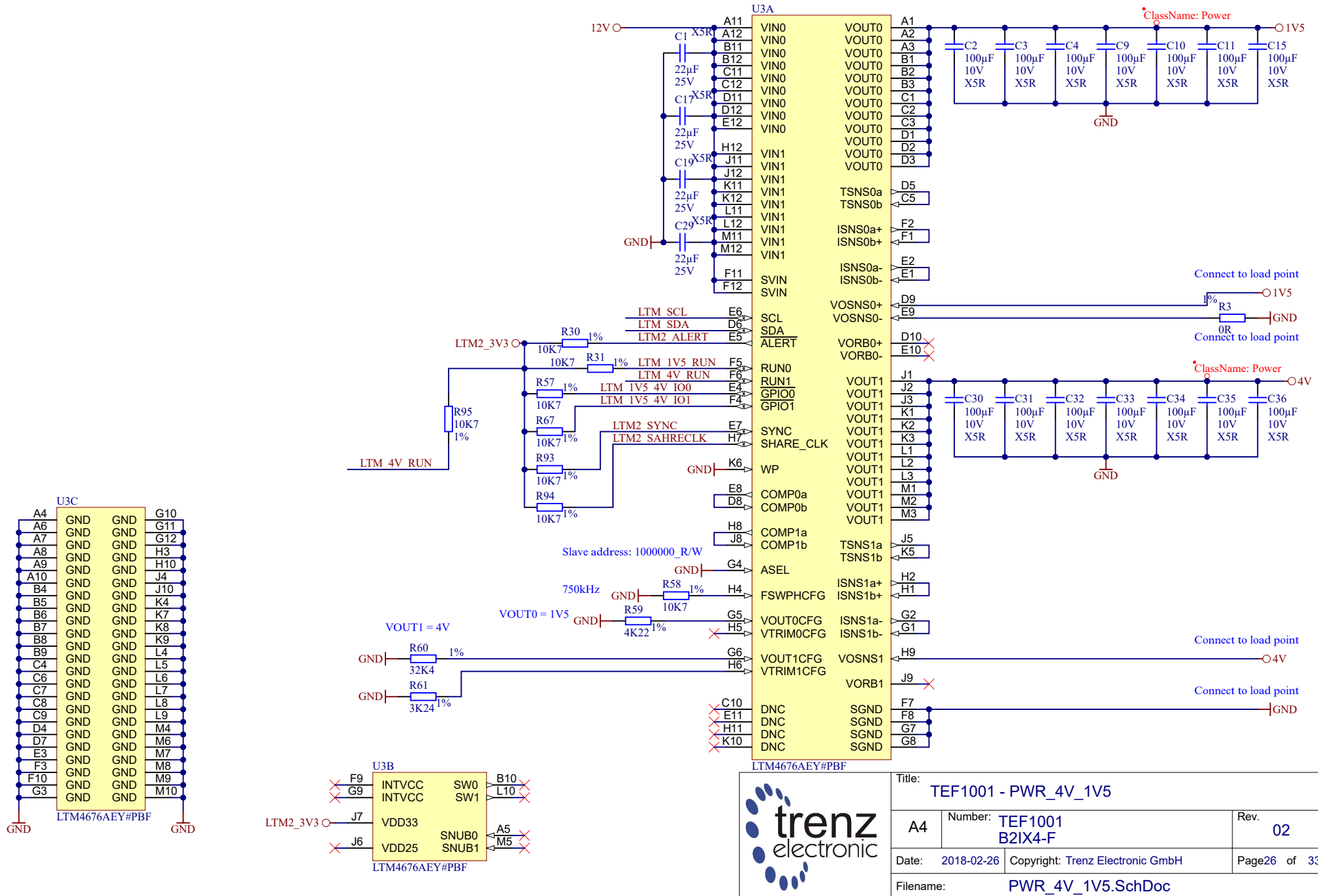
U_PWR_1V8
PWR_1V8.SchDoc

U_PWR_5V
PWR_5V.SchDoc



Title: TEF1001 - POWER			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page24 of 33
Filename: POWER.SchDoc			


U4A
LTM4676AEY#PBF
U4C
LTM4676AEY#PBF
U4B
LTM4676AEY#PBF
12V
LTM_3V3
GND
LTM_SCL
LTM_SDA
LTM1_ALERT
LTM_1V_IO1
LTM_1V_IO0
LTM_SYNC
LTM_SAHRECLK
LTM2_SAHRECLK
Slave address: 1001111_R/W
350kHz
VOUT01 = 1V
R = 2.43K / 2
ClassName: Power
1V
Connect to load point
Title: TEF1001 - PWR_1V
A4
Number: TEF1001 B2IX4-F
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page25 of 33
Filename: PWR_1V.SchDoc


U3A
LTM4676AEY#PBF
U3C
LTM4676AEY#PBF
U3B
LTM4676AEY#PBF
12V
1V5
4V
GND
LTM2_3V3
LTM_4V_RUN
LTM_SCL
LTM_SDA
LTM2_ALERT
LTM_1V5_RUN
LTM_4V_RUN
LTM_1V5_4V_IO0
LTM_1V5_4V_IO1
LTM2_SYNC
LTM2_SAHRECLK
Slave address: 1000000_R/W
750kHz
VOUT0 = 1V5
VOUT1 = 4V
ClassName: Power
Connect to load point
Title: TEF1001 - PWR_4V_1V5
A4
Number: TEF1001 B2IX4-F
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
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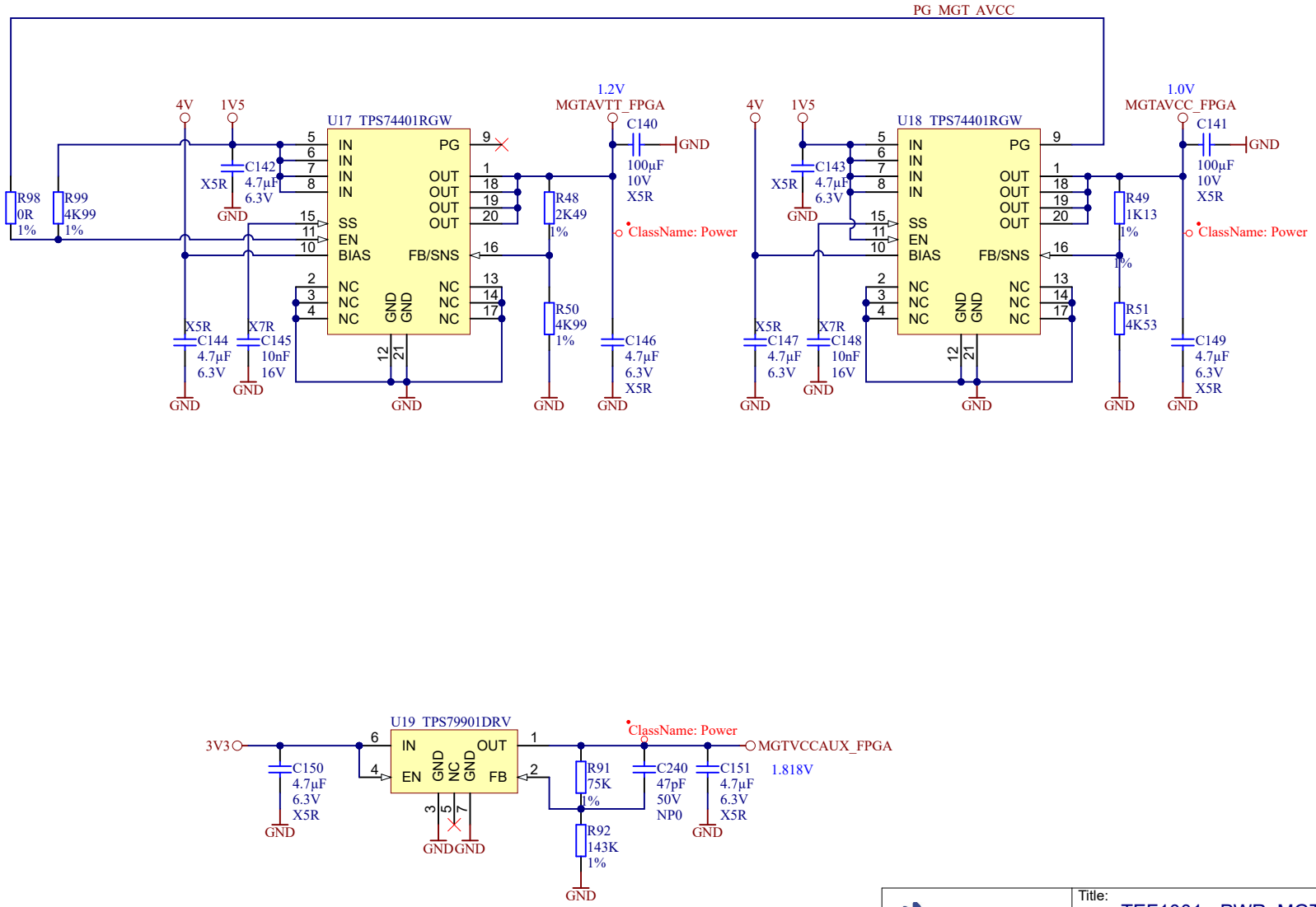
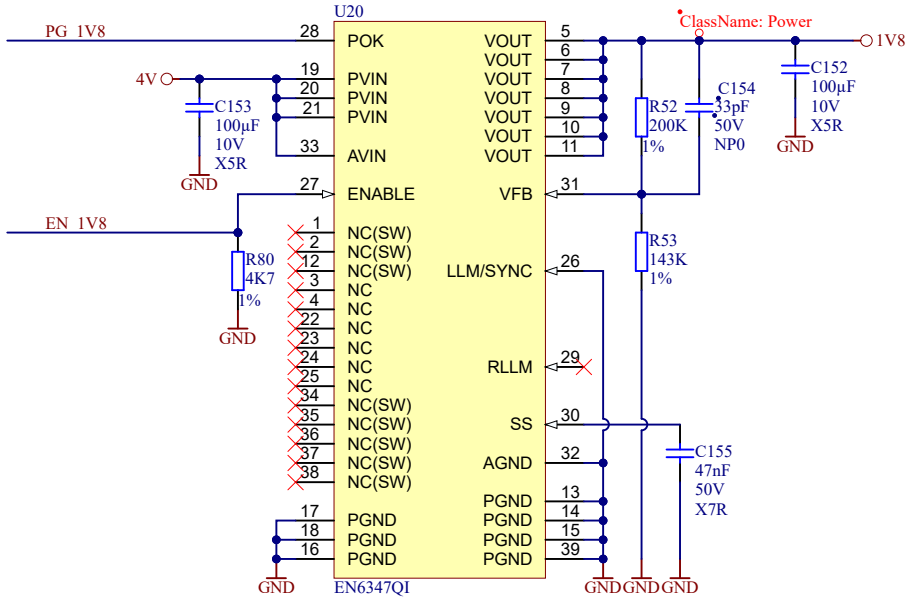
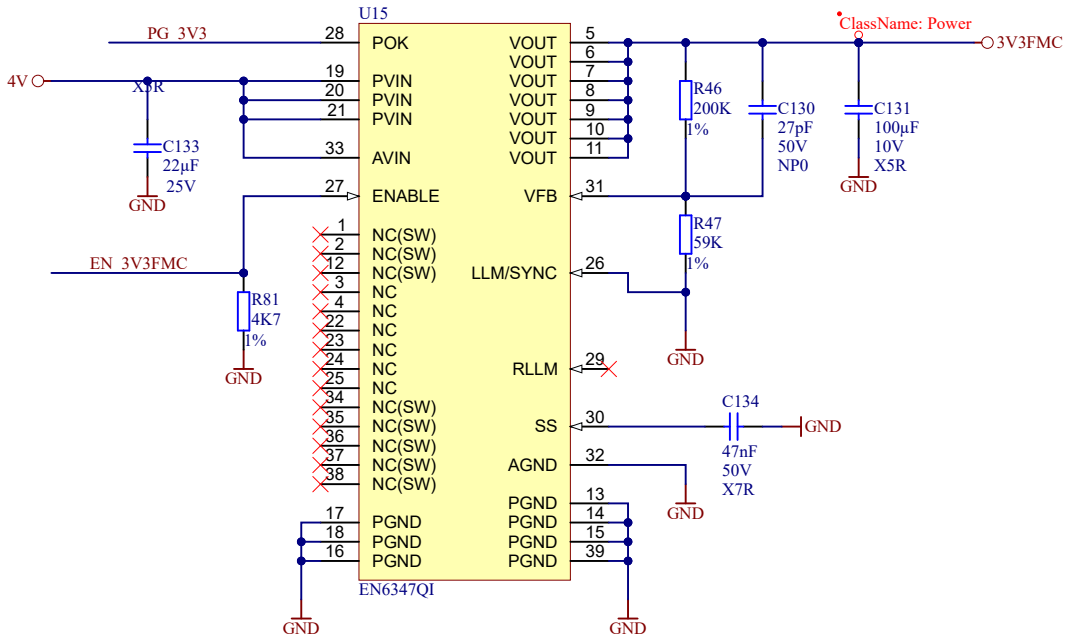
Filename: PWR_4V_1V5.SchDoc

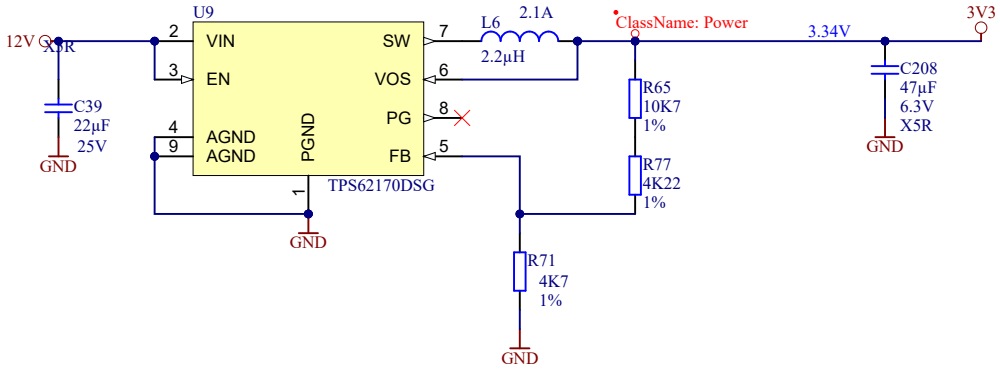


Title: TEF1001 - PWR_MGT			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page27 of 33
Filename: PWR_MGT.SchDoc			

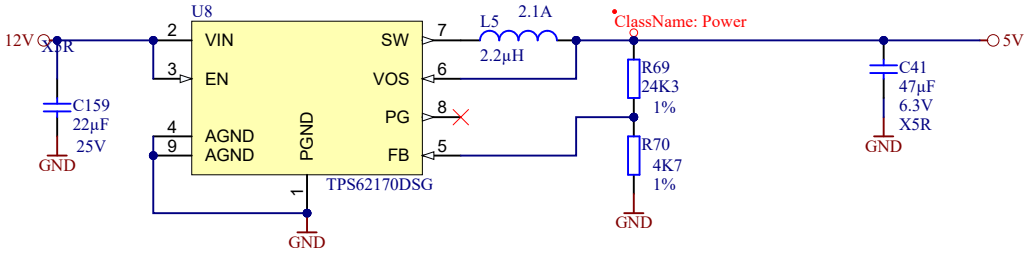


trenz electronic	Title: TEF1001 - PWR_1V8		
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page28 of 33
Filename: PWR_1V8.SchDoc			

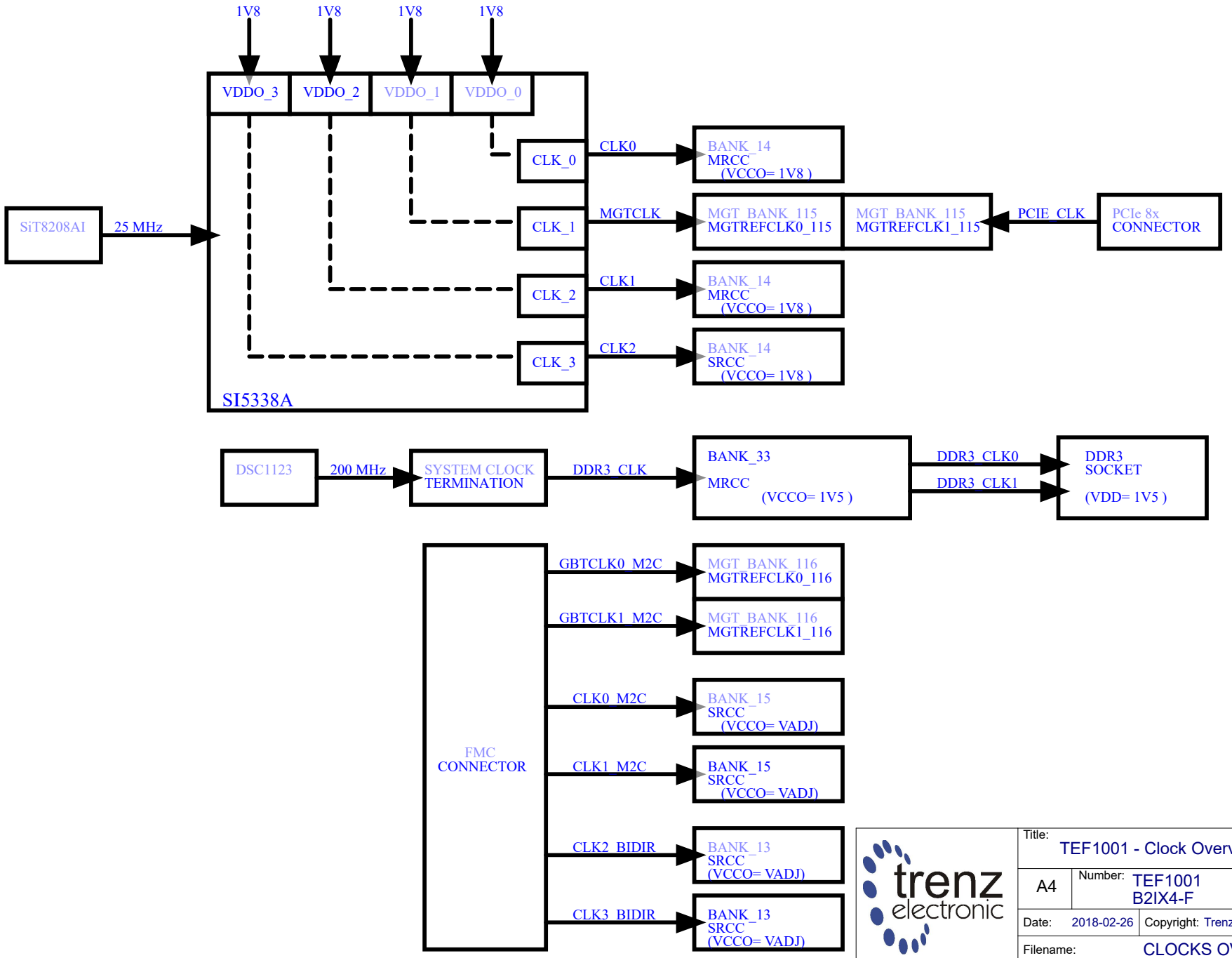




Title: TEF1001 - PWR_3V3			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page29 of 33
Filename: PWR_3V3.SchDoc			



Title: TEF1001 - PWR_5V			
A4	Number: TEF1001 B2IX4-F		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page30 of 33
Filename: PWR_5V.SchDoc			



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Title: TEF1001 - Clock Overview			
A4	Number: TEF1001 B2IX4-F		Rev. 02
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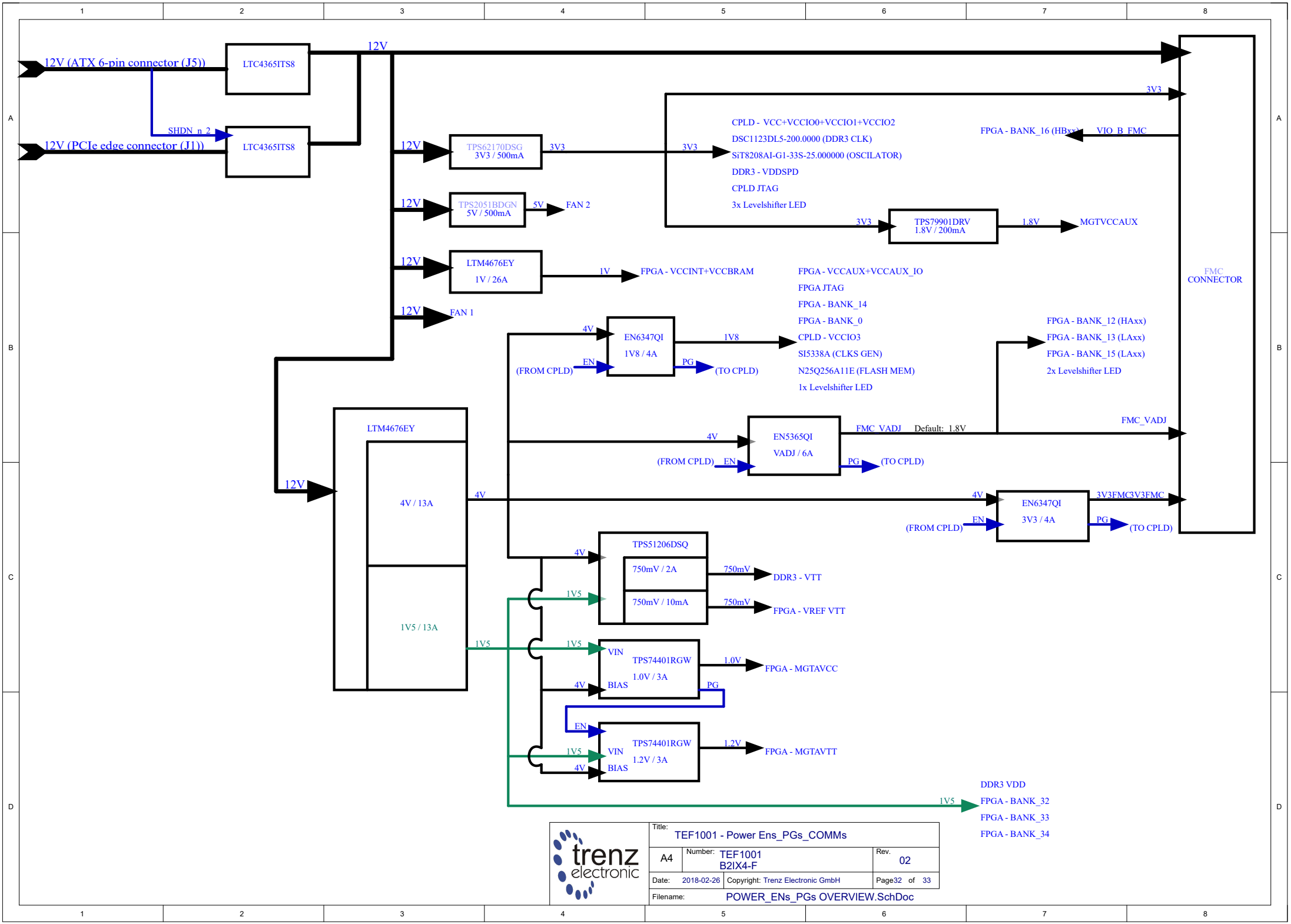
Filename: CLOCKS OVERVIEW.SchDoc			



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Title: TEF1001 - Power Ens_PGs_COMMs		
A4	Number: TEF1001 B2IX4-F	Rev. 02
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Filename: POWER_ENs_PGs OVERVIEW.SchDoc		

Revision 02:
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1) added C87, C88 4.7µF
2) C154 incremented from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)

Revision 02a (2020-04-15):
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1) VY: New FAN M1, F455B-05MD replaced by F455B-05LD

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Title: TEF1001 - Revision history			
A4	Number: TEF1001 B2IX4-F		Rev. 02
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Filename: Revision_Changes.SchDoc			