

1

2

3

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A

A

U\_FPGA  
FPGA.SchDoc

Special notes:



U\_SODIMM  
SODIMM.SchDoc



U\_CLOCK  
CLOCK.SchDoc



U\_POWER  
POWER.SchDoc



U\_CONN  
CONN.SchDoc



U\_CPLD  
CPLD.SchDoc



B

B

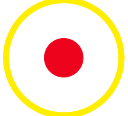
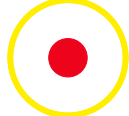
C

C

PM1

PM2

PM3



FIDU-DOT - small

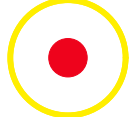
FIDU-DOT - small

FIDU-DOT - small

PM4

PM5

PM6

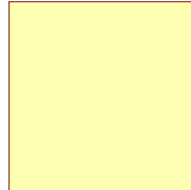


FIDU-DOT - small

FIDU-DOT - small

FIDU-DOT - small

Front Bracket screw head on Top  
MECH1



Slotblende Ndigo xTDC4 Lemo

Front Bracket screw head on Bottom  
MECH2



TEF1001 PCIe Frontplate

D

D

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT



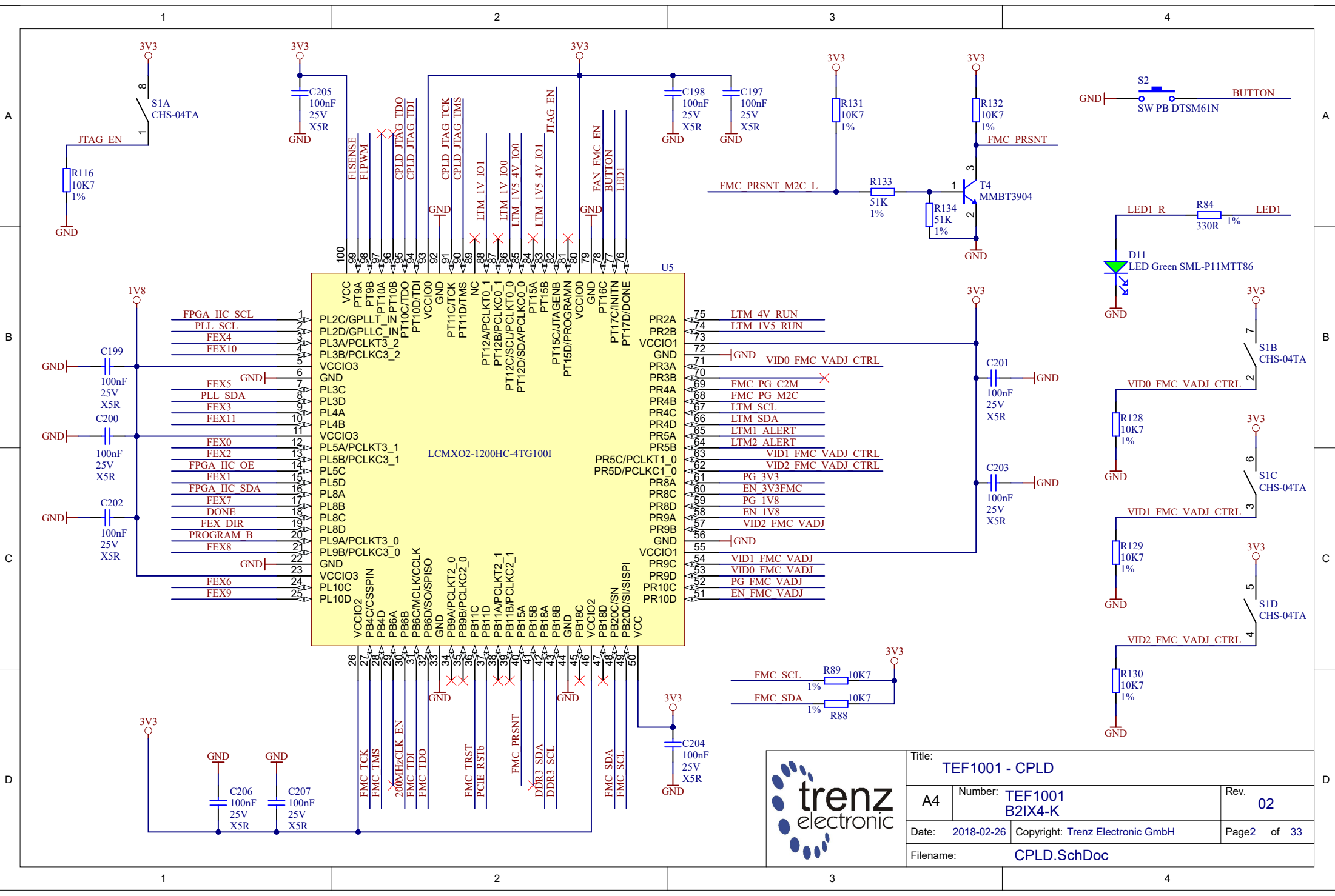
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| Title: TEF1001 - MAIN    |                                  |             |
| A4                       | Number: TEF1001 B2IX4-K          | Rev. 02     |
| Date: 2018-02-26         | Copyright: Trenz Electronic GmbH | Page1 of 33 |
| Filename: TEF1001.SchDoc |                                  |             |

1

2

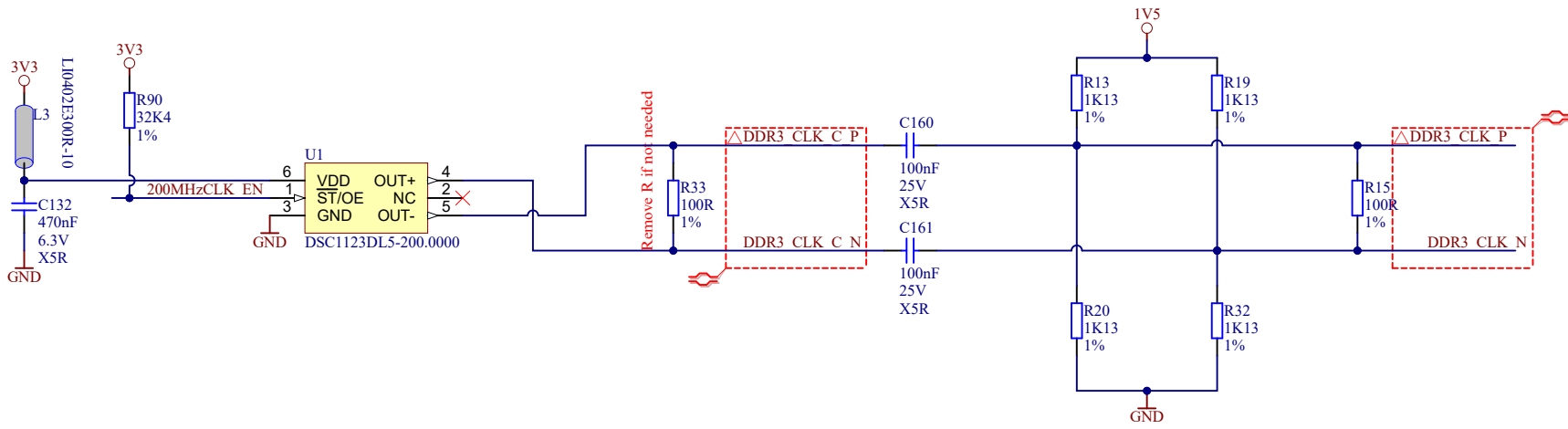
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4

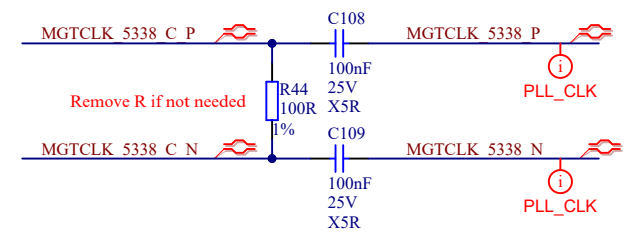
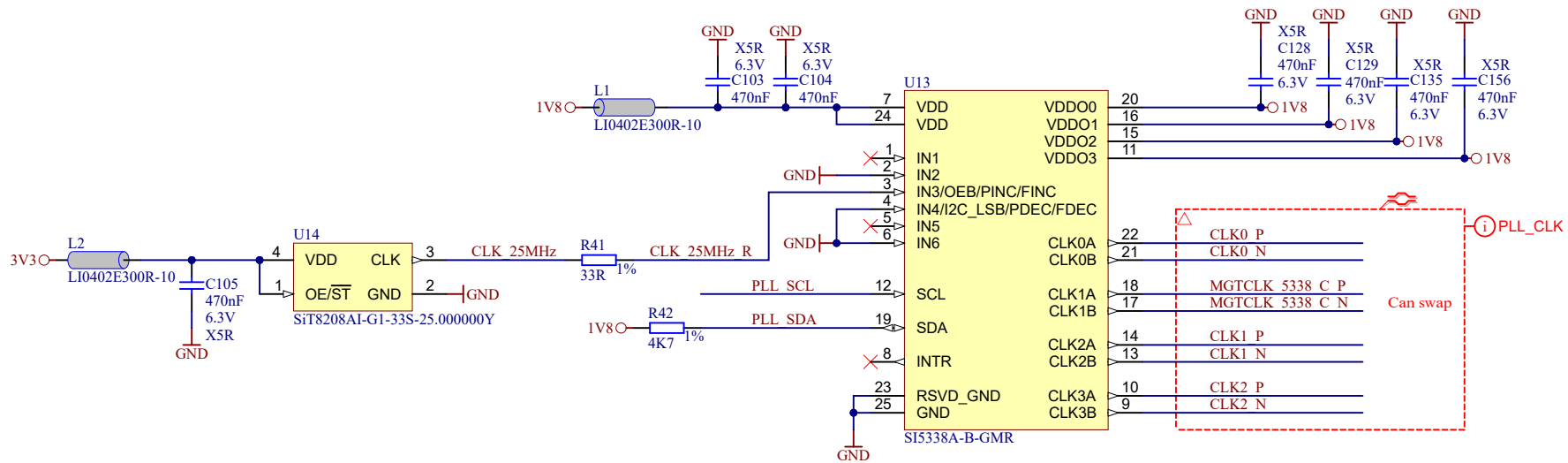



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| Title: TEF1001 - CPLD |                                  |             |
| A4                    | Number: TEF1001 B2IX4-K          | Rev. 02     |
| Date: 2018-02-26      | Copyright: Trenz Electronic GmbH | Page2 of 33 |
| Filename: CPLD.SchDoc |                                  |             |

U\_CLK-SI5338  
CLK-SI5338.SchDoc



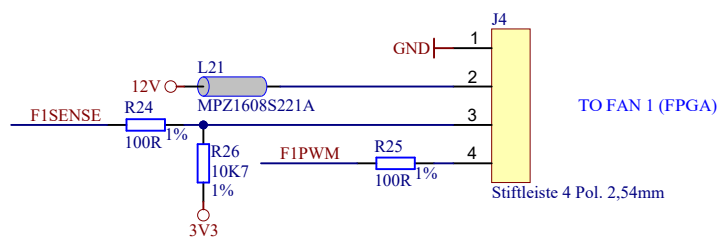
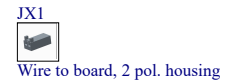
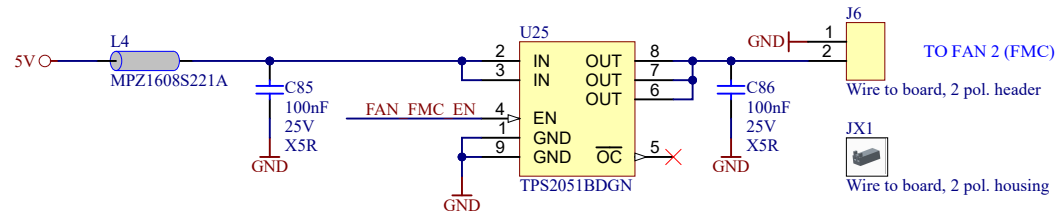
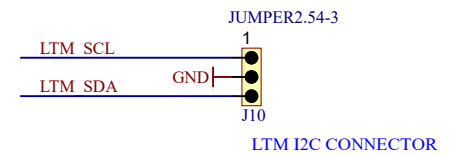
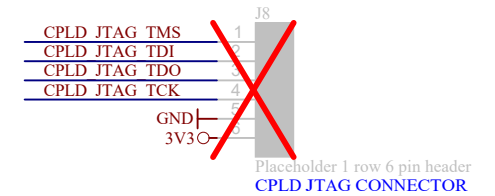
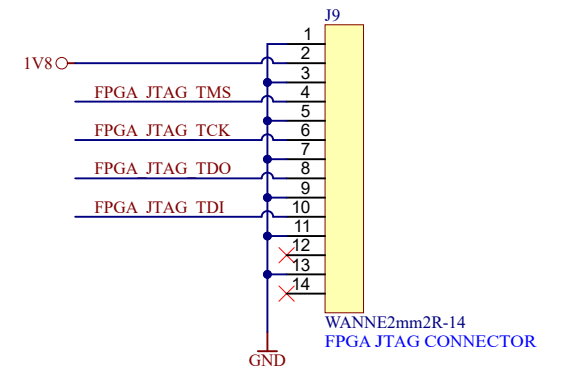
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|   |  |                                  | A4                     | Number: TEF1001<br>B2IX4-K |
| Date: 2018-02-26  |  | Copyright: Trenz Electronic GmbH |                        | Page3 of 33                |
| Filename: CLOCK.SchDoc  |  |                                  |                        |                            |



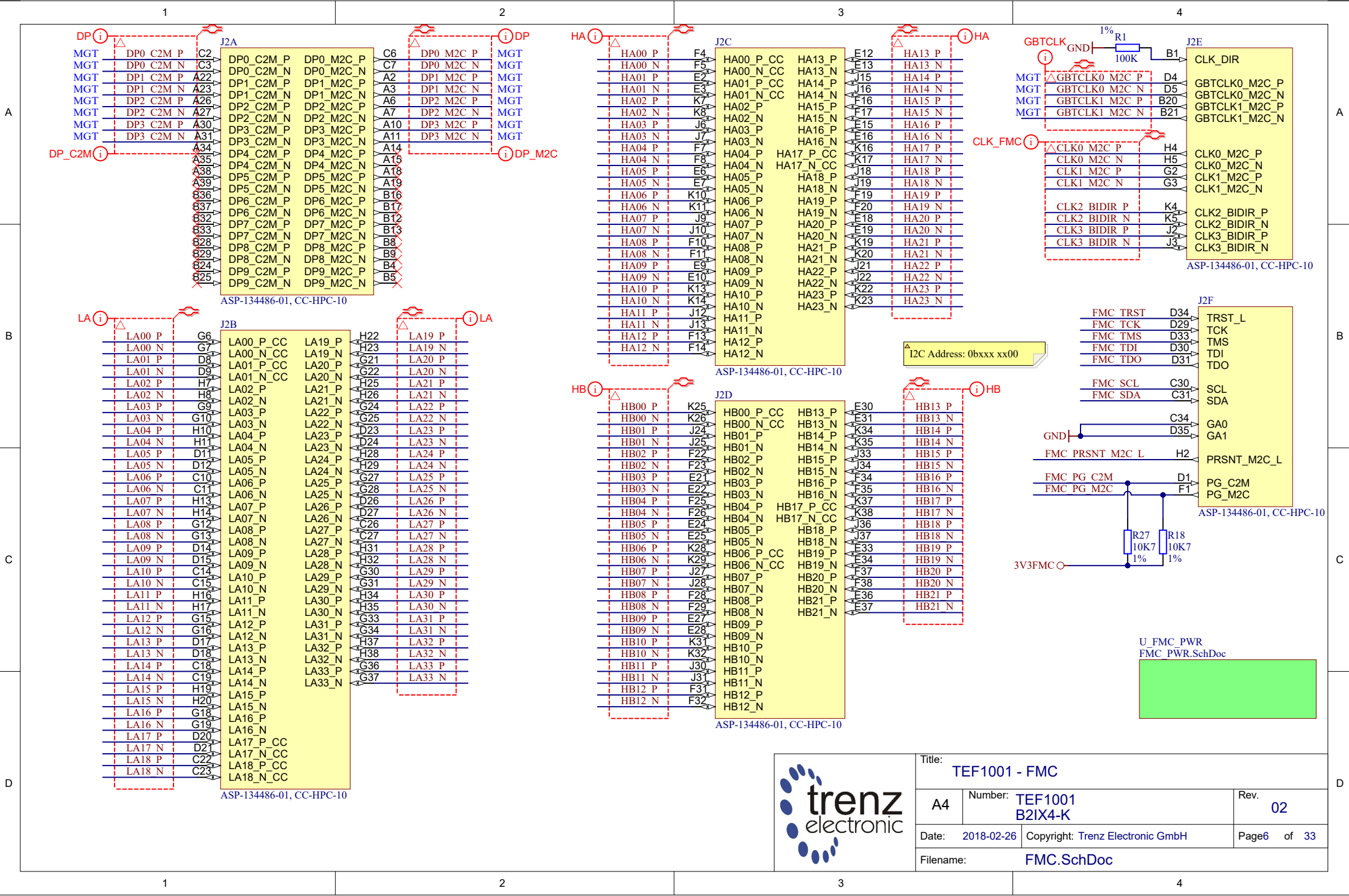
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|   |  | A4                               | Number: TEF1001 B2IX4-K |
| Date: 2018-02-26  |  | Copyright: Trenz Electronic GmbH |                         |
| Filename: CLK-SI5338.SchDoc   |  | Page4 of 33                      |                         |

U\_FMC  
FMC.SchDoc

U\_PCIE\_CONN  
PCIE\_CONN.SchDoc



|  |                              |   |                            |
|--|------------------------------|---|----------------------------|
|  | Title: <b>TEF1001 - CONN</b> |   |                            |
|  | A4                           | Number: <b>TEF1001 B2IX4-K</b>          | Rev. <b>02</b>             |
|  | Date: <b>2018-02-26</b>      | Copyright: <b>Trenz Electronic GmbH</b> | Page <b>5</b> of <b>33</b> |
|  | Filename: <b>CONN.SchDoc</b> |   |                            |



ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10

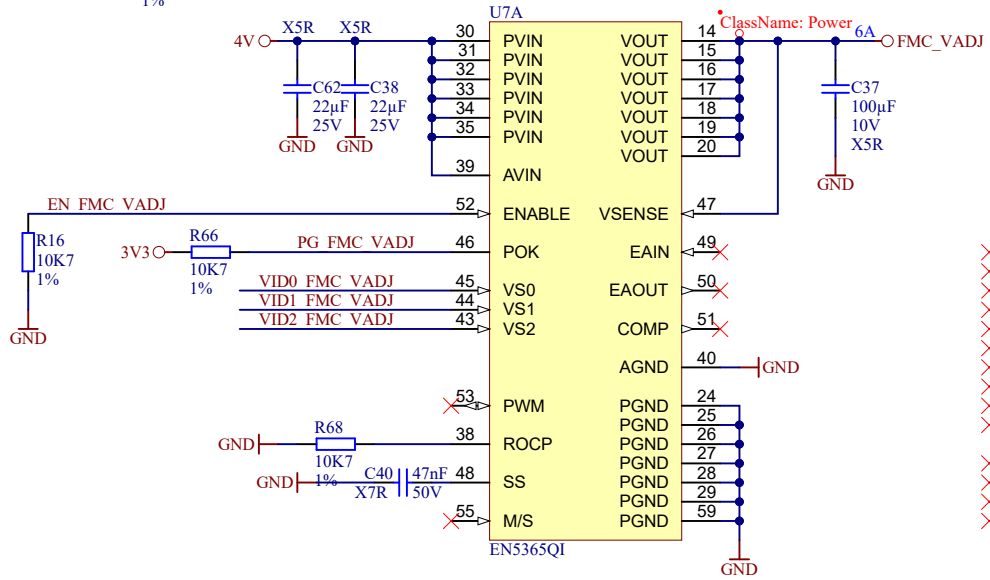
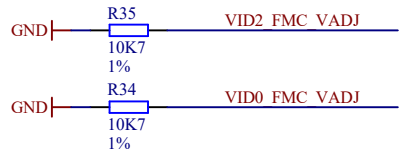
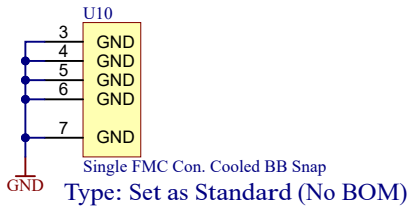
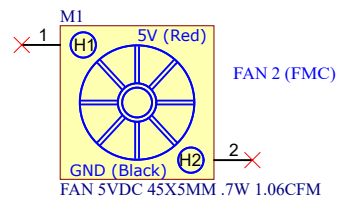
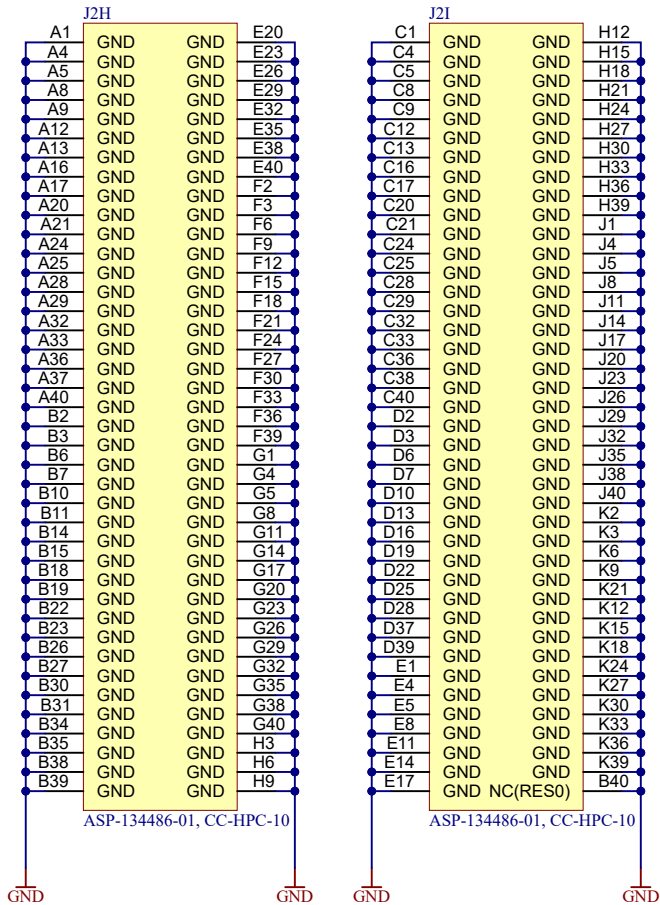
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ASP-134486-01, CC-HPC-10



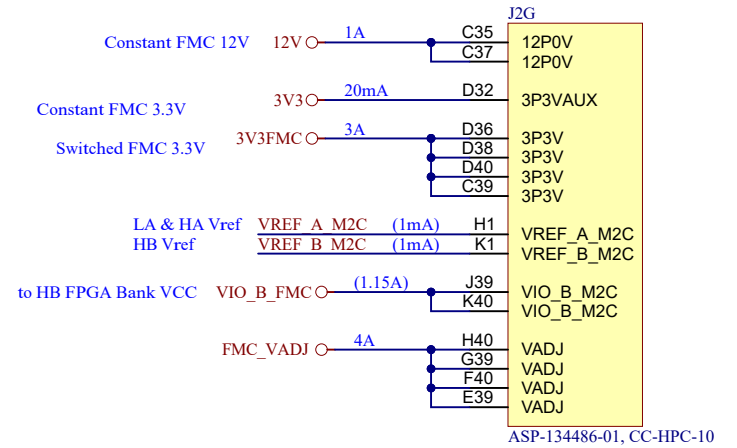
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| A4                   | Number: TEF1001 B2IX4-K          | Rev. 02     |
| Date: 2018-02-26     | Copyright: Trenz Electronic GmbH | Page6 of 33 |
| Filename: FMC.SchDoc |                                  |             |

U FMC\_PWR  
FMC\_PWR.SchDoc

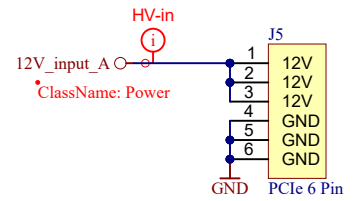
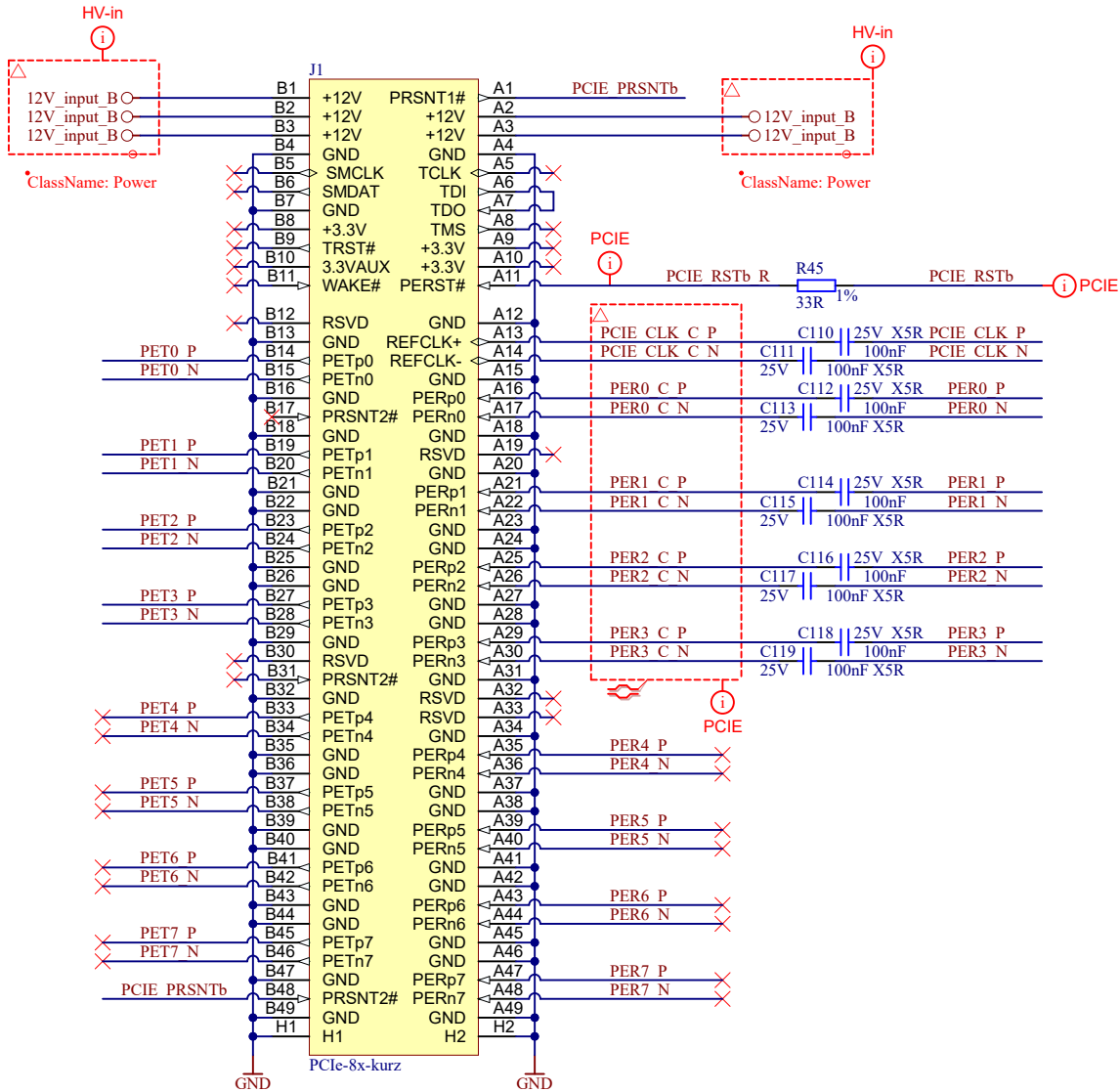



VS2 | VS1 | VS0 | Output Voltage

|   |   |   |       |
|---|---|---|-------|
| 0 | 0 | 0 | 3.3V  |
| 0 | 0 | 1 | 2.5V  |
| 0 | 1 | 0 | 1.8V  |
| 0 | 1 | 1 | 1.5V  |
| 1 | 0 | 0 | 1.25V |
| 1 | 0 | 1 | 1.2V  |



|                          |                                  |              |  |
|--------------------------|----------------------------------|--------------|--|
| Title: TEF1001 - FMC_PWR |                                  |              |  |
| A4                       | Number: TEF1001 B2IX4-K          | Rev. 02      |  |
| Date: 2018-02-26         | Copyright: Trenz Electronic GmbH | Page 7 of 33 |  |
| Filename: FMC_PWR.SchDoc |                                  |              |  |



|   |  |                                  |                                 |                         |
|---|--|----------------------------------|---------------------------------|-------------------------|
|  |  |                                  | Title: TEF1001 - PCIE CONNECTOR |                         |
|   |  |                                  | A4                              | Number: TEF1001 B2IX4-K |
| Date: 2018-02-26  |  | Copyright: Trenz Electronic GmbH |                                 | Page 8 of 33            |
| Filename: PCIE_CONN.SchDoc  |  |                                  |                                 |                         |



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U\_FPGA\_BANK\_12  
FPGA\_BANK\_12.SchDoc

U\_FPGA\_MGT\_BANKS  
FPGA\_MGT\_BANKS.SchDoc

U\_FPGA\_BANK\_13  
FPGA\_BANK\_13.SchDoc

U\_FPGA\_CFG  
FPGA\_CFG.SchDoc

U\_FPGA\_BANK\_14  
FPGA\_BANK\_14.SchDoc

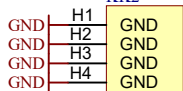
U\_DDR\_Banks  
DDR\_Banks.SchDoc

U\_FPGA\_BANK\_15  
FPGA\_BANK\_15.SchDoc

U\_FPGA\_POWER  
FPGA\_POWER.SchDoc

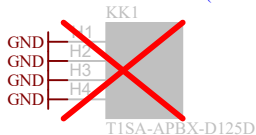
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FPGA\_BANK\_16.SchDoc

HEATSINK TYPE 2 (FPGA)  
KK2

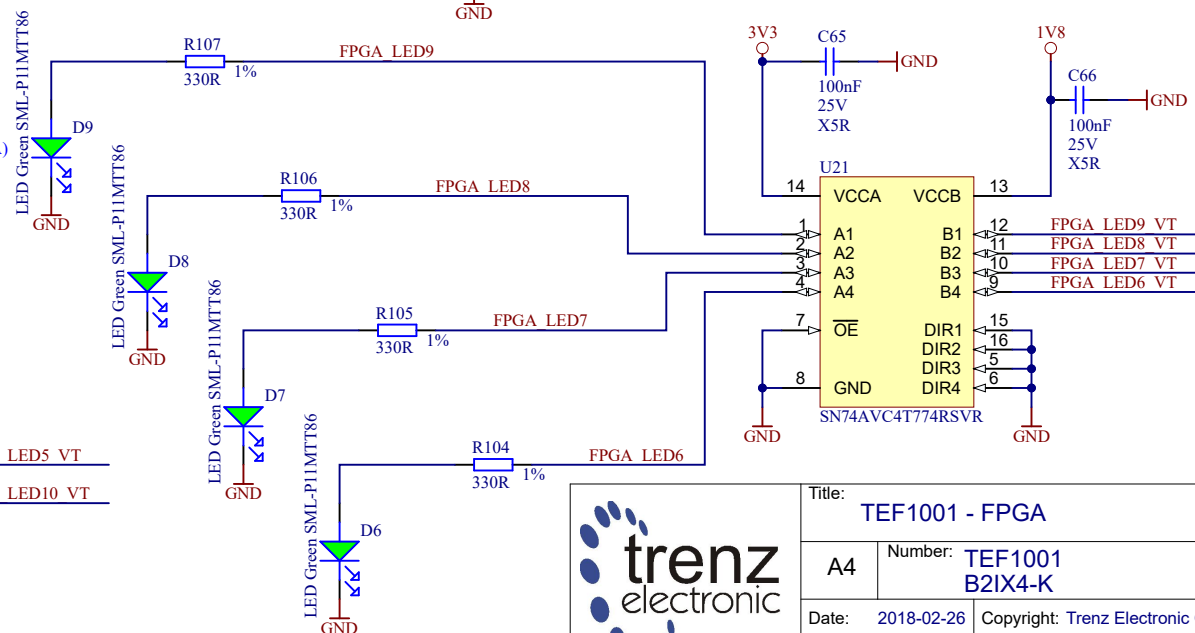
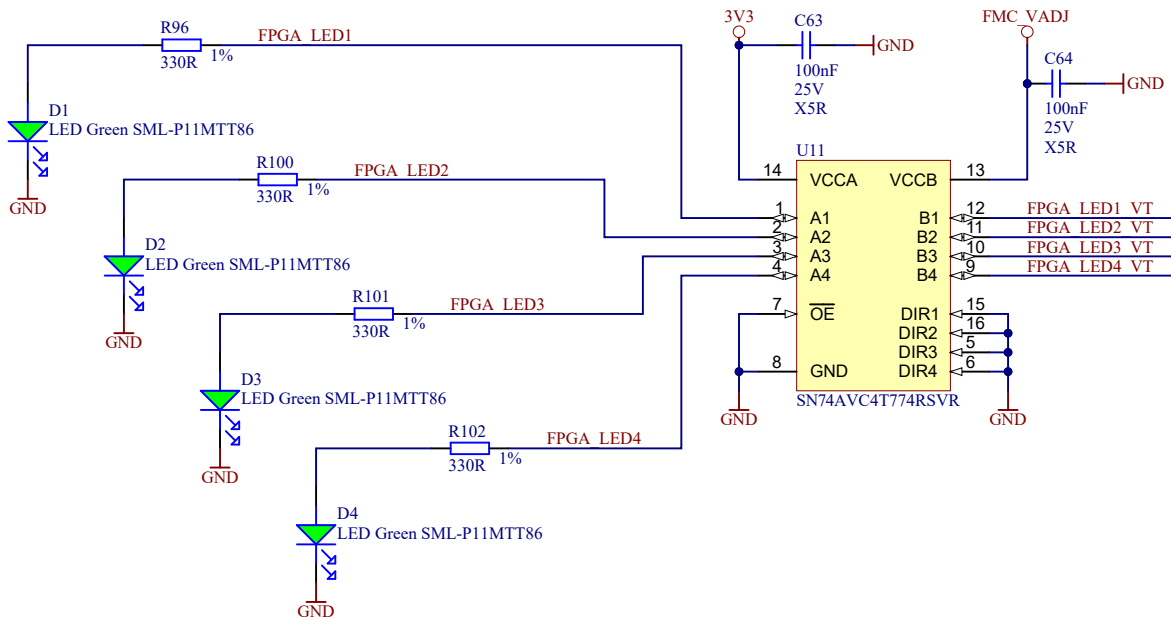
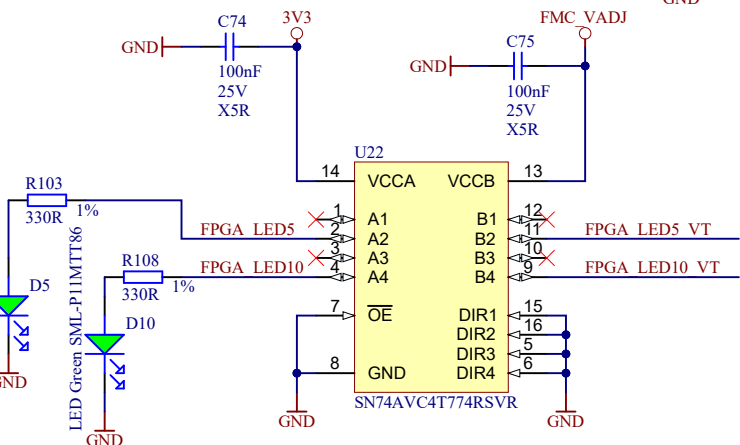


ATS-FPS058061011-40-C2-R0

HEATSINK TYPE 1 (FPGA)  
KK1



Hardware for HEATSINK TYPE 2 (FPGA)



|                       |                                  |             |
|-----------------------|----------------------------------|-------------|
| Title: TEF1001 - FPGA |                                  |             |
| A4                    | Number: TEF1001 B2IX4-K          | Rev. 02     |
| Date: 2018-02-26      | Copyright: Trenz Electronic GmbH | Page9 of 33 |
| Filename: FPGA.SchDoc |                                  |             |

A

A

B

B

C

C

D

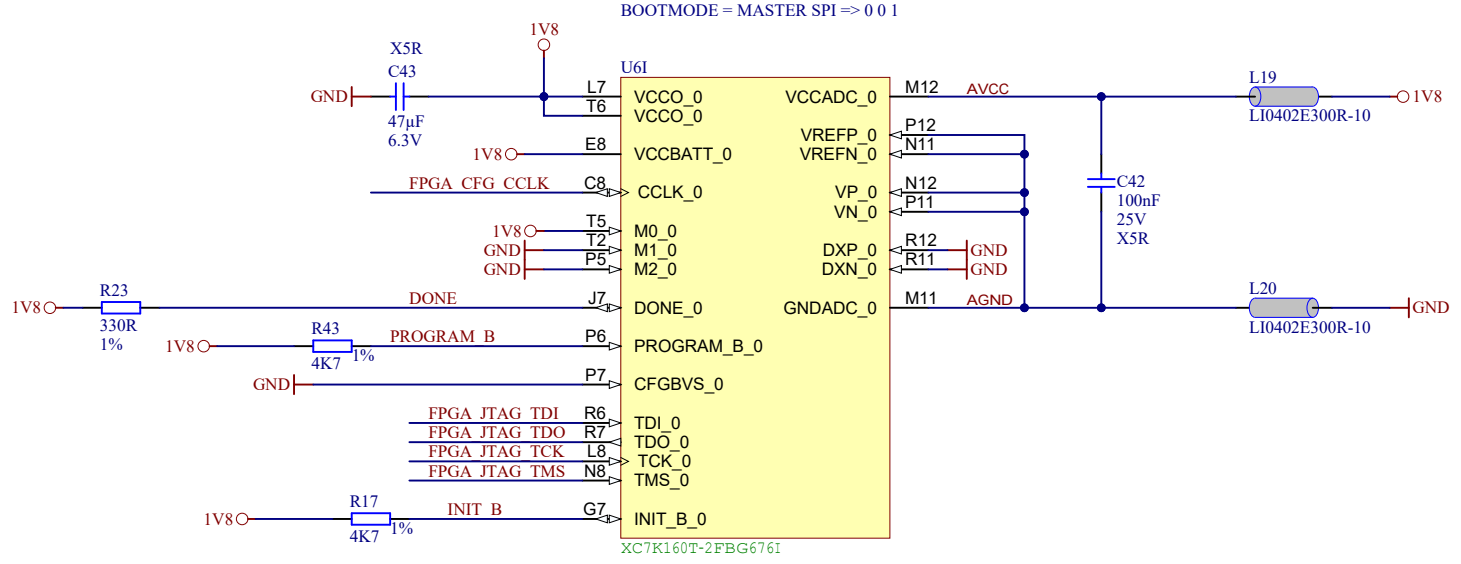
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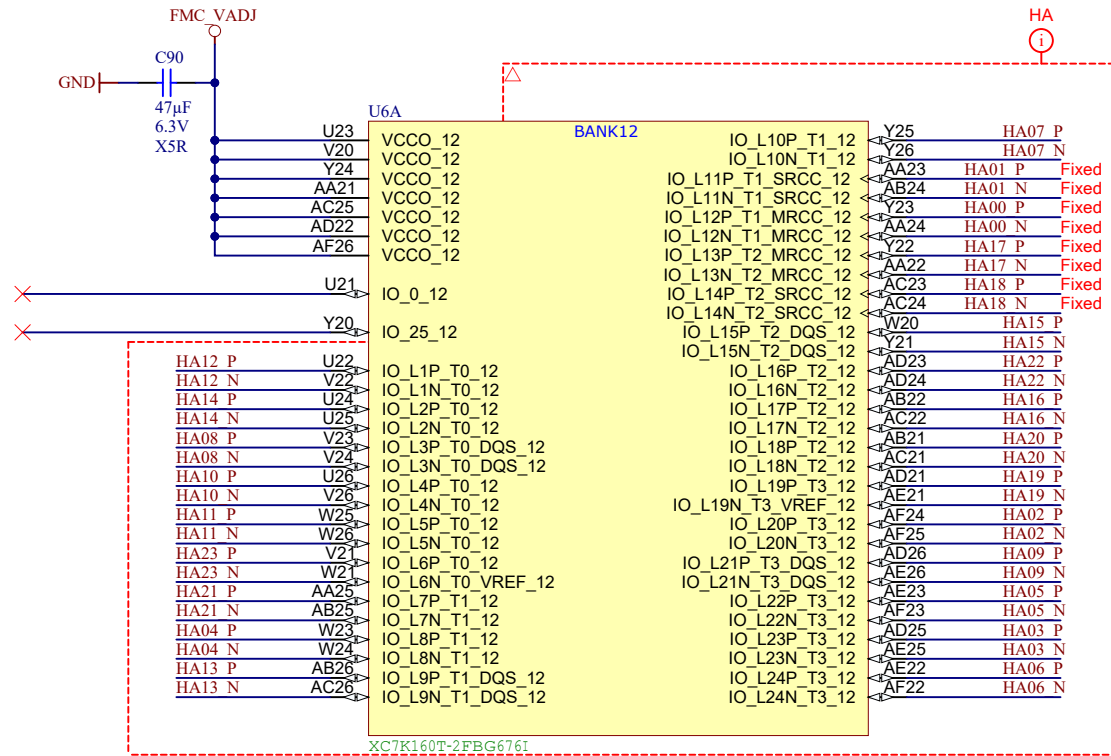
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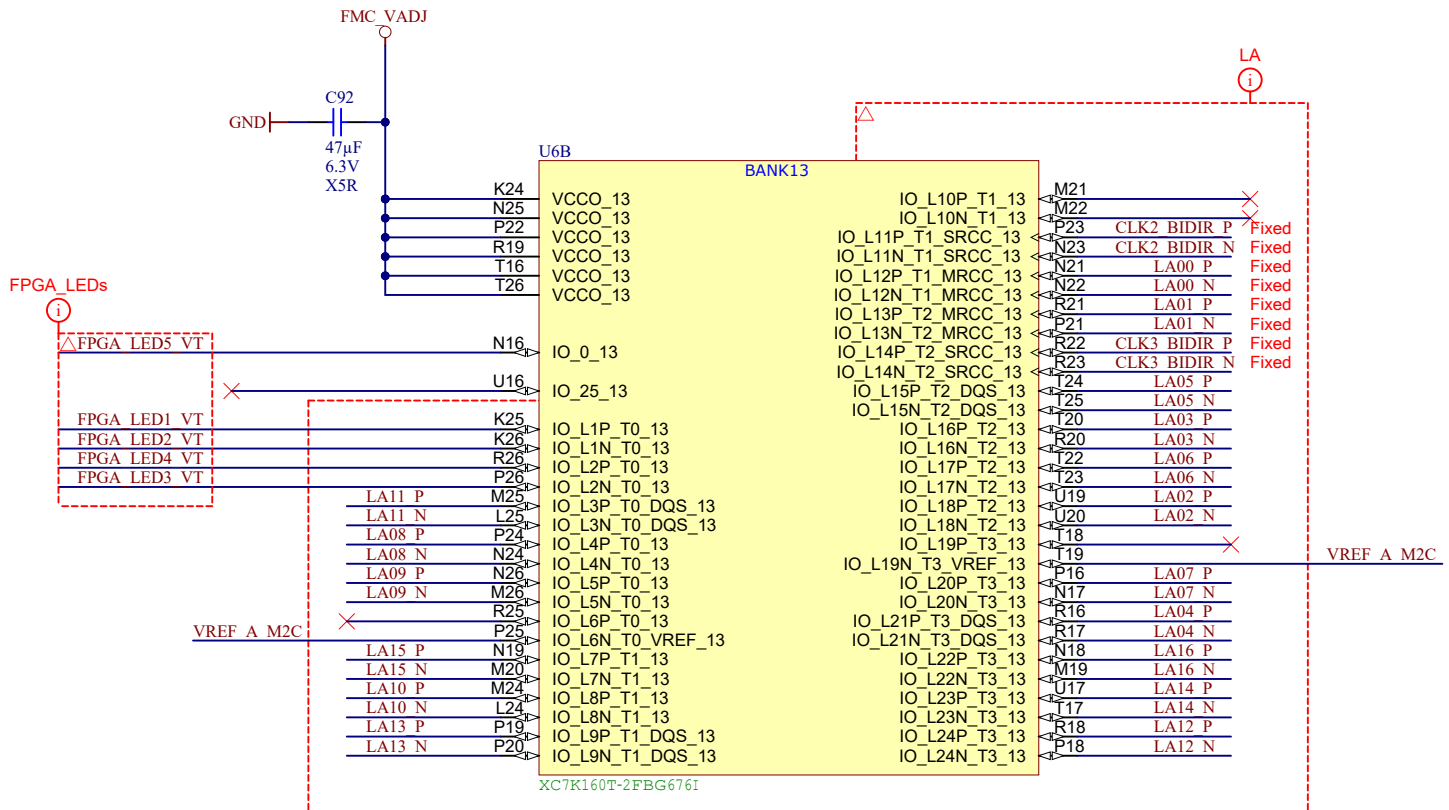
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|  |                           |                                  |               |
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|  | Title: TEF1001 - FPGA_CFG |                                  |               |
|  | A4                        | Number: TEF1001 B2IX4-K          | Rev. 02       |
|  | Date: 2018-02-26          | Copyright: Trenz Electronic GmbH | Page 10 of 33 |
|  | Filename: FPGA_CFG.SchDoc |                                  |               |



|  |                               |                                  |               |
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|  | Title: TEF1001 - FPGA_BANK_12 |                                  |               |
|  | A4                            | Number: TEF1001 B2IX4-K          | Rev. 02       |
|  | Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 11 of 33 |
|  | Filename: FPGA_BANK_12.SchDoc |                                  |               |



|                               |                                  |               |
|-------------------------------|----------------------------------|---------------|
| Title: TEF1001 - FPGA_BANK_13 |                                  |               |
| A4                            | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 12 of 33 |
| Filename: FPGA_BANK_13.SchDoc |                                  |               |

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A

A

B

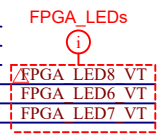
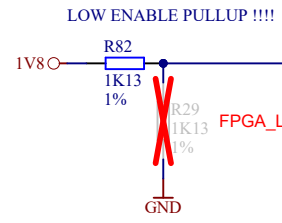
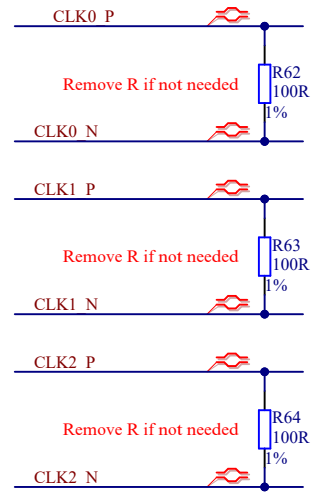
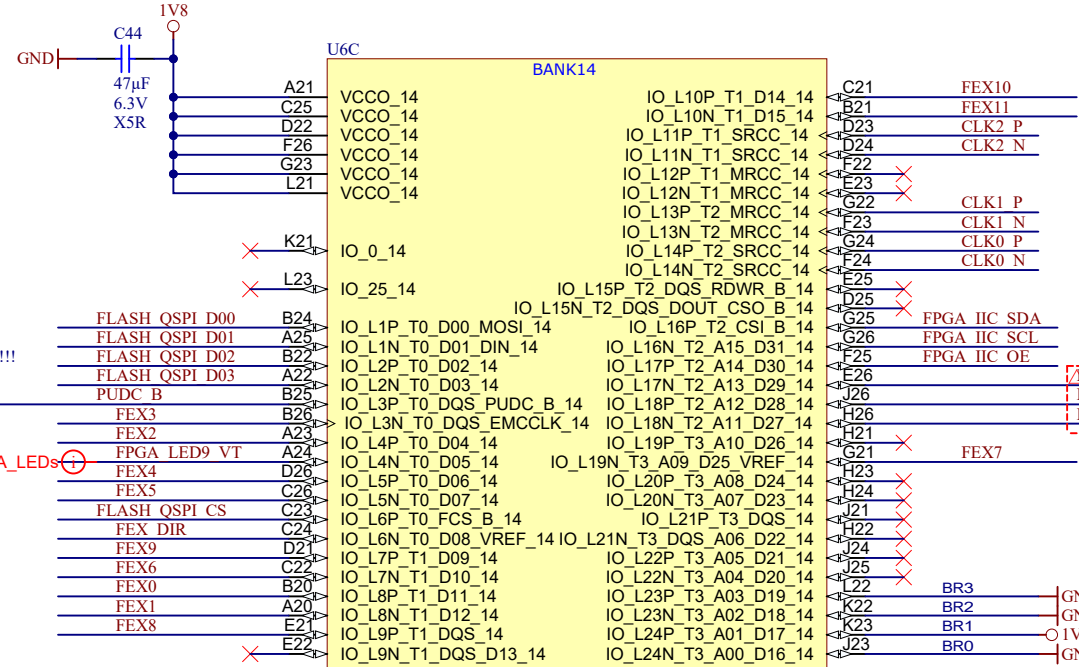
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C

C

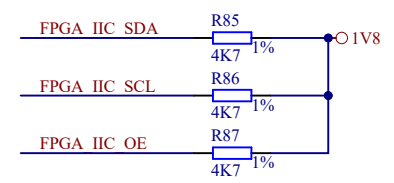
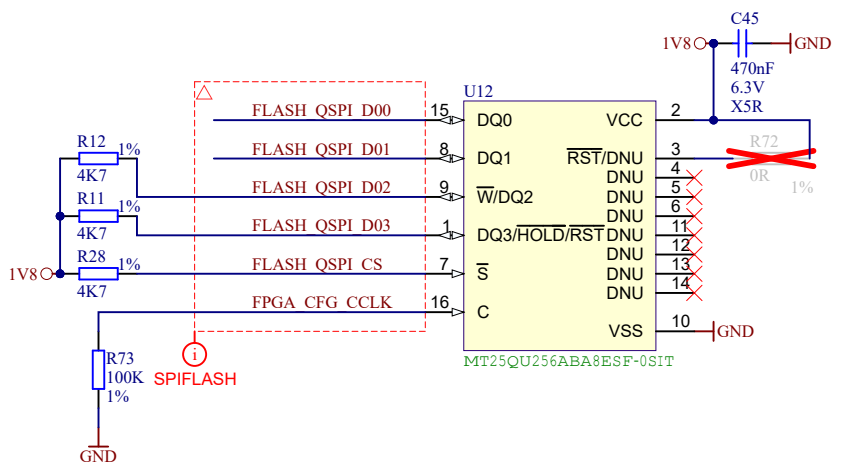
D

D



Board Revisions

| BR0 | BR1 | BR2 | BR3 |       |
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| 1   | 0   | 0   | 0   | REV01 |
| 0   | 1   | 0   | 0   | REV02 |



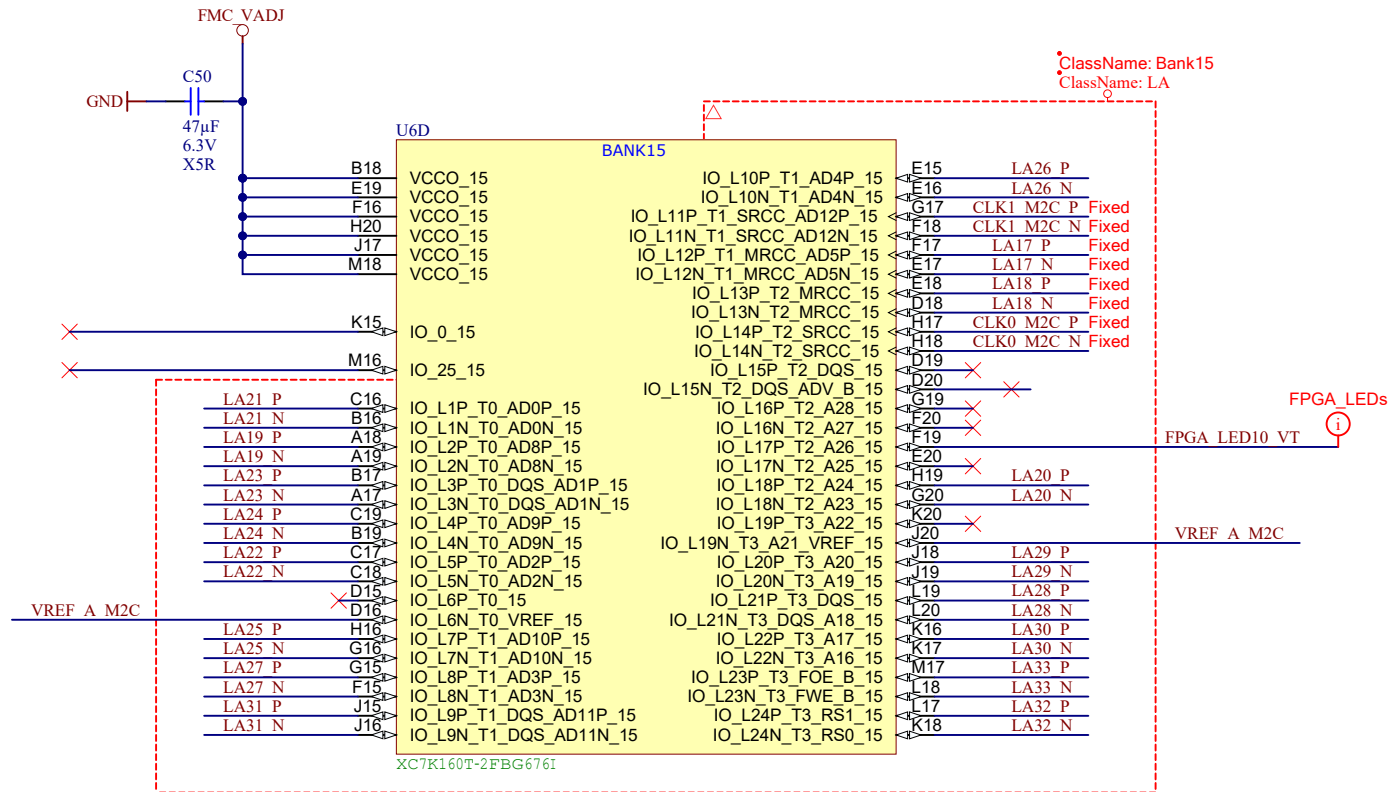
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| A4                            | Number: TEF1001 B2IX4-K          | Rev. 02      |
| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page13 of 33 |
| Filename: FPGA_BANK_14.SchDoc |                                  |              |

1

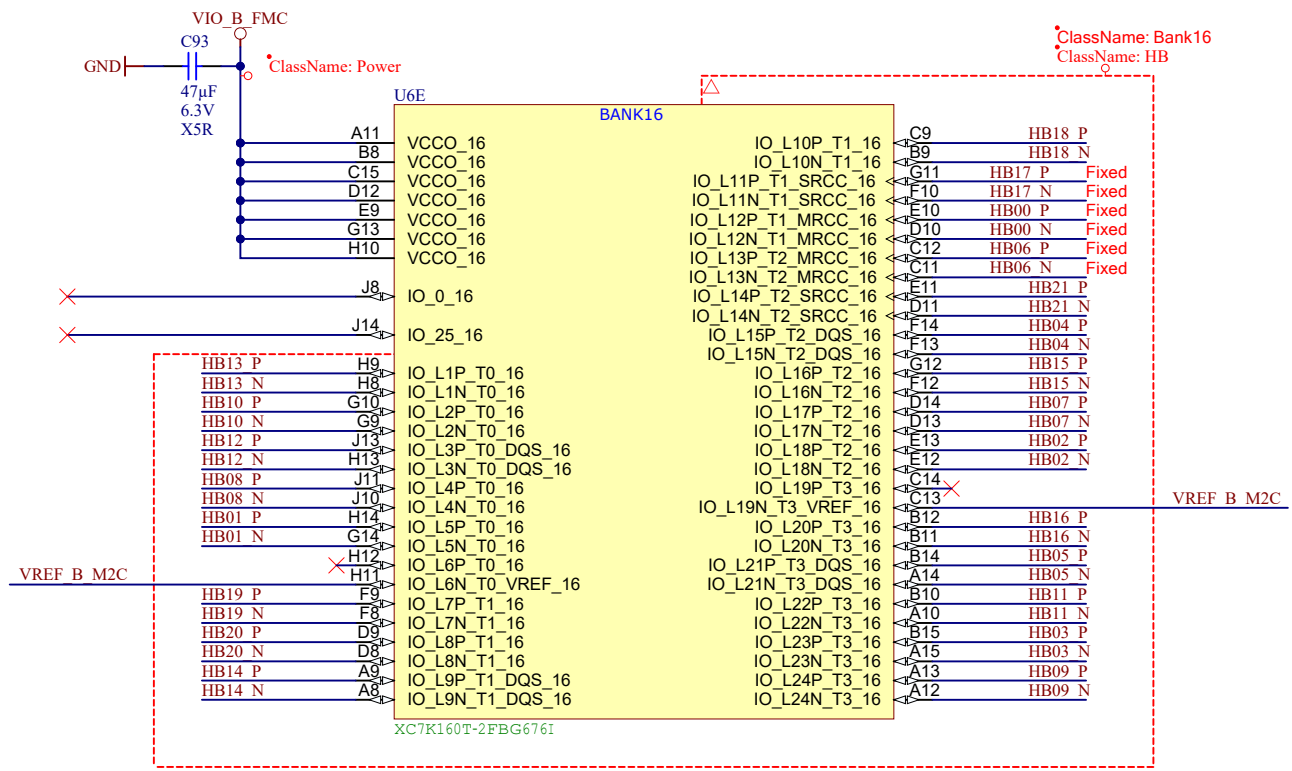
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3

4



|  |                               |                                  |               |
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|  | Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 14 of 33 |
|  | Filename: FPGA_BANK_15.SchDoc |                                  |               |



|                               |                                  |               |
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| Title: TEF1001 - FPGA_BANK_16 |                                  |               |
| A4                            | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 15 of 33 |
| Filename: FPGA_BANK_16.SchDoc |                                  |               |

1

2

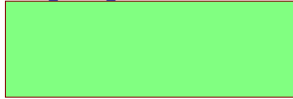
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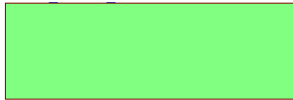
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A

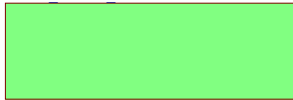
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FPGA\_BANK\_32.SchDoc



U\_FPGA\_BANK\_33  
FPGA\_BANK\_33.SchDoc



U\_FPGA\_BANK\_34  
FPGA\_BANK\_34.SchDoc



B

B

C

C

D


D

1

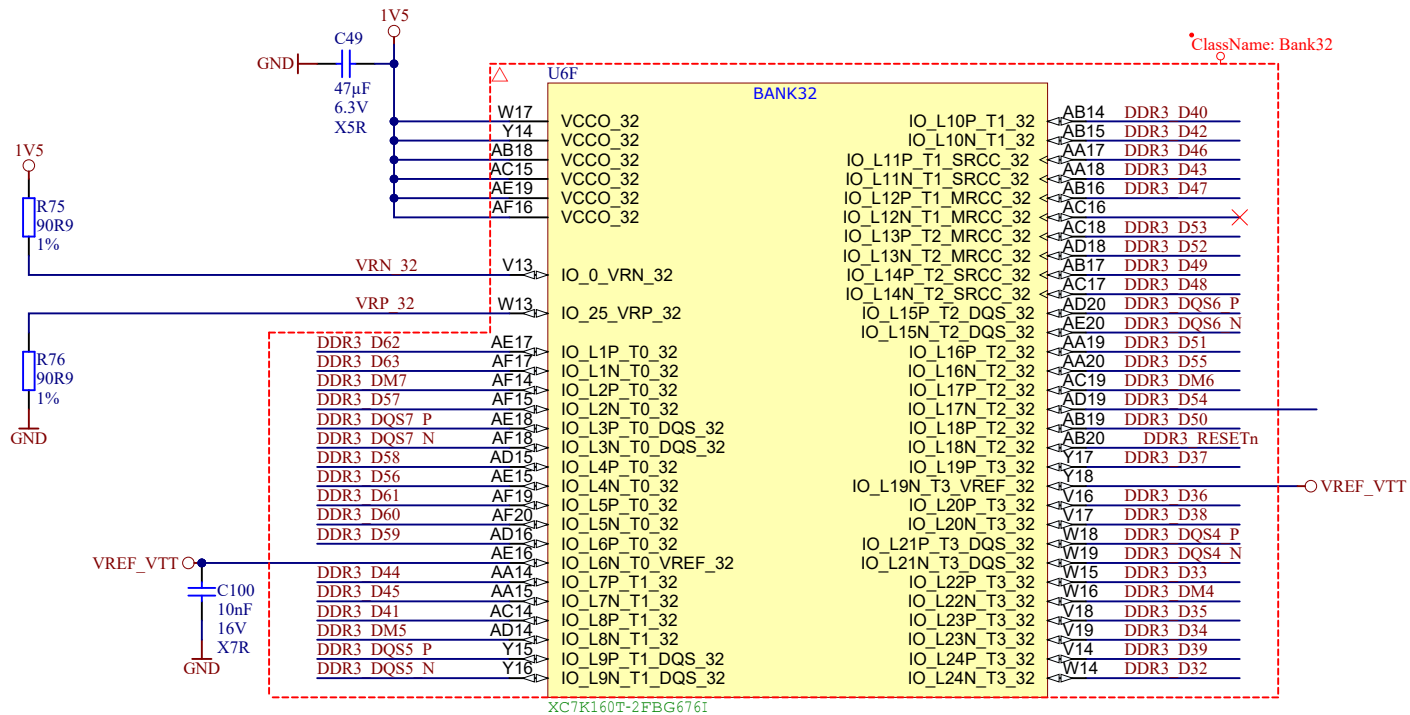
2

3

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|   |                            |                                  |               |
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|   | Date: 2018-02-26           | Copyright: Trenz Electronic GmbH | Page 16 of 33 |
|   | Filename: DDR_Banks.SchDoc |                                  |               |

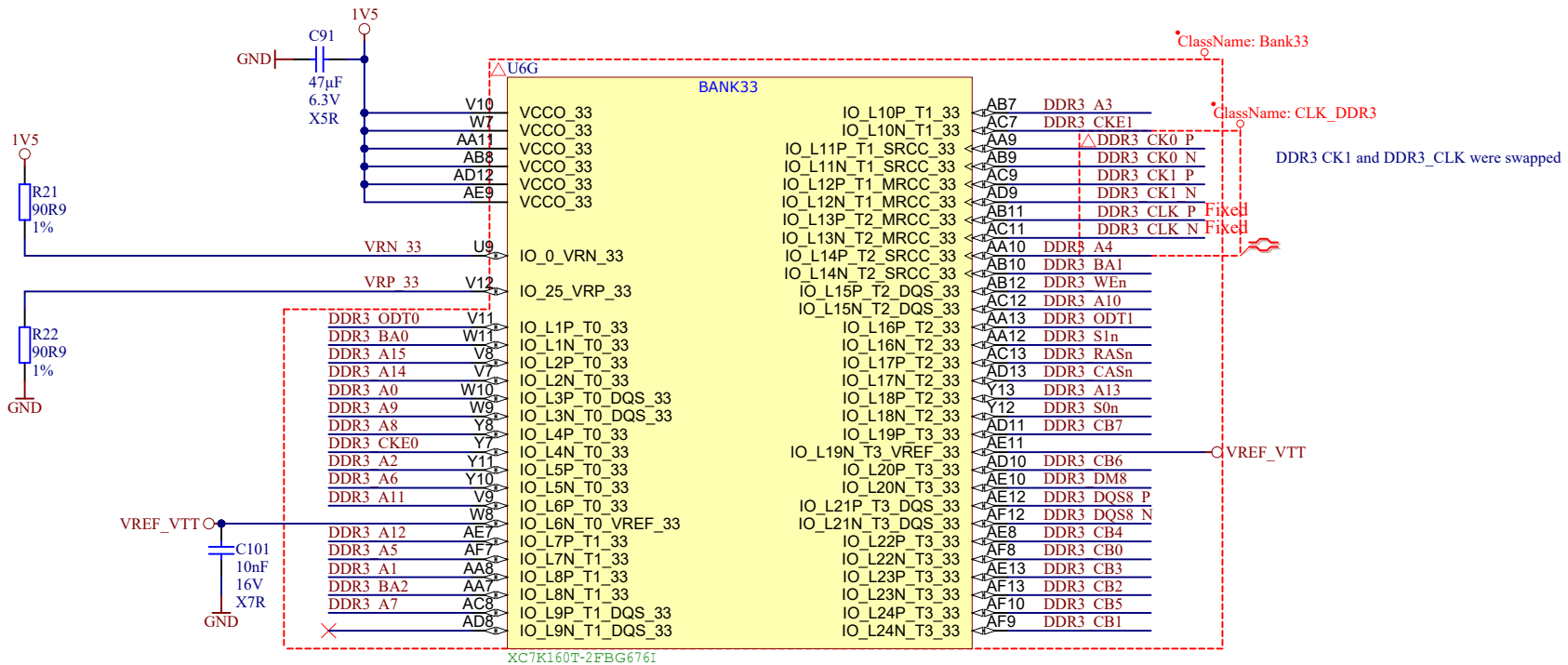




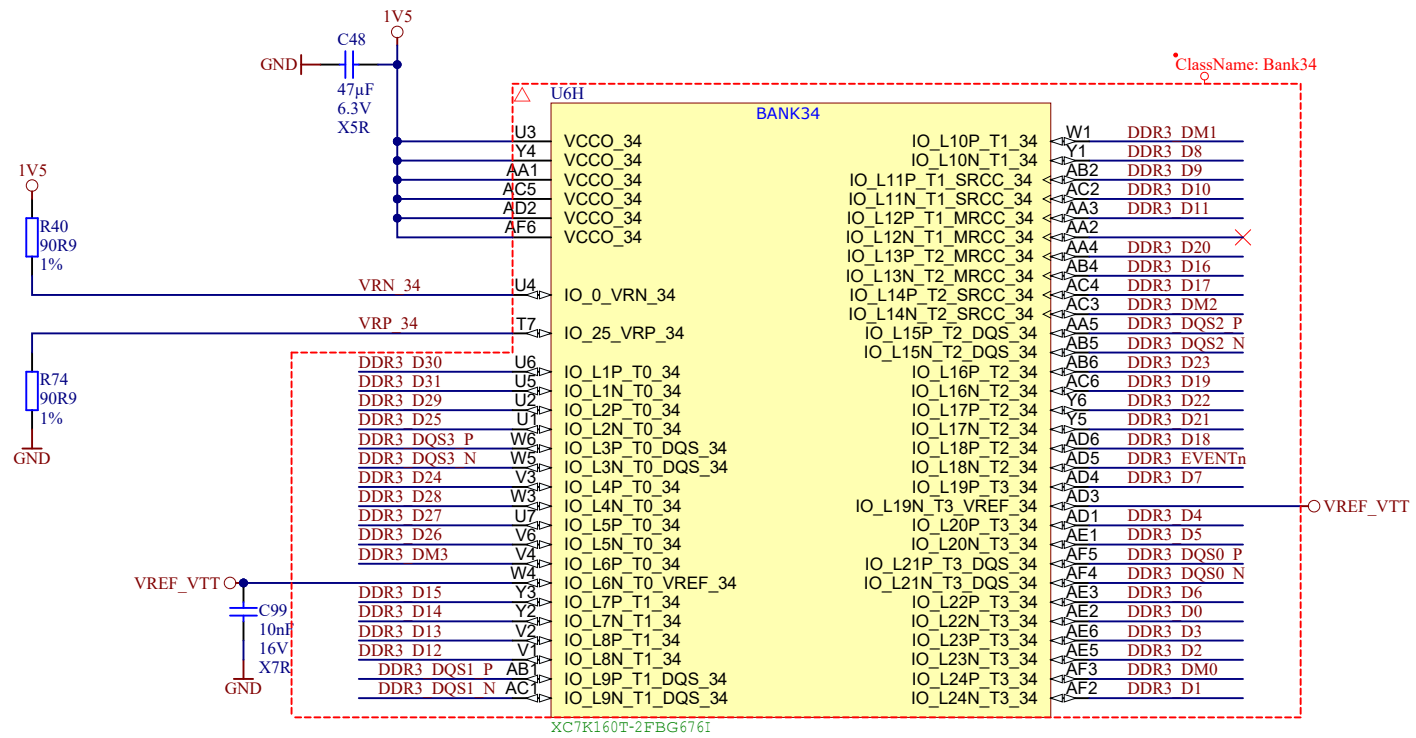
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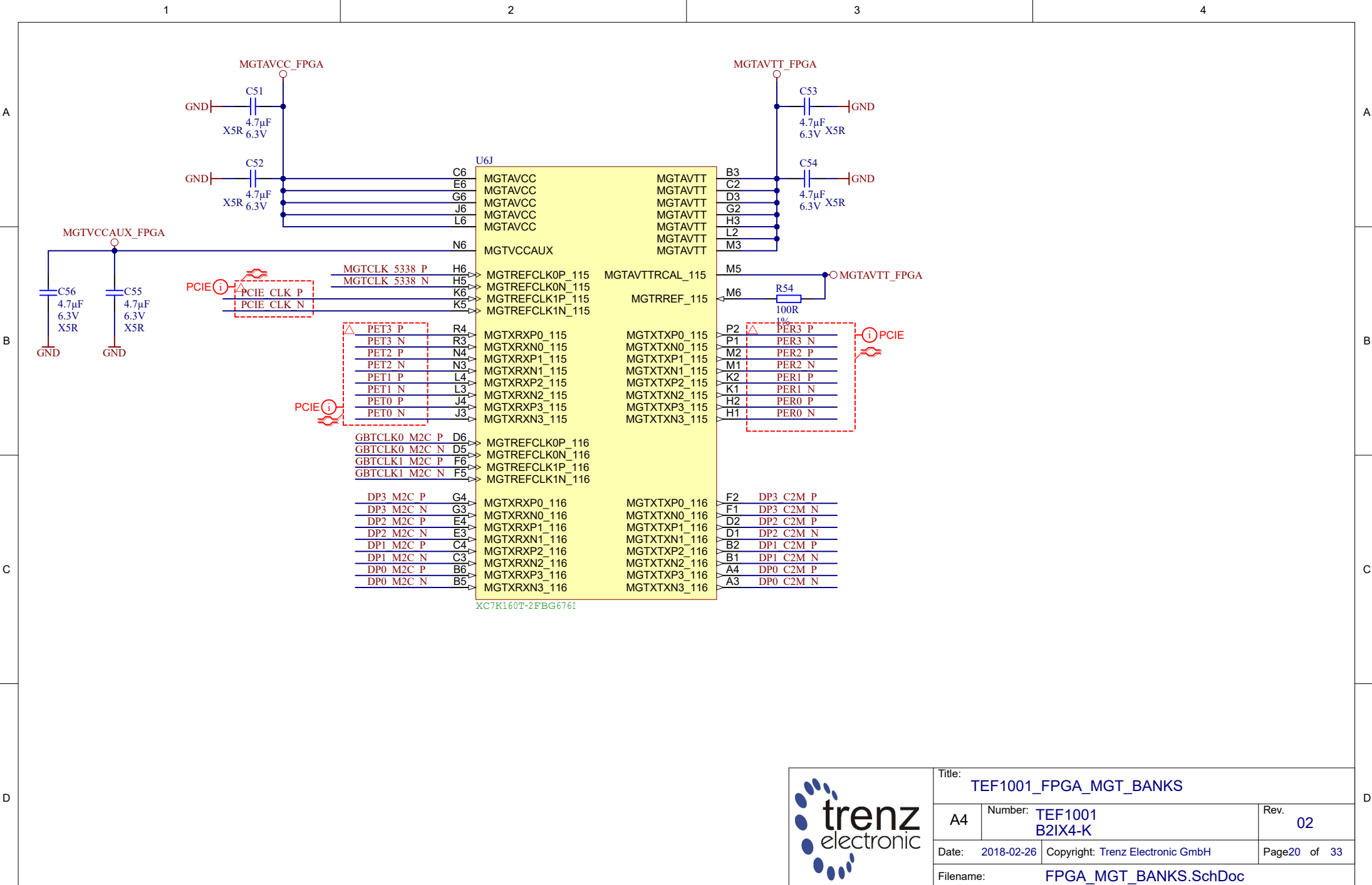
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| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 17 of 33 |
| Filename: FPGA_BANK_32.SchDoc |                                  |               |



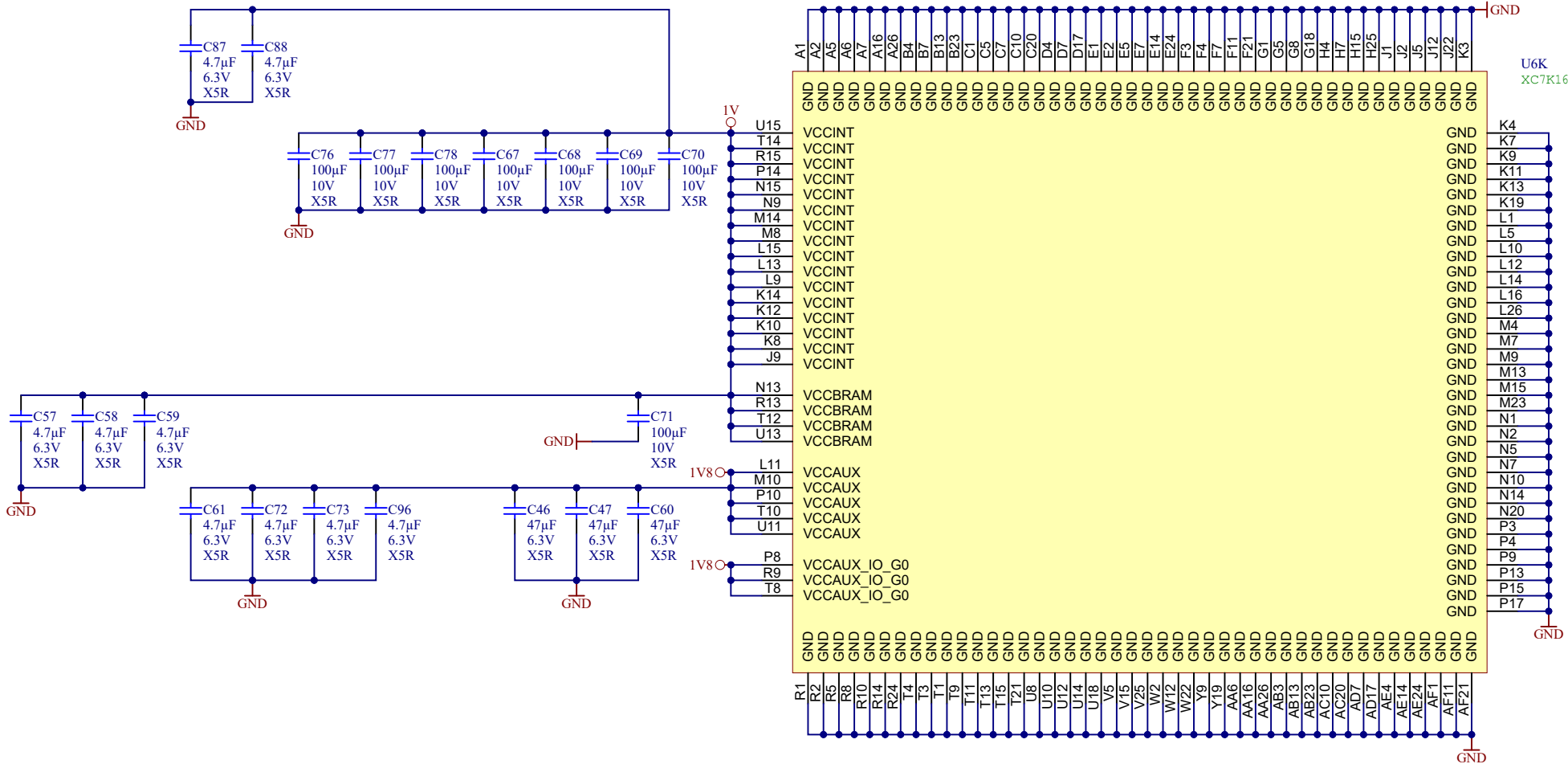
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| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 18 of 33 |
| Filename: FPGA_BANK_33.SchDoc |                                  |               |



|                               |                                  |               |
|-------------------------------|----------------------------------|---------------|
| Title: TEF1001 - FPGA_BANK_34 |                                  |               |
| A4                            | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26              | Copyright: Trenz Electronic GmbH | Page 19 of 33 |
| Filename: FPGA_BANK_34.SchDoc |                                  |               |



|  |                                 |                                  |
|--|---------------------------------|----------------------------------|
|  | Title: TEF1001_FPGA_MGT_BANKS   |                                  |
|  | A4                              | Number: TEF1001 B2IX4-K          |
|  | Date: 2018-02-26                | Copyright: Trenz Electronic GmbH |
|  | Filename: FPGA_MGT_BANKS.SchDoc | Page20 of 33                     |



|                             |                                  |              |
|-----------------------------|----------------------------------|--------------|
| Title: TEF1001 - FPGA_POWER |                                  |              |
| A4                          | Number: TEF1001<br>B2IX4-K       | Rev. 02      |
| Date: 2018-02-26            | Copyright: Trenz Electronic GmbH | Page21 of 33 |
| Filename: FPGA_POWER.SchDoc |                                  |              |

A

B

C

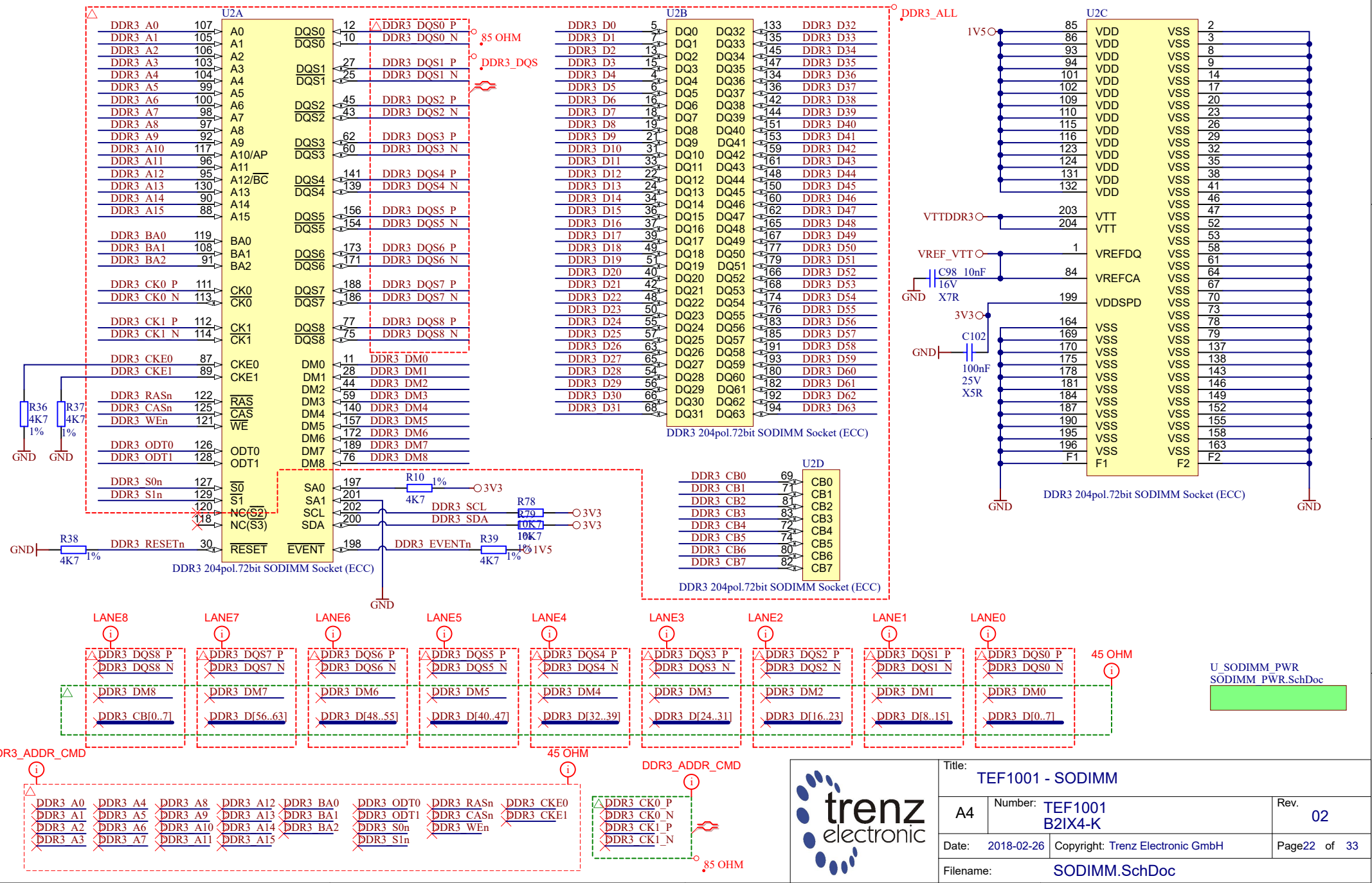
D

A

B

C

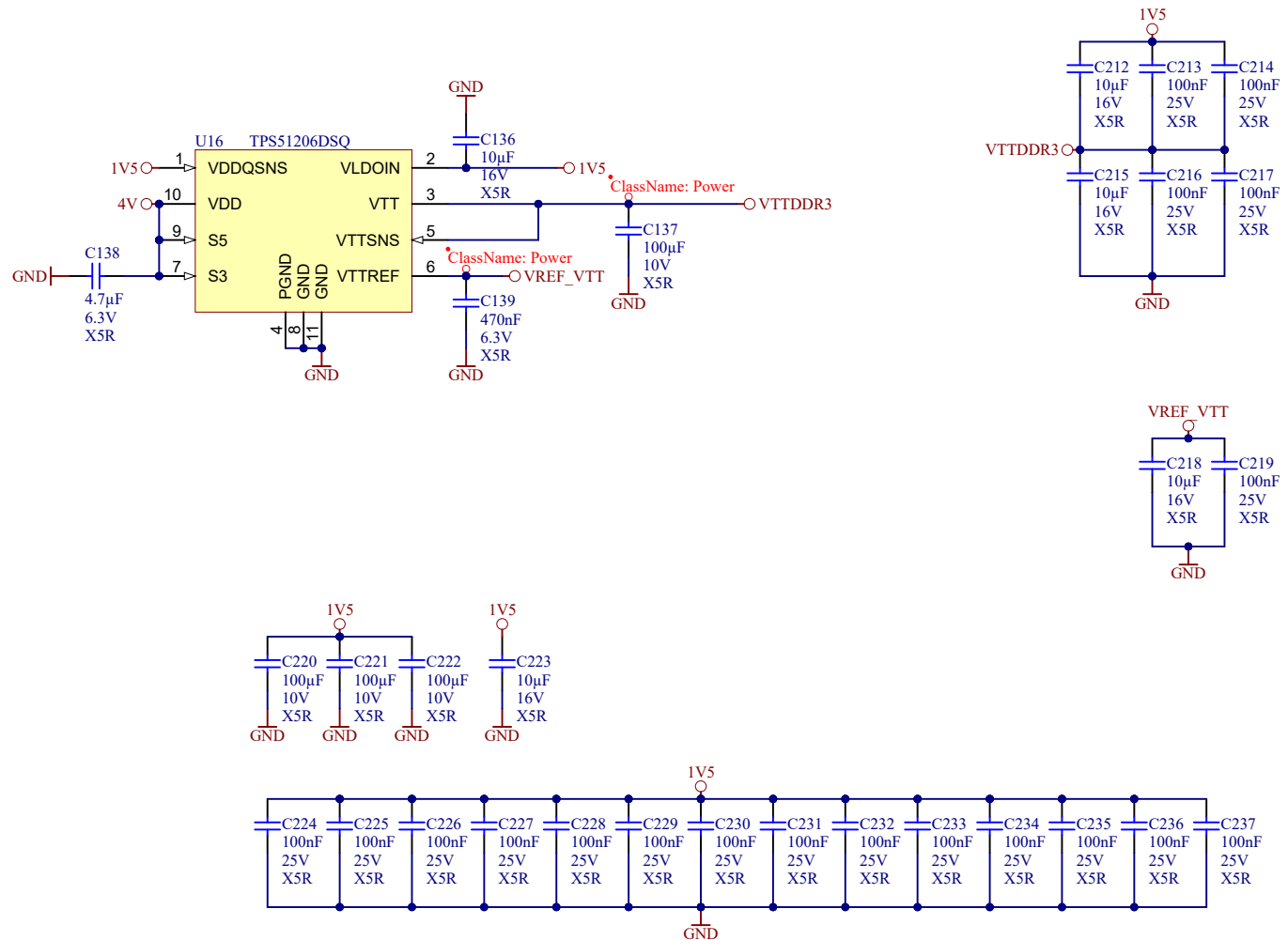
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U\_SODIMM\_PWR  
SODIMM\_PWR.SchDoc



|                         |                                  |               |
|-------------------------|----------------------------------|---------------|
| Title: TEF1001 - SODIMM |                                  |               |
| A4                      | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26        | Copyright: Trenz Electronic GmbH | Page 22 of 33 |
| Filename: SODIMM.SchDoc |                                  |               |



|                             |                                  |                             |
|-----------------------------|----------------------------------|-----------------------------|
| Title: TEF1001 - SODIMM_PWR |                                  |                             |
| A4                          | Number: TEF1001<br>B2IX4-K       | Rev. 02                     |
| Date: 2018-02-26            | Copyright: Trenz Electronic GmbH |                             |
| Page 23 of 33               |                                  | Filename: SODIMM_PWR.SchDoc |

U\_PWR\_4V\_1V5  
PWR\_4V\_1V5.SchDoc

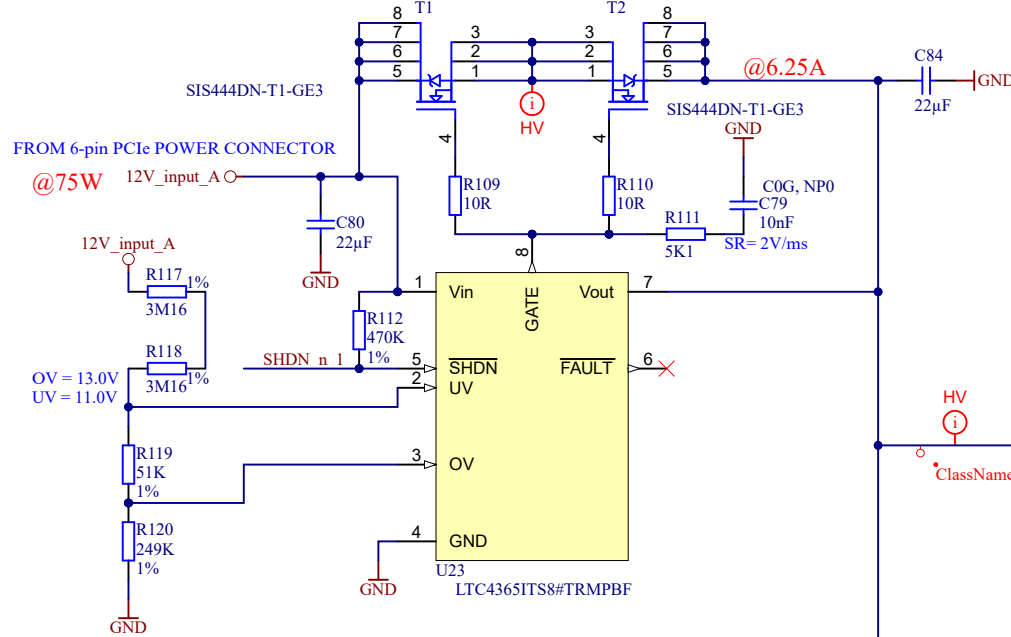
U\_PWR\_3V3  
PWR\_3V3.SchDoc

U\_PWR\_1V  
PWR\_1V.SchDoc

U\_PWR\_MGT  
PWR\_MGT.SchDoc

U\_PWR\_1V8  
PWR\_1V8.SchDoc

U\_PWR\_5V  
PWR\_5V.SchDoc



FAN FPGA

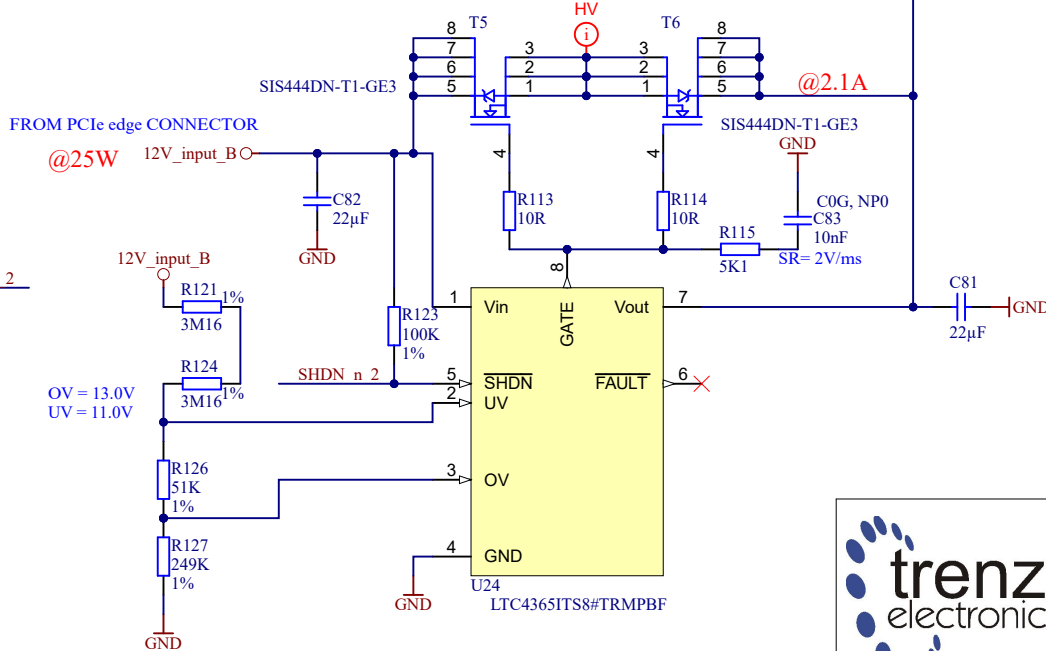
FMC J2 Connector MIN11.4V MAX12.6V (Sec. 5.10. Power Supply Req.)

U4 REGULATOR 1V MIN5.75V MAX26.5V

U3 REGULATOR 4V&1V5 MIN5.75V MAX26.5V

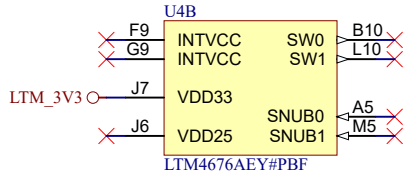
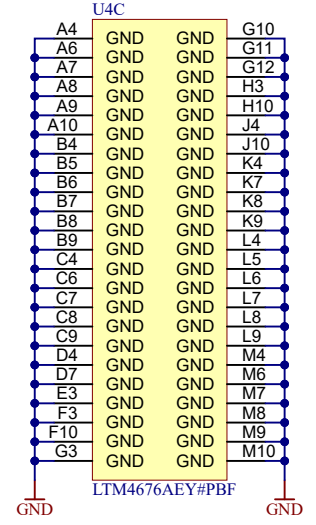
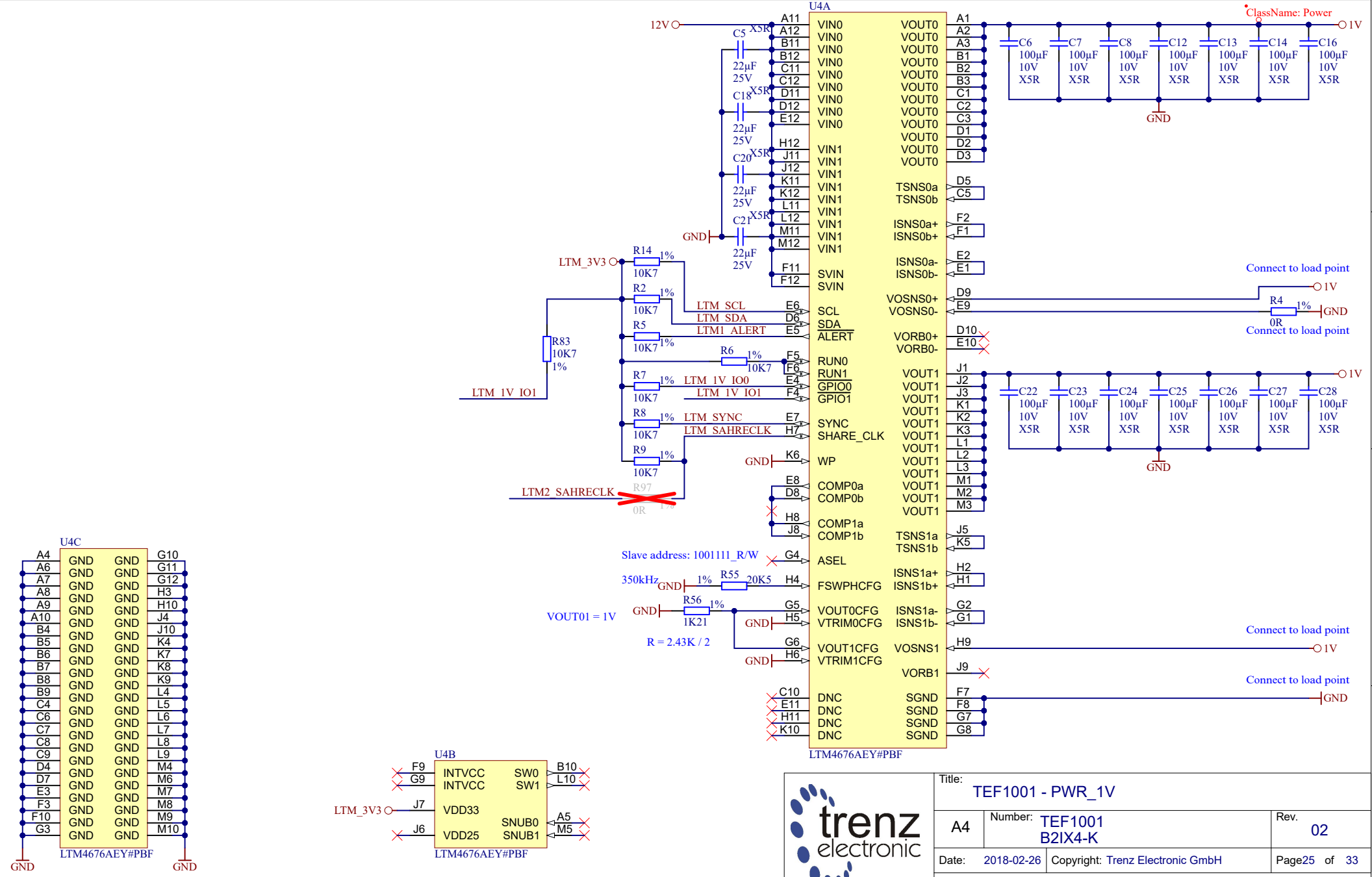
U9 REGULATOR 3V3 MIN4.5V MAX17V

U8 REGULATOR 5V MIN6V MAX17V

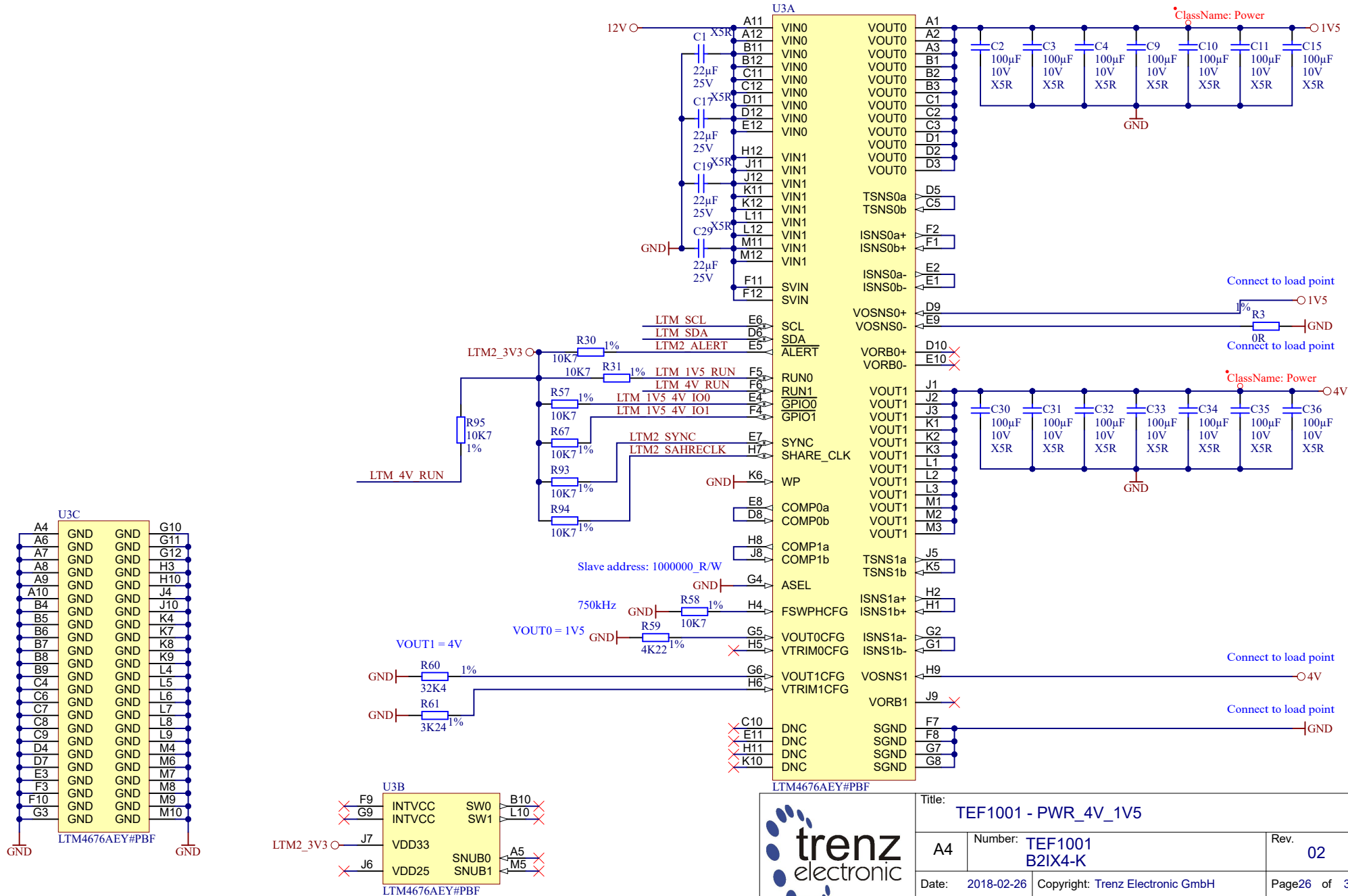


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| Title: TEF1001 - POWER |                                  |              |
| A4                     | Number: TEF1001 B2IX4-K          | Rev. 02      |
| Date: 2018-02-26       | Copyright: Trenz Electronic GmbH | Page24 of 33 |
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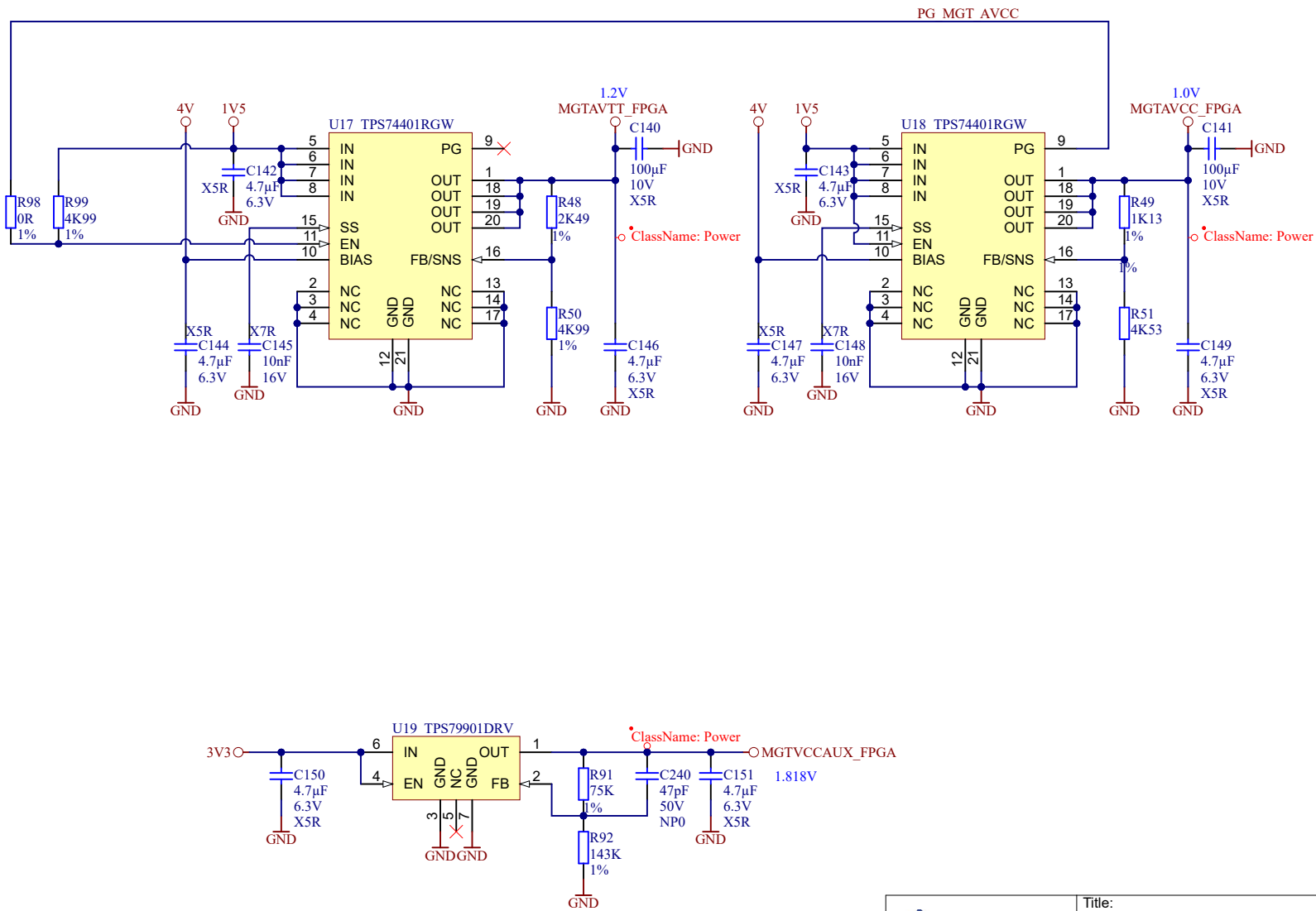




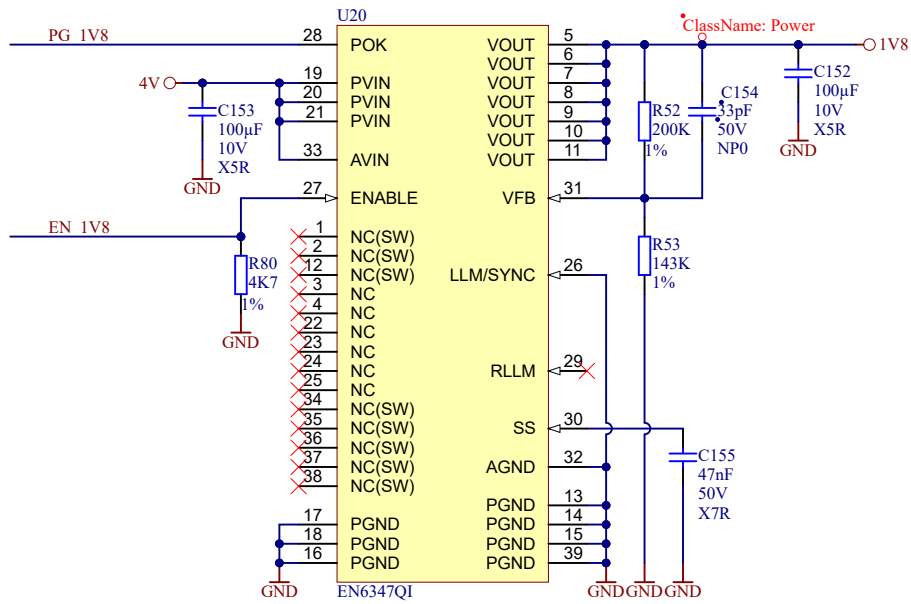
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| A4                      | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26        | Copyright: Trenz Electronic GmbH | Page 25 of 33 |
| Filename: PWR_1V.SchDoc |                                  |               |




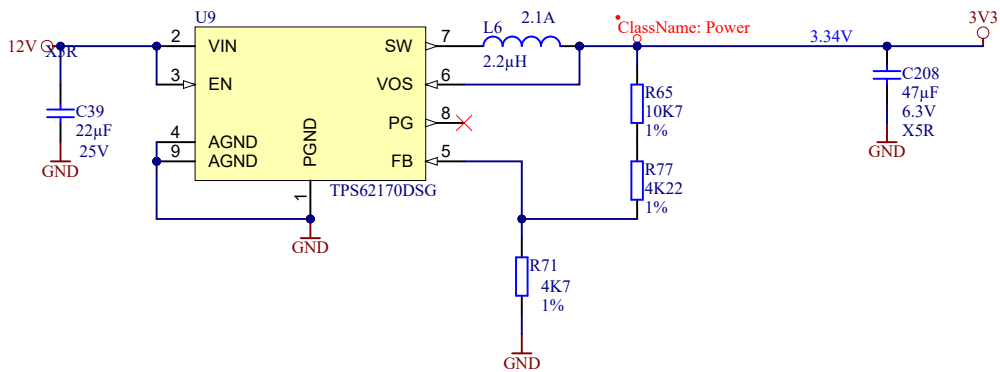
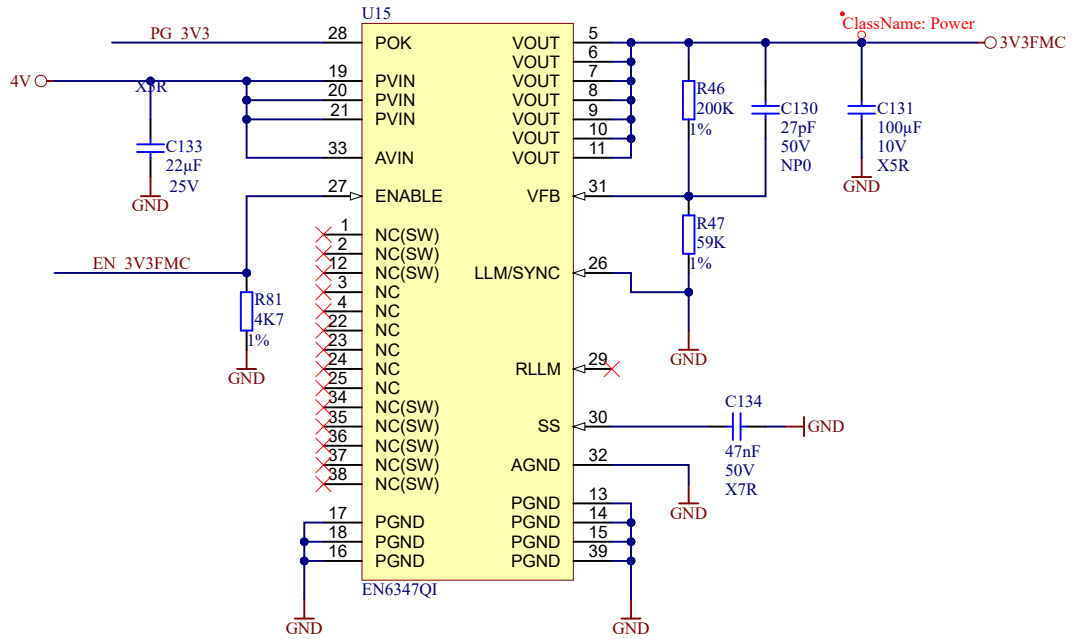
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| Date: 2018-02-26            | Copyright: Trenz Electronic GmbH | Page 26 of 33 |
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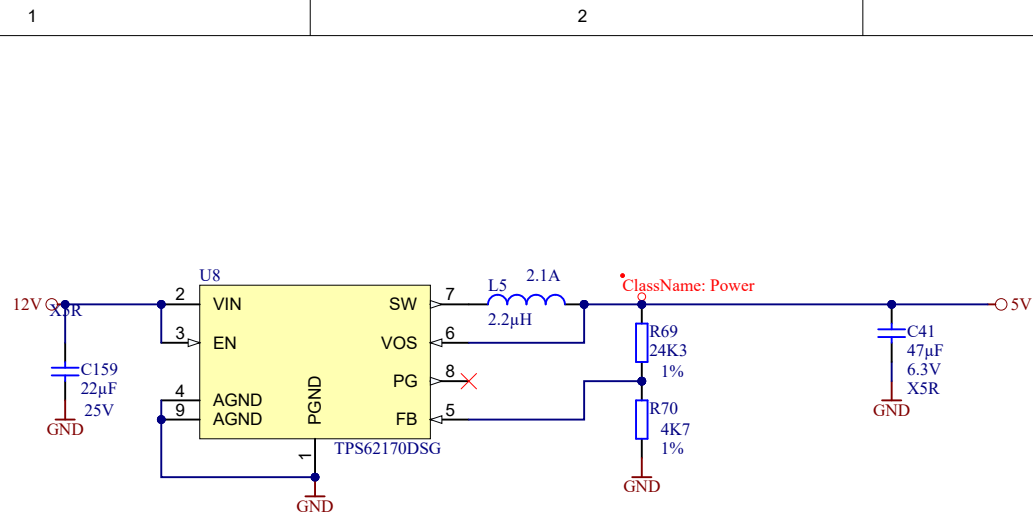
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| A4                       | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26         | Copyright: Trenz Electronic GmbH | Page 27 of 33 |
| Filename: PWR_MGT.SchDoc |                                  |               |




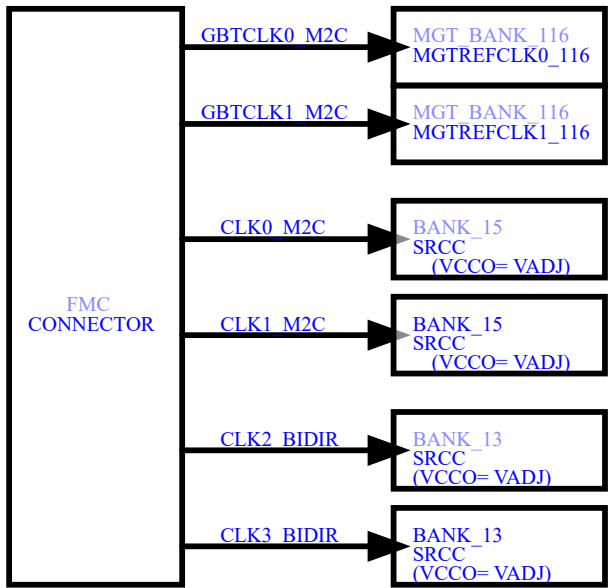
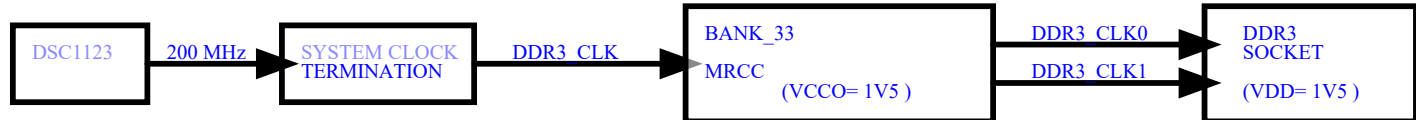
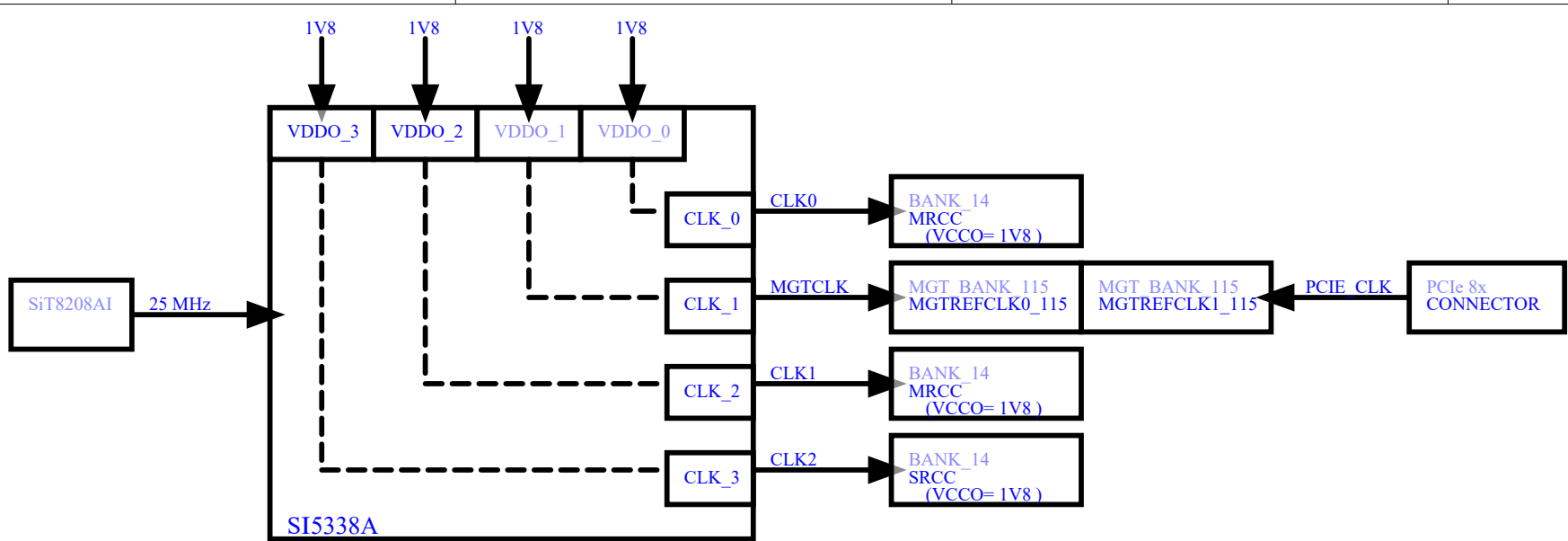
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| Date: 2018-02-26  |  | Copyright: Trenz Electronic GmbH |                          | Page 28 of 33           |
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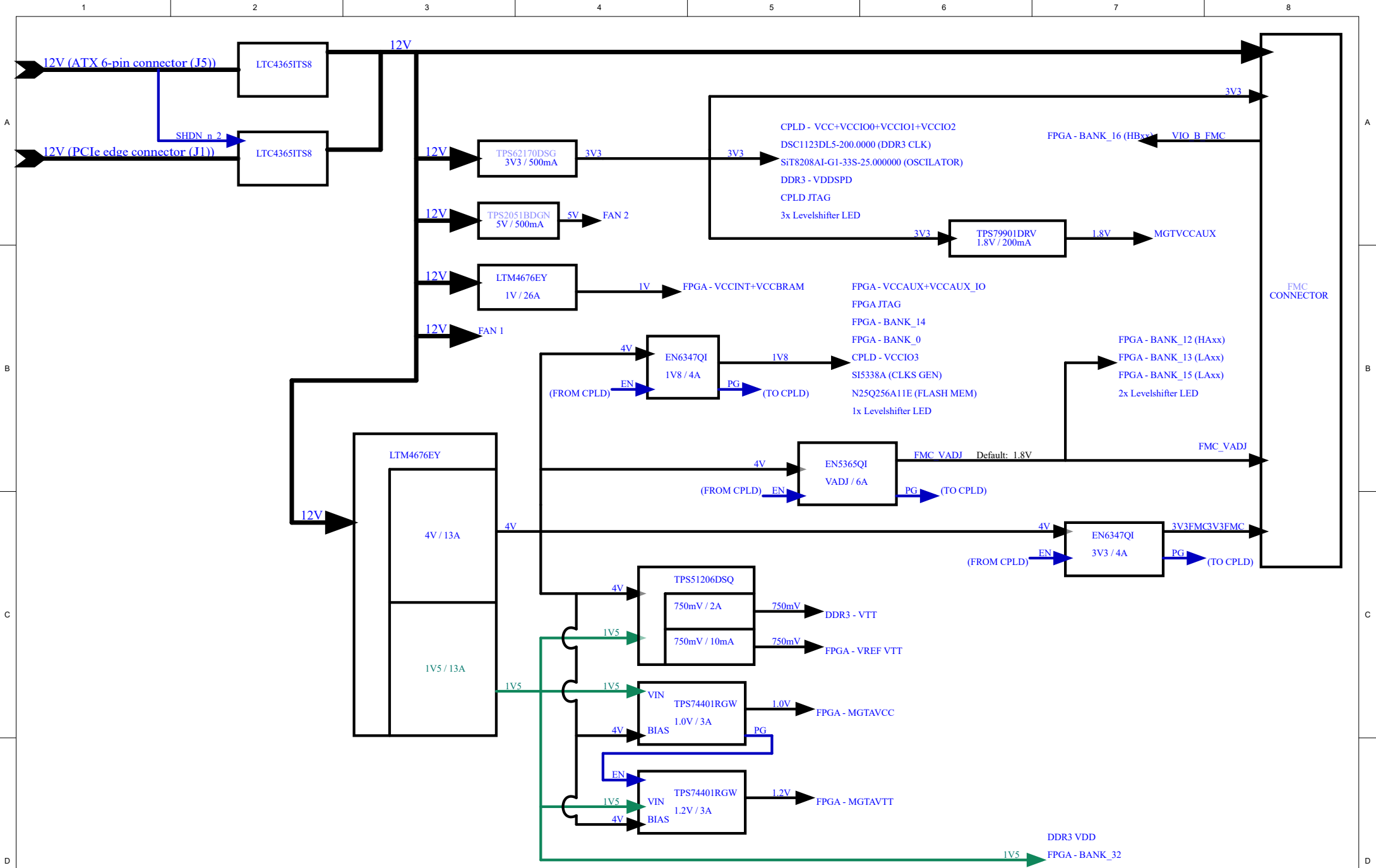
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| Filename: PWR_3V3.SchDoc |                                  |              |



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|  |  | Title: TEF1001 - PWR_5V          |                            |
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| Filename: PWR_5V.SchDoc   |  | Page 30 of 33                    |                            |



|                                  |                                  |               |
|----------------------------------|----------------------------------|---------------|
| Title: TEF1001 - Clock Overview  |                                  |               |
| A4                               | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26                 | Copyright: Trenz Electronic GmbH | Page 31 of 33 |
| Filename: CLOCKS OVERVIEW.SchDoc |                                  |               |



|   |                                  |               |
|---|----------------------------------|---------------|
| Title: TEF1001 - Power Ens_PGs_COMMs    |                                  |               |
| A4                                      | Number: TEF1001 B2IX4-K          | Rev. 02       |
| Date: 2018-02-26                        | Copyright: Trenz Electronic GmbH | Page 32 of 33 |
| Filename: POWER_ENs_PGs OVERVIEW.SchDoc |                                  |               |




Revision 02:

- 1) added C87, C88 4.7µF
- 2) C154 incremented from 27pF to 33pF
- 3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
- 4) added S1 (FMC\_VADJ value, and JTAG\_EN)
- 5) T4 and resistors added for reading the FMC\_PRSNT\_M2C value
- 6) U25 and capacitors added (FMC\_FAN)
- 7) added screws for bracket
- 8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)

Revision 02a (2020-04-15):

- 1) VY: New FAN M1, F455B-05MD replaced by F455B-05LD

|   |  |   |                             |
|---|--|---|-----------------------------|
|  | Title: <b>TEF1001 - Revision history</b> |   |                             |
|   | A4                                       | Number: <b>TEF1001<br/>B2IX4-K</b>      | Rev. <b>02</b>              |
|   | Date: <b>2018-11-19</b>                  | Copyright: <b>Trenz Electronic GmbH</b> | Page <b>33</b> of <b>33</b> |
|   | Filename: <b>Revision_Changes.SchDoc</b> |   |                             |